AN INTERLINE DYNAMIC VOLTAGE RESTORER (IDVR)

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Abstract - *This paper deals with improving the voltage quality of sensitive loads from voltage sags using interline dynamic voltage restorer (IDVR). The higher active power requirement associated with voltage phase jump compensation has caused a substantial rise in size and cost of dc link energy storage system of DVR. The existing control strategies either mitigate the phase jump or improve the utilization of dc link energy by (i) reducing the amplitude of injected voltage, or (ii) optimizing the dc bus energy support. In this paper, an enhanced sag compensation strategy is proposed that mitigates the phase jump in the load voltage while improving the overall sag compensation time. An analytical study shows that the proposed method significantly increases the DVR sag support time (more than 50%) compared with the existing phase jump compensation methods. This enhancement can also be seen as a considerable reduction in dc link capacitor size for new installation. The performance of proposed method is evaluated using simulation study and finally, verified experimentally on a scaled lab prototype.*

***Key Words*: dynamic voltage restorer (DVR), sag/swell, dc link capacitor, total harmonic distortion.**

1. INTRODUCTION

In the industrial distribution systems, the grid voltage disturbances (voltage sags, swells, flicker and harmonics) are the most common power quality problems. Sag is the most frequent voltage disturbance which is typically caused by fault at remote bus and is always accompanied by a phase angle jump. The phase angle jump in the voltage can initiate transient current in the capacitors, transformers and motors. It can also disturb the operation of converters and may lead to glitch in the performance of thyristor based loads. In order to protect sensitive loads from grid voltage sags, custom power devices (such as, SVC, D-STAT COM, DVR and UPQC) are being widely used. Among these devices, IDVR has emerged as the most cost effective and comprehensive solution. It consists of a dc link capacitor (serving as energy reserve for DVR), series injection transformer, six switch VSI and LC filter for removing switching harmonics from injected voltage. The primary function of IDVR is to inject a voltage with certain magnitude and phase angle. This paper proposes a new control strategy in which the main objective is to enhance the sag compensation time while mitigating the voltage phase angle jump. The performance of proposed method is validated using simulation as well as experimental studies.

1.1 Inverter

An inverter is an electronic device that converts direct current (DC) to alternating current (AC). Direct current is created by devices, such as batteries and solar panels, which is converted into AC by an inverter. It does not produce any power, the power is provided by DC source. It is widely used in industrial and domestic application. Inverters are made in many different sizes.

1.2 Square wave

This is one of the simplest waveforms an inverter design can produce and is best suited to low-sensitivity applications such as lighting and heating. Generally, square wave output is not suitable for sensitive electronics.

2. IDVR:

Interline Dynamic voltage restorer (IDVR) is a method of overcoming voltage sags which occur in electrical power distribution. Voltage sags reduce the efficiency. IDVR saves energy through voltage injections that can affect the phase and wave shape of the power being supplied. The basic principle of interline dynamic voltage restorer is to inject a voltage of the necessary magnitude and frequency to restore the load side voltage to the desired amplitude and waveform, even when the source voltage is unbalanced or distorted. The IDVR can generate or absorb independently controllable real and reactive power at the load side.

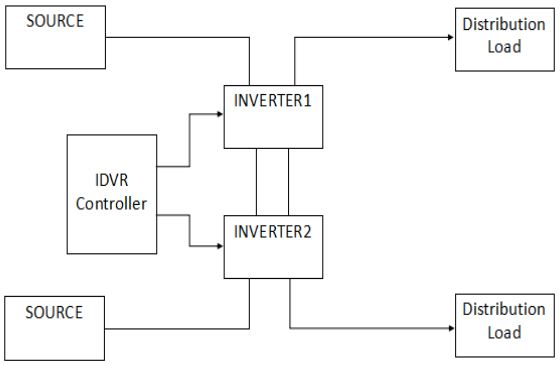


Fig 2.1: block diagram of interline dynamic voltage restorer

The main objective is to maintain voltage quality using IDVRs with improved DF in feeders. In this block diagram, there are

two power system feeders. The first system represents that it is in normal condition. When fault occurs in second system, it will acts & adjust the dc link voltage. There are two converters used for two IDVR feeders, the converter will maintain and injects the active and reactive power when the system fault occurs. The work of the controller is to compare the two feeder voltages and dc link voltages using dc voltage controller & ac voltage controller. This control value, DF error value & PQ enable value switching to the control output, it gives to the PWM control.

The circuit diagram of an Interline Dynamic Voltage Restorer using voltage controlled source is shown in Fig.2.2. The 3-phase voltage source inverter is connected to the secondary side of the isolation transformer. Whenever fault occurs, the IDVR controller injects voltage to the transmission line. Here, we are using MOSFET as switching devices.

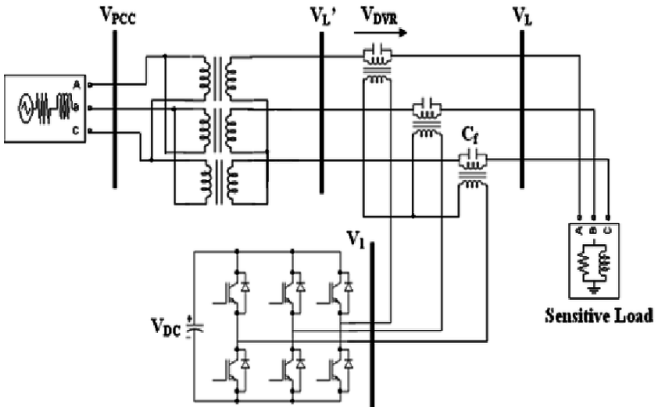


Fig.2.2: circuit diagram of interline dynamic voltage restorer.

3.SIMULATION AND RESULTS

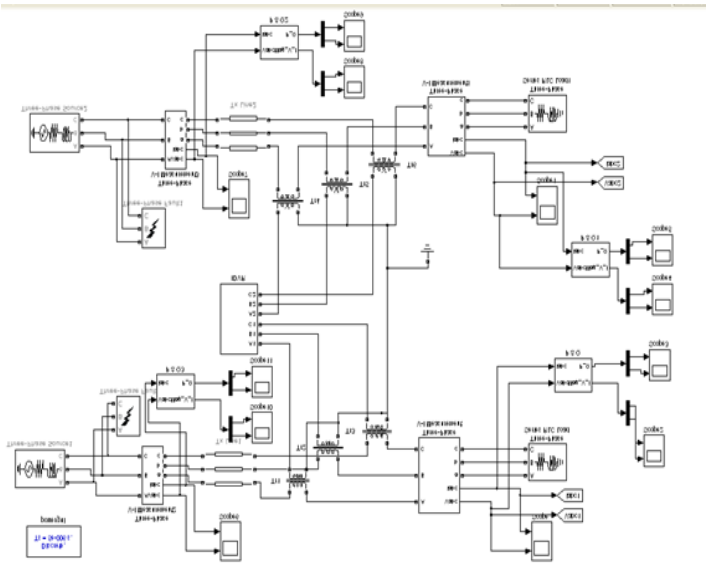
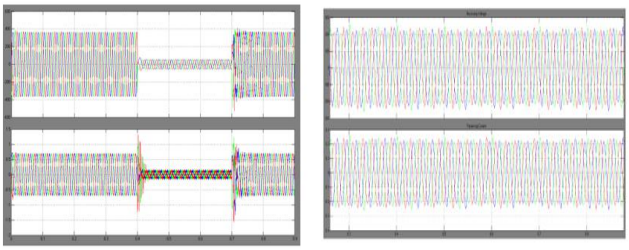
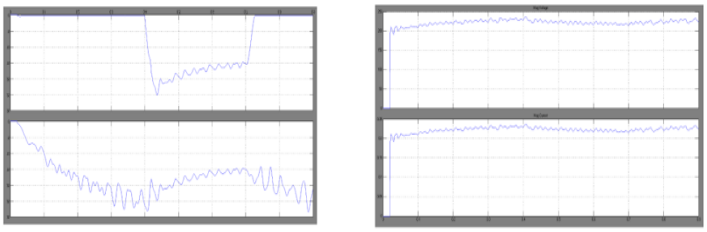


Fig.3.1. Simulation circuit of IDVR.



(a) At faulty condition (b)at IDVR condition

Fig.3.2 GRID VOLTAGE AND CURRENT IN TRANSMISSION LINE1



(a) (b)

Fig.3.3 REAL AND REACTIVE POWER (a) AT FAULTY CONDITION (b) AFTER INJECTION IDVR IN LINE1

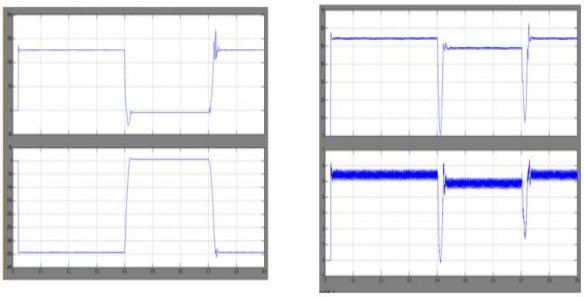


Fig 3.4 REAL AND REACTIVE POWER AT FAULTY CONDITION AFTER INJECTION IDVR

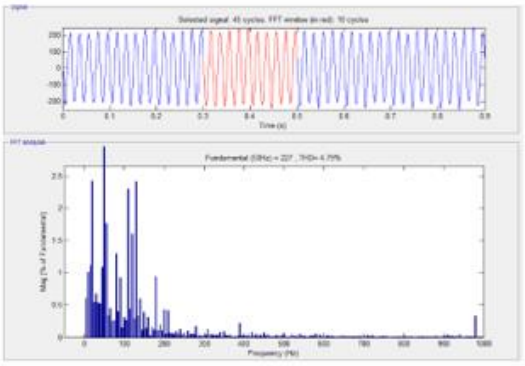


Fig 3.4 :HARMONIC (THD) REDUCTION IN LINE1 AFTER INJECTION

4. HARDWARE

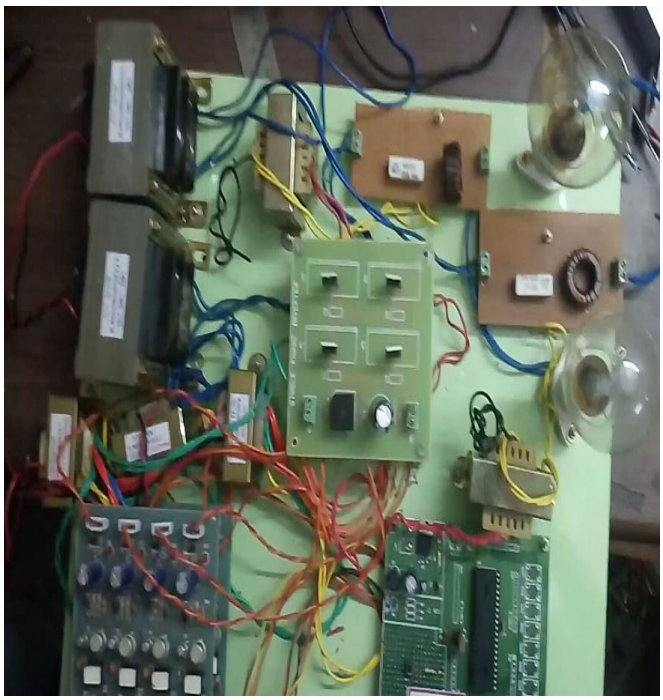


Fig 4.1 : hardware of IDVR

5. CONCLUSIONS

In this paper an enhanced sag compensation scheme is proposed for IDVR. The proposed strategy improves the voltage quality of sensitive loads by protecting them against the voltage sags involving the phase angle jump. It also increases sag compensation time by operating in minimum active power mode through a controlled transition once the phase angle jump is compensated. To illustrate the effectiveness of the proposed method an analytical comparison is carried out with the existing phase jump compensation schemes. It is shown that sag compensation time can be extended from 10 to 25 cycles (considering presag injection as the reference method) for the designed limit of 50% sag depth with 450 phase jump. Further extension in compensation time can be achieved for intermediate sag depths. This extended compensation time can be seen as considerable reduction in dc link capacitor size (for the studied case more than 50%) for the new installation. The effectiveness of the proposed method is evaluated through extensive simulations in MATLAB/Simulink and validated on a scaled lab prototype experimentally. The experimental results demonstrate the feasibility of the proposed phase jump compensation method for practical applications.

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