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DESIGN OF LOW POWER HIGH GAIN OPERATIONAL AMPLIFIER USING GDI TECHNIQUE

Sowmiya.M[1], Prabakaran.A.P[2]

[1]*P.G Student, Dept. of ECE, A.V.C College of Engineering,*
[2]*Associate Professor, Dept. of ECE, A.V.C College of Engineering,*

Abstract - *A novel technique of designing a low power high gain instrumentation amplifier for biomedical applications.The trend towards implementing systems with low supply voltages has created a challenging task in the design of VLSI analog circuits. The design of a low-power, high-gain and highly stable amplifier for bio-medical applications. Low powerdissipation, high-gain are achieved Apart from technological modifications, developing new circuit structures which avoidstacking too many transistors between the supply rails are preferable for low-voltage operation, especially if they do notincrease the circuit complexity.*

Key Words:

1. INTRODUCTION

Biomedical signal processing aims at fetching useful information from biomedical signals. Earlier the primary focus was on processing the biomedical signal to extract the original signal and remove noise. Detecting biomedical signals is a very challenging task as these signals normally consists of very weak amplitude in the order of few mV with almost equivalent noise signal levels. These signals also have a very low frequency range usually below 1KHZ. With the growth of microelectronics and embedded design more and more applications require very weak amplitude signal detection and measurement. These weak amplitude biomedical signals need to be suitably amplified along with rejection of noise. To overcome this problem instrumentation amplifiers are used to suppress any unwanted noise or the common mode signals that affects the original signal and also provide proper amplification to the desired signal. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology. CMOS Op-amp can be used efficiently for practical consequences for example designing of a switched capacitor filter, analog to digital converter etc. In this case the designs of the individual op amps are combined with feedback and by various parameters that affect the amplifier such as input capacitance, output resistance.

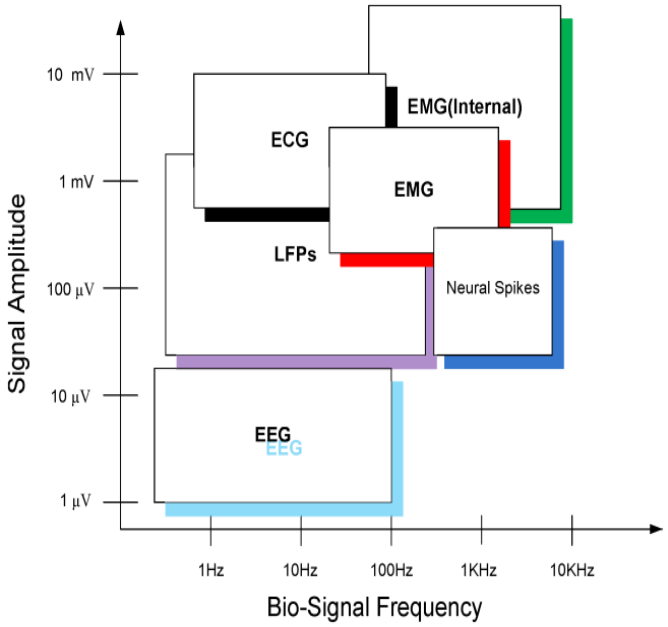

FIG-1: Biomedical signals

2. LITERATURE REVIEW

2.1A PROGRAMMABLE 1.5 V CMOS CLASS-AB OPERATIONAL AMPLIFIER WITH HYBRID NESTED MILLER COMPENSATION FOR 120 DB GAIN AND 6 MHZ UGF

The paper presents a rail-to-rail class-AB operational amplifier in a standard Vth =0.6 V CMOS technology operating at 1.5 V. A hybrid nested Miller compensation technique yields 6 MHz unity gain frequency at 300 p A supply current, 120 dB gain and programmability. Operation down to 1.0 V at 15.A is possible with 400 kHz UGF. The die area of the chip is 0.05 mm2 (70 mil').The design of ultimate low voltage CMOS op Amp topologies requires frequency compensation methods that are suited for a cascade of inverting gain stages. Hybrid Nested Miller compensation and multipath hybrid nested Miller compensation meet that demand, whereas traditional methods fails. Employing these new techniques, a four stage CMOS op Amp with a gain of 120 dB and a unity gain frequency of 6 MHz is demonstrated

2.2 INTEGRATED CIRCUITS AND ELECTRODE INTERFACES FOR NONINVASIVE PHYSIOLOGICAL MONITORING

This paper presents a systematic approach to instrumentation amplifier (IA) design using CMOS transistors operating in weak inversion is shown to offer high energy and noise efficiency. Practical methodologies to obviate 1/f noise, counteract electrode offset drift, improve common-mode rejection ratio, and obtain sub-Hertz high-pass cutoff are illustrated with a survey of the state-of-Theart IAs. From these interface considerations, we developed system requirements for reliable signal acquisition in bio potential, electrode–tissue impedance, and spectro photo metric measurements. Some of the main techniques for implementing CMOS sub threshold integrated instrumentation amplifiers in a low-noise and power-efficient manner were covered: pseudo resistors, chopping, driven right-leg circuits, impedance bootstrapping, and application-specific design for electrode–tissue impedance measurements and photo plethysmography.

3. PROPOPSED SYSTEM

The first stage of an op-amp is a differential amplifier stage. Differential Amplifier having two inputs and the difference of these two inputs will be amplified. The first stage provides the maximum gain of an op-amp. The second stage is a common source stage. The compensation capacitance (CC) is placed between first stage and second stage. The compensation capacitance (CC) provides the stability to the op-amp. The compensation capacitance (CC) increase the phase margin of the design and for a stable system the phase margin is should be greater than 450. The second stage increases the gain of the op-amp and converts the second stage input voltage into the current. The second stage is nothing more than the current sink inverter. The second stage is a common source stage which increases the DC voltage gain and improve the output signal swing for a given power supply voltage. The second stage is followed by a buffer stage, which provides a lower the output resistance and maintains a large voltage swing. The buffer stage also provides better slew rate (SR) of an Op-Amp. It is not necessary all applications require low output impedance. If the Op-Amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. The Biasing current is used to provide to keep all the transistors in saturation region. The purpose of the compensation circuit or compensation capacitance is to reduce the overall gain at higher frequencies and provides stability when negative feedback is applied to the Op-Amp.

3.1 Simulation

Simulation tool for simulating Op-amp design. Advanced features like Cadence Virtuoso Schematic Editor for providing high speed and easy design methods, Cadence Virtuoso Layout Suite for speeding up the physical layout of the design, Cadence Virtuoso Visualization and Analysis for efficiently analyzing the performance of the design and Cadence Assura Physical Verification for reducing overall verification time, because a quick and instinctive debug capability is incorporated within the Virtuoso custom design environment. It easily compares, repair, remove and distinguish errors.

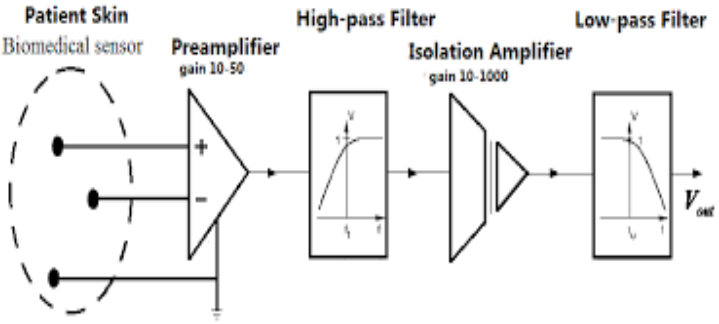

Fig-2: High power to low power

4. SIMULATION RESULT

Designing of op-amp The Op-Amp design process mainly involves the two major steps. First one is called Design conception while another one is termed as Design optimization. Architecture is proposed to meet the given specifications in design conception. This step is usually done to calculate the design values by hand calculations which are necessary for choices that must be made. The “first-cut” design is taken & verified for the specifications and then optimized in the second step of the design optimization. The optimization can include different environmental influences or process variations and is usually done by using Computer simulation.

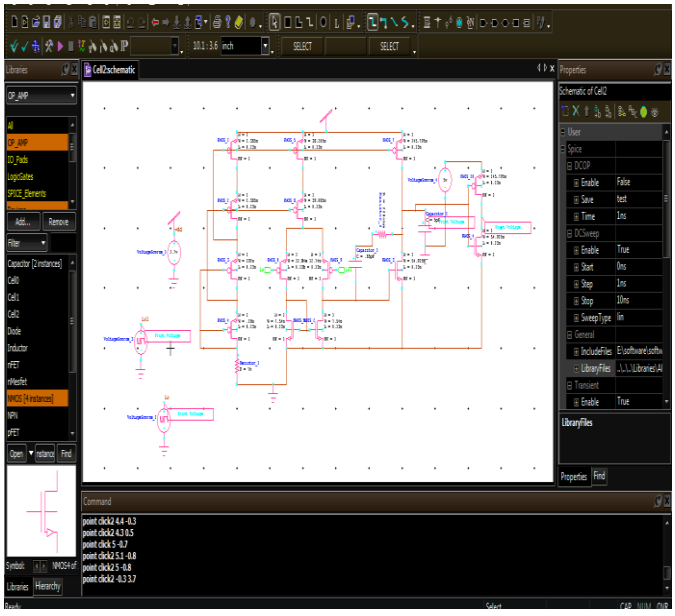

Fig-3: Cell2 S -Edit design

5. OUTPUT WAVEFORM OF S EDIT

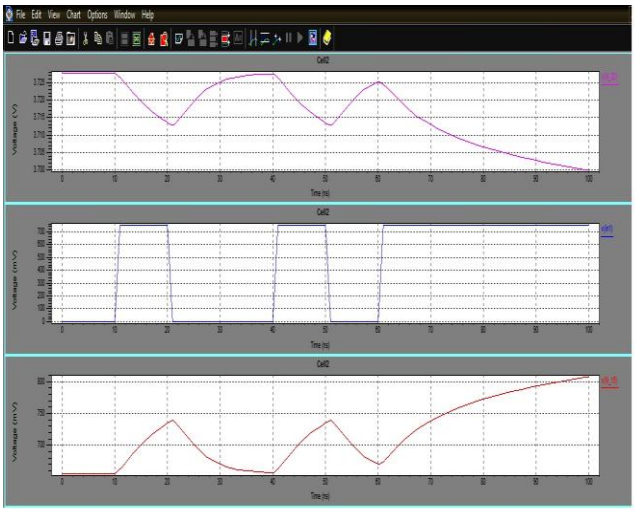

Fig-4: output wave form S Edit design

5.1 L EDIT DESIGN

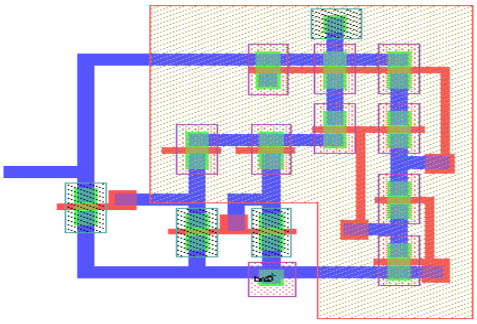

Fig-5: L Edit

5.2 L EDIT OUTPUT WAVEFORM

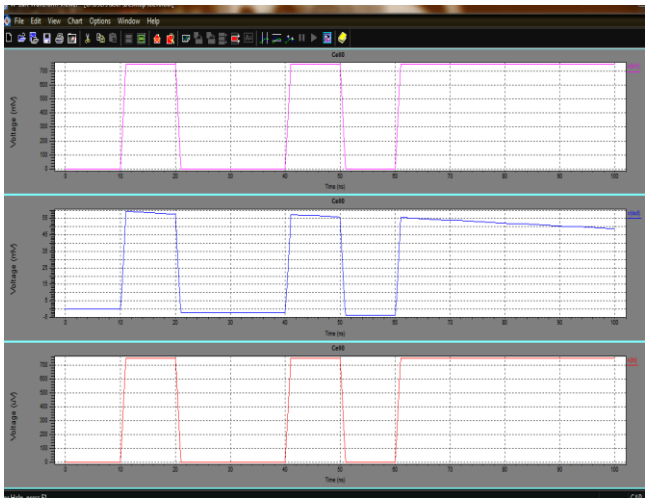

Fig-5: output waveform L-Edit design

6. CONCLUSION

Proposed a 2 stage CMOS op-amp and analyzed its behavior. Simulation results confirm that the proposed design procedure can be utilized to design op-amps that meet all the required specifications. The simulation is done with Tspice software. The design is on 0.18µm technology. The unit gain bandwidth achieved for the design is 8MHz, the gain is 70db and phase margin is of 75degree to ensure a good stability. The total power consumed is Average power consumed -> 1.401808e-003 watts.

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