

A Comparative Study of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology for Industrial Drive

Aparna Prayag¹, Sanjay Bodkhe²

¹Research Scholar, Electrical Engg. Department, G. H. Rasoni college of Engg, Nagpur, India

² Former Professor, Electrical Engg. Department, G.H. Rasoni college of Engg, Nagpur, India

Abstract - In recent years multilevel inverter technology has become popular for medium and high power industrial applications. There are three main multilevel inverter topologies-Neutral Point Clamped, Flying Capacitor and Cascaded H Bridge. Cascaded H Bridge has become famous because of its modular design, simple control, reliability, availability and the absence of capacitor imbalance problem. In this paper we are focusing on this topology which is series connection of several H-Bridge cells with equal and un-equal magnitude of dc sources known as symmetrical and asymmetrical structure. Here symmetrical, binary asymmetrical and trinary asymmetrical topologies (formed by cascading two H-bridge cells) fed induction motor drives are compared in order to find an optimum arrangement with high quality output voltage. Performance of these structures is verified through computer simulation using MATLAB/Simulink.

Key Words: Multilevel inverter, symmetrical, asymmetrical, Cascaded H Bridge, Total harmonic distortion (THD).

1. INTRODUCTION

High performance a.c drive systems require high quality inverter output with low harmonic contents. Conventional two level inverters require high switching frequency to obtain a quality output voltage waveform. In high power and high voltage applications, these two level inverters, have some limitations in operating at high frequency. Harmonic reduction by raising switching frequency of two level inverter is difficult. From this aspect Multilevel (begins with three level) approach is promising alternative.

The main conception of multilevel inverter (MLI) is to achieve higher power by using number of power switches with several low voltage dc sources. It can produce output voltage waveform in steps which is closer to sine wave and reduces total harmonic distortion. Important points regarding topological structure of multilevel inverter are:

- It should have less switching devices as far as possible.
- It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.
- Each switching device should have lower switching frequency owing to multilevel approach.

Recently multilevel inverters have been used in various industrial applications like distributed generation, adjustable speed drives, flexible ac transmission system,, HVDC, electrical vehicles etc. due to noticeable advantages like high quality output voltage using low switching frequency, low harmonic contents, low electromagnetic interference, less voltage stress on power switches, more efficiency and low dv/dt stress on load [1]-[9].

Improvement in these advantages is possible by increasing number of levels of output voltage waveform but it requires large number of switches that makes circuit complex. It also raises cost and size of the circuit.

2. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded H Bridge multilevel inverter is also known as multi-cell inverter. It consists of series connected H-bridges. In the topology each H-bridge is supplied by isolated dc source of identical value on its dc side and connected in series on their ac side. Batteries, fuel cells or ultra-capacitors are used as isolated dc sources [10]. The total output voltage is attained by adding voltages produced by each H-bridge connected to form cascaded circuit. Each cell creates three voltage levels positive, zero and negative by linking dc source to ac output through various arrangements of the four switches used in it.

Fig.1 presents single phase structure of CHB-MLI using two H bridges. An output voltage waveform is obtained by summing the output voltage of both the cells connected in series.

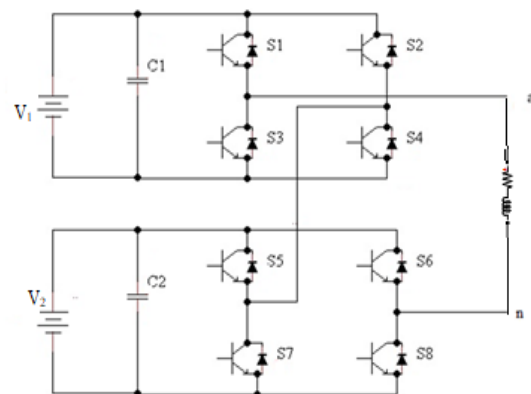


Fig -1: Single phase leg of CHB

If m numbers of H-bridges are joined in series then total voltage across the load is

$$(V_{an}) = (V_o)_1 + (V_o)_2 + \dots + (V_o)_m$$

$$(V_{an}) = \sum_{k=1}^m (V_o)_m \quad (1)$$

2.1 Symmetrical Cascaded H-Bridge Inverter

When each cell of CHB-MLI is supplied by same magnitude of dc source then this structure is known as symmetrical structure.

The magnitude of dc source is given as

$$V_k = Vdc$$

$$k = 1, 2, \dots, m. \quad (2)$$

$$V_1 = V_2 = \dots = V_m = Vdc$$

The total number of output voltage levels n in symmetric multilevel inverter is given by

$$n = 2m + 1 \quad (3)$$

Where n is number of power cells used for cascade structure The maximum voltage generated by this arrangement is

$$V_M = m \times Vdc \quad (4)$$

For instance, if $m=2$ as shown in Fig. 1 it generates 5 level voltage with maximum voltage 2Vdc.

2.2 Asymmetrical Cascaded H-Bridge Inverter

Asymmetrical multilevel inverters help to produce more number of output levels without increasing the number of cells. The magnitude of dc voltages sources can be selected according to a geometric progression with a factor of 2 or 3 [11].

If dc voltage sources are in the ratio of 1:2, then the inverter is known as binary asymmetric multilevel inverter. The value of each dc source can be calculated as

$$V_k = 2^{(k-1)} Vdc$$

$$k = 1, 2, \dots, m. \quad (5)$$

The effective number of output voltage levels n and maximum voltage generated can be expressed as

$$n = 2^{(m+1)} - 1 \quad (6)$$

$$V_M = (2^m - 1)Vdc \quad (7)$$

For two H-bridge cascaded topology this structure generates 7 levels with maximum value 3Vdc.

If dc voltage sources are in the ratio of 1:3, then the inverter is known as trinary asymmetric multilevel inverter. The value of each dc source can be calculated as

$$V_k = 3^{(k-1)} Vdc$$

$$k = 1, 2, \dots, m. \quad (8)$$

In this case number of voltage levels and maximum voltage generated can be calculated as

$$n = 3^m \quad (9)$$

$$V_M = \frac{(3^m - 1)}{2} Vdc \quad (10)$$

Now, for two H-bridge cascaded topology this structure generates 9 levels with maximum voltage 4Vdc.

All these points of asymmetrical inverter are summarized in table1.

Table -1: Asymmetrical CHB-MLI

| Binary Asymmetric CHB-MLI | Trinary Asymmetric CHB-MLI |
|--|--|
| Voltage sources are in the ratio 1:2 | Voltage sources are in the ratio 1:3 |
| Value of dc voltage source $V_k = 2^{(k-1)} Vdc$ $k = 1, 2, \dots, m.$ | Value of dc voltage source $V_k = 3^{(k-1)} Vdc$ $k = 1, 2, \dots, m.$ |
| No. of output voltage levels $n = 2^{(m+1)} - 1$ | No. of output voltage levels $n = 3^m$ |
| Maximum voltage generated. $V_M = (2^m - 1)Vdc$ | Maximum voltage generated. $V_M = \frac{(3^m - 1)}{2} Vdc$ |

3. COMPARISON BETWEEN SYMMERICAL AND ASYMMERICAL CASCADED H BRIDGE MULTILEVEL INVERTER

From above discussion it is seen that trinary asymmetrical multilevel inverter can produce more voltage levels and higher maximum output voltage with the same number of bridges as compared to symmetrical and binary asymmetrical structure. Table 2 presents comparison based on the number of levels (n), number of switches (N_s), dc sources (N_d) maximum output voltages (V_M) and number of variety in voltage magnitudes (N_v), total voltage blocked by switches (V_b) when m number of cells are connected in series.

Table -2: Comparison of Symmetrical and Asymmetrical CHB-MLI

| Parameters | Symmetrical Structure | Asymmetrical Structure | |
|------------|-----------------------|------------------------|------------------------------|
| | | Binary | Trinary |
| n | $2m + 1$ | $2^{(m+1)} - 1$ | 3^m |
| N_s | $4m$ | $4m$ | $4m$ |
| N_d | m | m | m |
| V_M | mV_{dc} | $(2^m - 1)V_{dc}$ | $\frac{(3^m - 1)}{2} V_{dc}$ |
| N_v | 1 | m | m |
| V_b | $4mV_{dc}$ | $4(2^m - 1)V_{dc}$ | $2(3^m - 1)V_{dc}$ |

Chart 1 compares number of switches required to generate specific number of output voltage levels and Chart 2 shows number of dc sources required for the three configurations. It is clear that trinary asymmetrical configuration needs less components

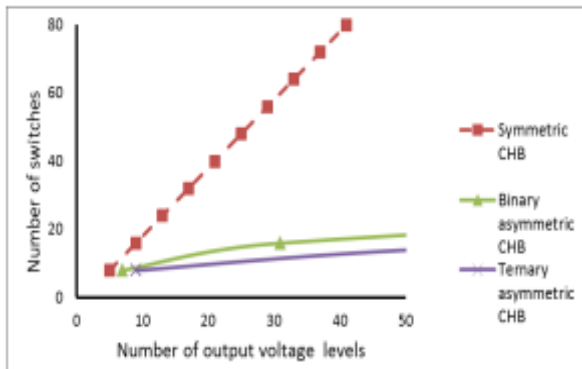


Chart -1: Number of switches vs number of output voltage levels

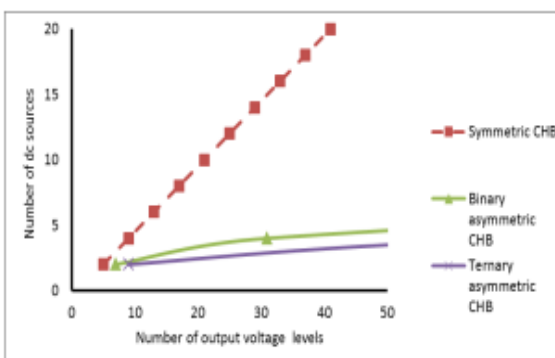


Chart -2: Number of dc sources vs number of output voltage levels

4. SIMULATION STUDY

The three phase symmetrical, binary asymmetrical and trinary asymmetrical cascaded H-bridge multilevel inverters fed three phase induction motor are modelled in MATLAB/Simulink environment. In each model configuration

two H –bridges are used, so that number of switches and number of dc sources in all the models are same. The switches used in the simulations are assumed to be ideal. Separate dc sources are used in the simulation studies. In practice these dc voltage sources are available via distributed energy resources like photovoltaic panels, fuel cells and ultra-capacitors. If the available source is an ac source then the required dc voltage sources can be obtained by using rectifiers.

A multicarrier level shifted phase disposition PWM scheme is used in this paper to generate pulses for the switches of CHB-MLI. The conventional sinusoidal PWM technique can be applied to multilevel inverter topologies by using multiple carriers. Therefore it is known as multi-carrier PWM technique. A sinusoidal reference waveform of fundamental frequency is compared with high frequency carrier waveforms having same amplitude. For m level inverter ($m-1$) carriers are required [12].

Simulation parameters used are given in Table 3 and results are shown from Fig. 2 to Fig.16. Comparison is given in Table 4.

Table -3: Simulation Parameters

| Description | Parameter | Value |
|------------------------------|---------------|-------------|
| Symmetric inverter | V1 | 160.5 volts |
| | V2 | 160.5 volts |
| Binary asymmetric inverter | V1 | 214 volts |
| | V2 | 107 volts |
| Trinary asymmetric inverter | V1 | 180 volts |
| | V2 | 60 volts |
| Load-3 Phase Induction Motor | Rated voltage | 400 volt |
| | Rated current | 10 amp |
| | Rated power | 5.4 H.P |
| | Rated speed | 1430 rpm |
| | Rated torque | 2.9 N-m |

4.1 Simulation Results Of Symmetric CHB 5-Level Inverter

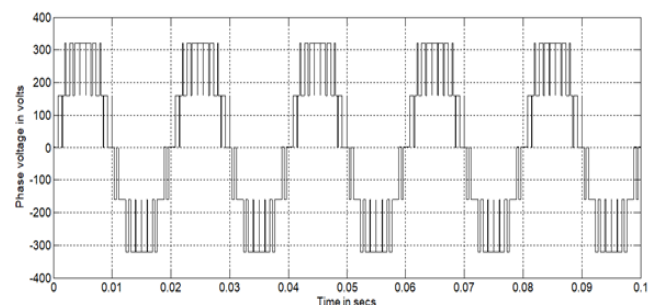


Fig -2: Phase Voltage (V_A) Waveform

4.2 Simulation Results Of Binary Asymmetric CHB 7-Level Inverter

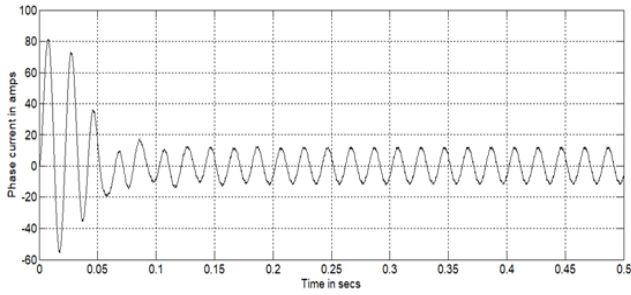


Fig -3: Phase Current (I_A) Waveform

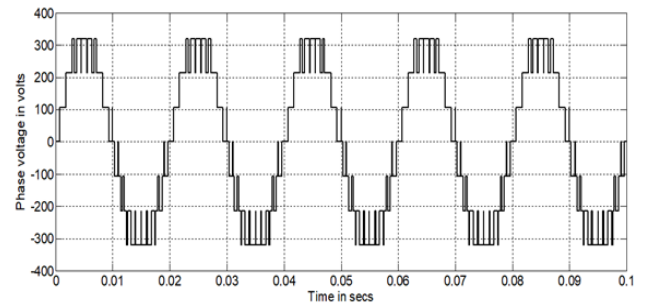


Fig -7: Phase Voltage (V_A) Waveform

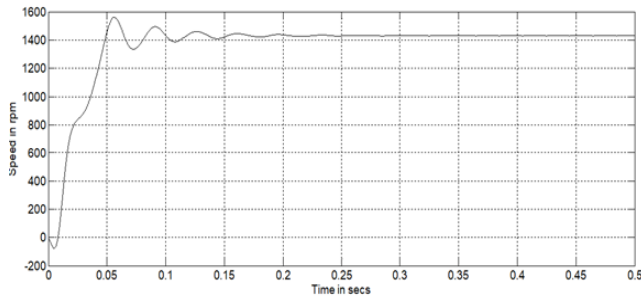


Fig -4: Rotor Speed

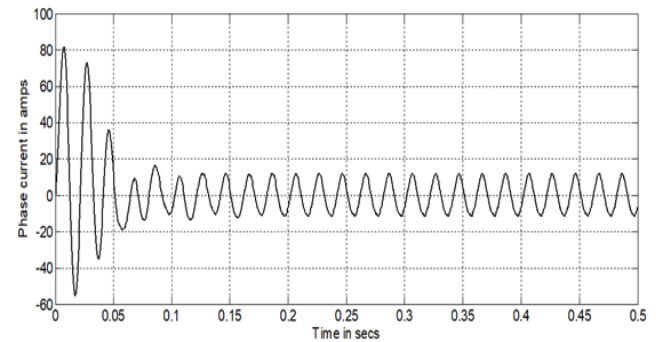


Fig -8: Phase Current (I_A) Waveform

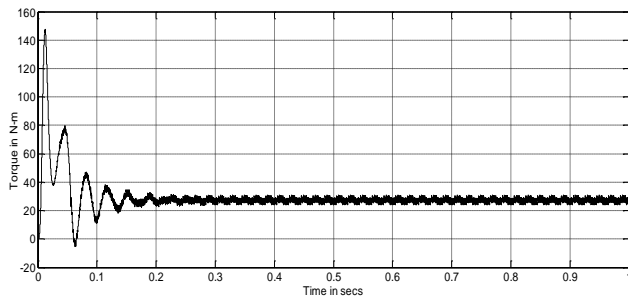


Fig -5: Electromagnetic Torque

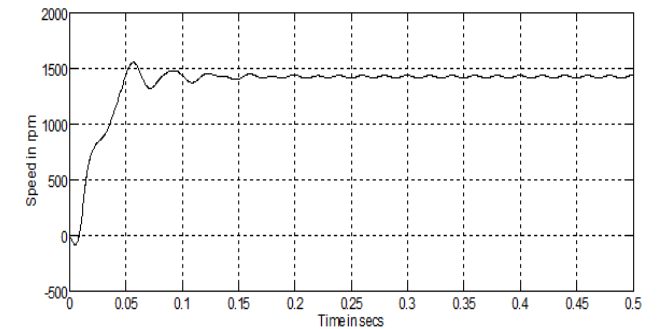


Fig -9: Rotor Speed

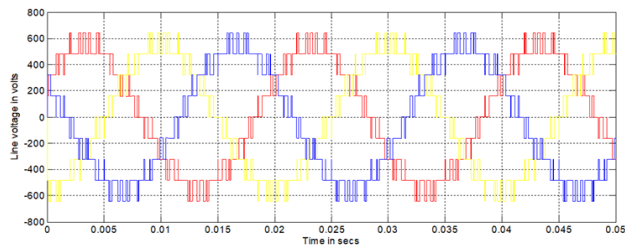


Fig -6: Line voltages and Harmonic Spectrum of Voltage V_{AB}

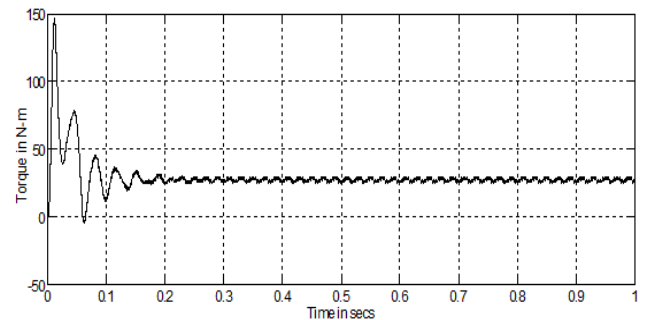


Fig -10: Electromagnetic Torque

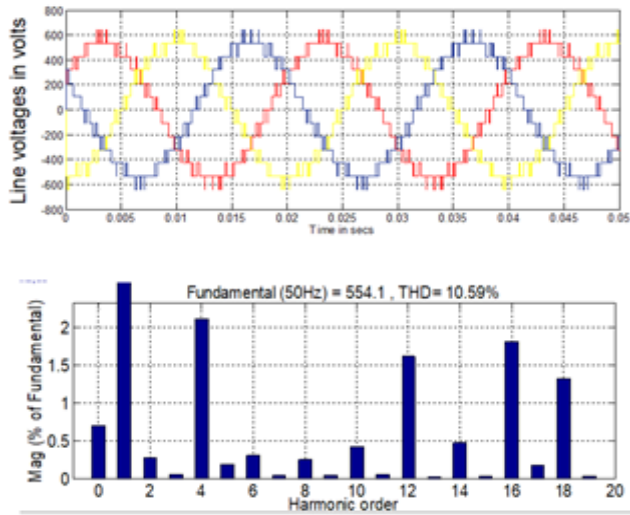


Fig -11: Line voltages and Harmonic Spectrum of Voltage V_{AB}

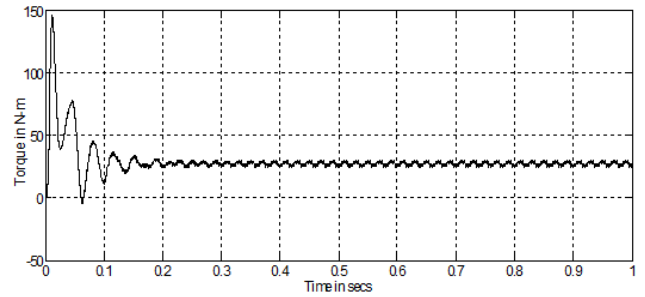


Fig -15: Electromagnetic Torque

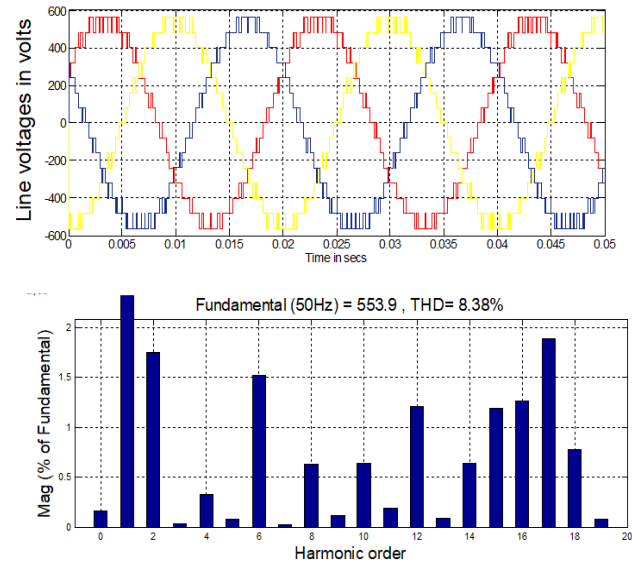


Fig -16: Line voltages and Harmonic Spectrum of Voltage V_{AB}

4.3 Simulation Results Of Trinary Asymmetric CHB 9-Level Inverter

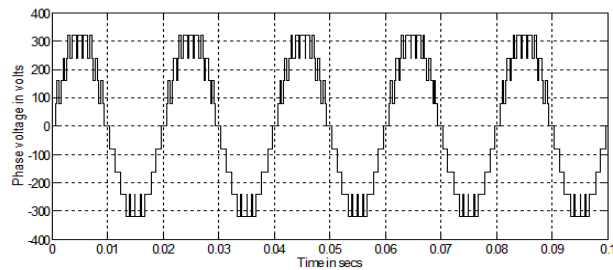


Fig -12: Phase Voltage (V_A) Waveform

Table -4: Comparison of Performance Parameters of Symmetric and Asymmetric CHB Inverter

| Parameters | Symmetric inverter | Asymmetric inverter | |
|-----------------------|--------------------|---------------------|--------------------|
| | | Binary asymmetric | Trinary asymmetric |
| Number of dc sources | 2 | 2 | 2 |
| Number of switches | 8 | 8 | 8 |
| Fundamental Frequency | 50 Hz | 50 Hz | 50 Hz |
| Carrier frequency | 1 kHz | 1 kHz | 1 kHz |
| Voltage levels | 5 | 7 | 9 |
| VL (volts) | 554.1 | 554.1 | 553.9 |
| Voltage THD (%) | 16.97 | 10.59 | 8.38 |

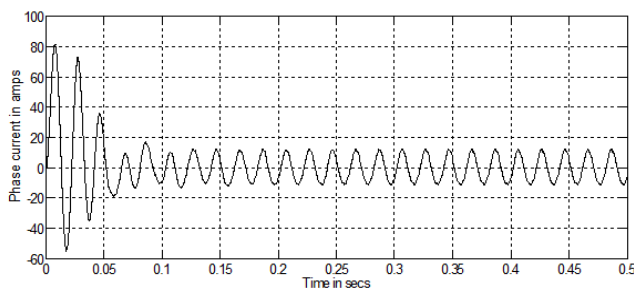


Fig -13: Phase Current (I_A) Waveform

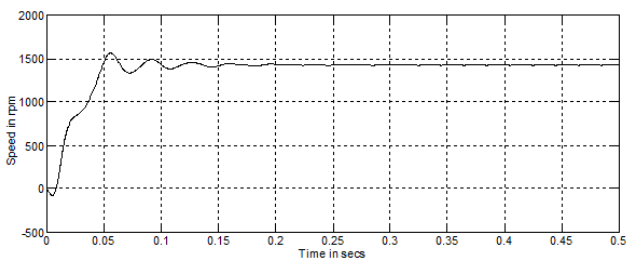


Fig -14: Rotor Speed

5. CONCLUSIONS

In this paper the comparison of symmetrical, binary asymmetrical and trinary asymmetrical CHB-MLI with two H-bridges in series fed induction motor is carried out. MATLAB/Simulink models are developed for all the three topologies. Using PD-PWM a pulse generation circuit is designed.

From simulation results it is observed that the generated voltage spectrum is very much improved for nine level inverter topology. Among three configurations trinary- CHB inverter requires least number of switches and dc sources and generates high quality voltage with minimum harmonics.

Using this configuration motor performance is better. It is clear from simulation waveform that the output current waveform is smoother. The currents fluctuate up to 0.1 sec and after that it reaches a constant value. The extreme high value of current at the starting points of the simulation is due to the fact that before the rotor gains any speed, the stator acts as a very high power load. The fluctuations in the current values die out at about 0.15 sec and the currents attain a fairly constant value to reach its full speed of 1430 rpm.

The electromagnetic torque characteristic of the induction motor supplied by three phase asymmetrical nine level inverter shows that at the starting instant, the torque has an oscillating characteristic. A nearly constant electromagnetic torque is obtained after a time of 0.15 sec.

It is observed that as the stator currents settle to a constant value the electromagnetic torque also attains a fairly constant value. Torque achieves a mean value of about 26.9 N-m at steady state

CHB inverter requires least number of switches and dc sources and generates high quality voltage with minimum harmonics.

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