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# Performance Evaluation of Controlled Inverter Using Quantum Dot Cellular Automata (QCA)

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**Abstract –** *Quantum Dot Cellular Automata is one of the emerging field in the branch of nanotechnology which helps to overcome the limitation of conventional transistor based CMOS technology like excessive power dissipation, short channel effects etc. in the nano domain. This paper demonstrates the design and layout of novel controlled inverter using majority gate based on Quantum Dot Cellular Automata with minimum complexity in comparisons to previous designs. The stability of the circuit has been determined by calculating the kink energy. The simulation results are captured and verified using QCA Designer tool.*

**Keywords**- QCA, Majority gate, QCA designer.

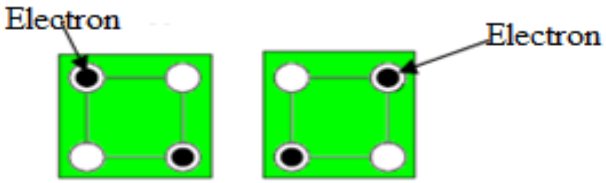
## 1. INTRODUCTION

Shrinking transistor size has been the major issue to achieve low power dissipation, high device density and high speed in today's technology. But the scaling of transistor in the nano regime suffers several obstacles like excessive power dissipation, short channel effects etc. Quantum Dot Cellular Automata is an approach of computing information with quantum dots as an alternative of CMOS technology. Conventional CMOS based transistor technology transfers information by the change of voltage or current whereas QCA transfers information by changing its polarisation state. Quantum Dot Cellular Automata do not use transistors. A quantum cell is the basic element of QCA. Information is encoded in a QCA cell by changing the charge configuration within a cell. Quantum Dot Cellular Automata is projected as an emerging nanotechnology to build IC's as an alternative of conventional CMOS technology. The advantages of QCA technology includes smaller circuit size, low power dissipation and high speed computing.

## 2. QCA BACKGROUND

### 2.1. QCA Cell

The fundamental unit of QCA is a cell. Each cell contains four quantum dots arranged in a square pattern. Dots are the places where electrons can sit. The quantum dots contain mobile electrons which quantum mechanically tunnel between dots within a cell but not outside the cell. If a cell is charged with two excess electrons, each try to occupy the furthest possible site with respect to each other due to columbic interaction. Therefore, two different cell sates exists. The state of a cell is called its polarisation denoted by P. The state P=-1 is used to represent logic '0' and state P=+1 is used to represent logic '1'.The following fig shows the two possible minimum energy states of a quantum cell.




Polarisation=-1 Binary '0'  Polarisation=+1 Binary '1'

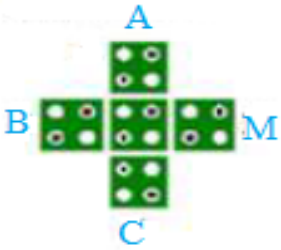
Fig1. Shows the schematic of a quantum cell.

A Polarisation P is defined by :-

$$P=\frac{(p_1+p_3)-(p_2+p_4)}{p_1+p_2+p_3+p_4}$$

### 2.2. Majority Gate

Five QCA cells are required to build a three input majority gate. Two of them are used as input and one is used as a fixed polarisation. By changing the value of polarisation we can built AND or OR gate. The following fig 2 shows the generalised structure of majority gate



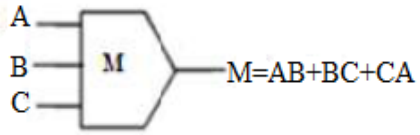
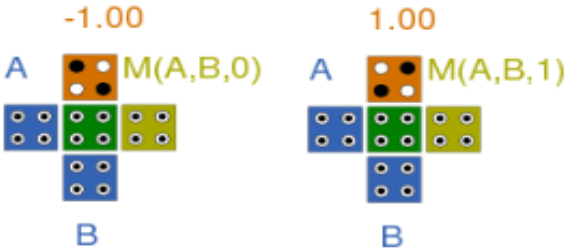



Fig 2.Structure of Majority gate

The general expression of majority gate is

M (A, B, C)=AB+BC+CA




(a) (b)

Fig3. (a) 2 input AND gate (b)2 input OR gate

By assigning the value of C as 0 we can construct a AND gate

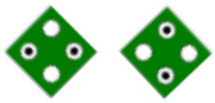
M(A,B,0)=A.B

By assigning the value of C as 1 we can construct a OR gate.

M(A,B,1)=A+B

### 2.3. QCA WIRE

A QCA wire is used to transmit information from one place to another. There are mainly 2 types of QCA wire namely, 45 degree and 90 degree.



Logic '0' Logic '1'

Fig 4. 45 degree QCA wire

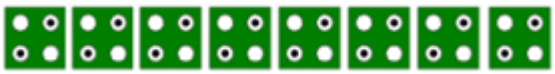


Fig 5. 90 degree QCA wire

### 2.4. QCA Clocking

Clocking is used to push the information from one cell to the next cell. Clocking leads to adjustment of tunnelling barriers between quantum dots for transfer of electrons between dots by application of an appropriate of an appropriate voltage to a cell. There are mainly four types of clocking namely, switch hold release and relax.

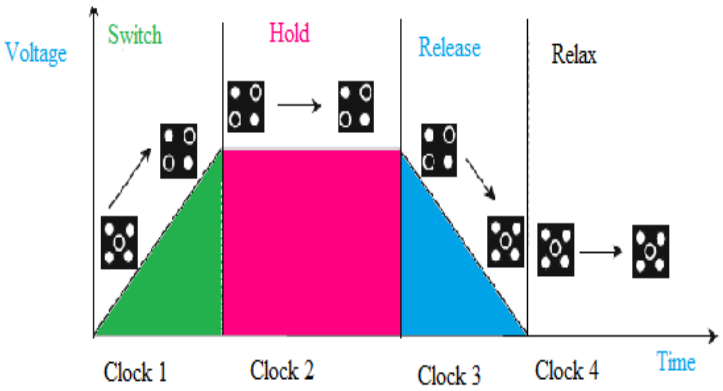



Fig6. Clocking of QCA

### 3. IMPLEMENTATION OF CONTROLLED INVERTER

A controlled inverter circuit is implemented using an Ex-OR gate, a logic variable can be complemented or allowed to pass through it unchanged. This is done by using one Ex-OR input as a control input and the other logic variable input. If the input bit is a 0, the output is , 0 XOR 1=1 and if the input is a 1, the output is ,1 XOR 1=0.When the control input is high , output Y =A and when control input is low, output Y=A. Thus ,we can say that an Ex-OR gate can be used as a controlled inverter, that is, one of the input can be used to decide whether the signal at the other input will be inverted or not. Here control input is B & logic variable input is A shown in fig 7 & 8.

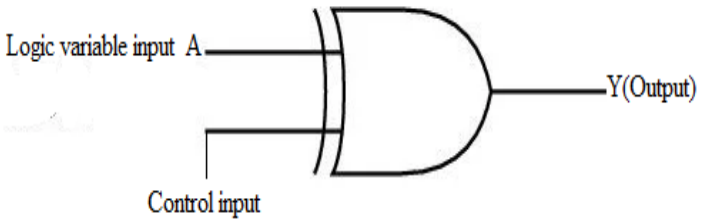



Fig 7. Schematic of controlled inverter using Ex-OR gate

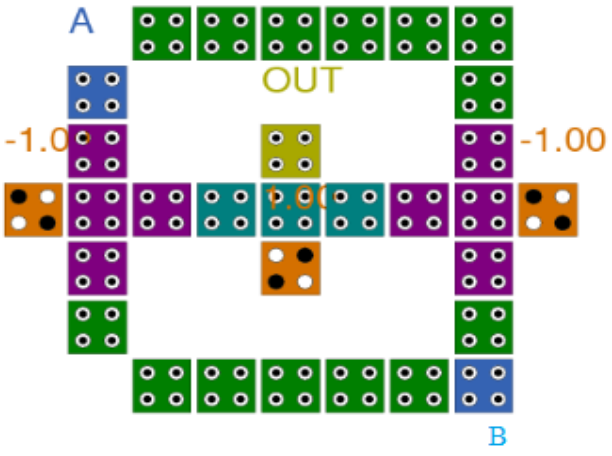



Fig 8.Layout of controlled inverter

## 4. COMPARISIONS

The table 1 shows the performance and analysis of proposed design with the previous QCA XOR design in terms of the cell count area and latency. The controlled inverter is built using Ex-OR gate having an area of 0.03 $um^2$.

| | CELL COUNT | AREA ($um^2$) | LATENCY |
|---|---|---|---|
| Conventional Design[4] | 74 | 0.11 | 1 |
| Conventional Design[5] | 67 | 0.07 | 2 |
| Proposed Design | 31 | 0.03 | 0.75 |

Table 1. Comparisons of QCA XOR gates

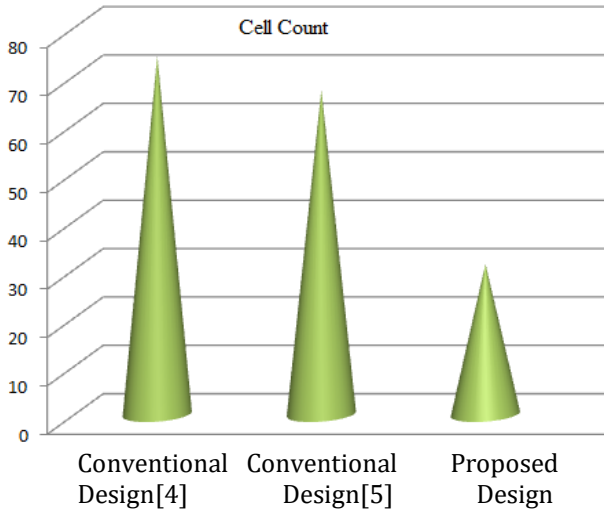



Fig 9. Cell comparison

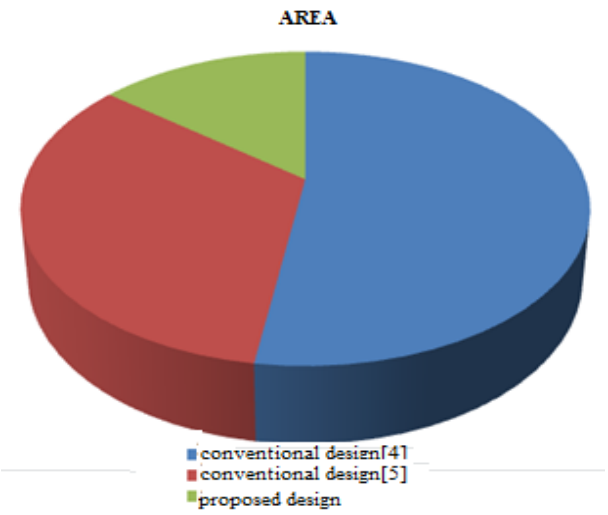



Fig 10. Area Comparison

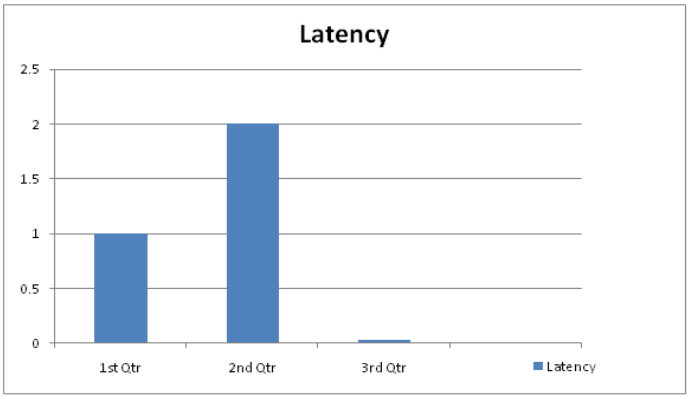



Fig 11. Latency Comparison

## 5. QCA DESIGNER TOOL & SIMULATION RESULTS

The proposed circuit in this paper have been verified using the QCA Designer tool with version 2.0.3.The default parameters for the coherence vector mode(Euler mode and Randomize Simulation Order) are:-

Temperature=1K
Relaxation Time=1.000000e-015 s
Time Step=1.000000e-016 s
Total Simulation time=7.000000e-011 s
Clock High=9.800000e-022 J
Clock Low=3.800000e-023 J
Clock Shift=0.000000e+000
Clock Amplitude factor=2.000000
Radius of effect=80.000000 nm
Relative permittivity=12.900000
Layer Separation=11.500000 nm

The main window screenshot of QCA Designer with coherence Simulation vector mode is shown in Fig 12.

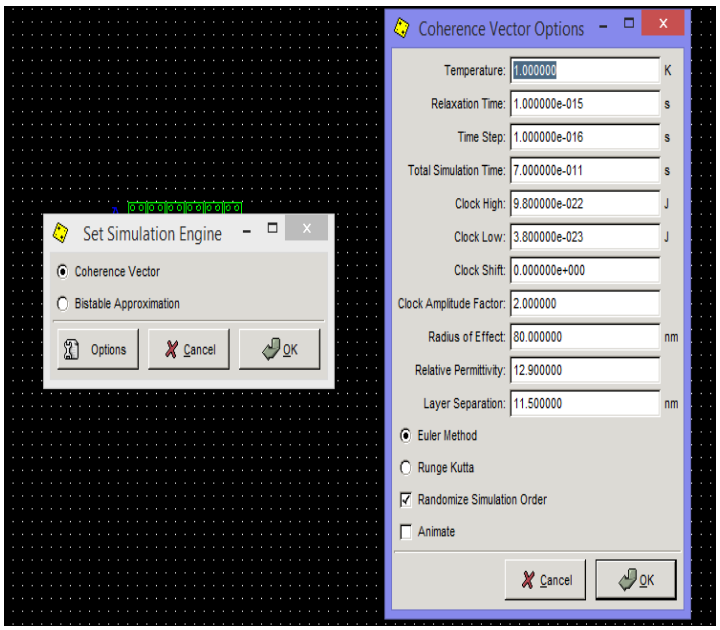



Fig 12. Main screenshot of QCA Designer

The controlled inverter is built using 31 cells having an area of 0.03 um$^2$.The number of cells is proportional to the area. Hence decreasing number of cells is relatively an improvement of area. The simulation results of the proposed controlled inverter are shown below in fig 13:-

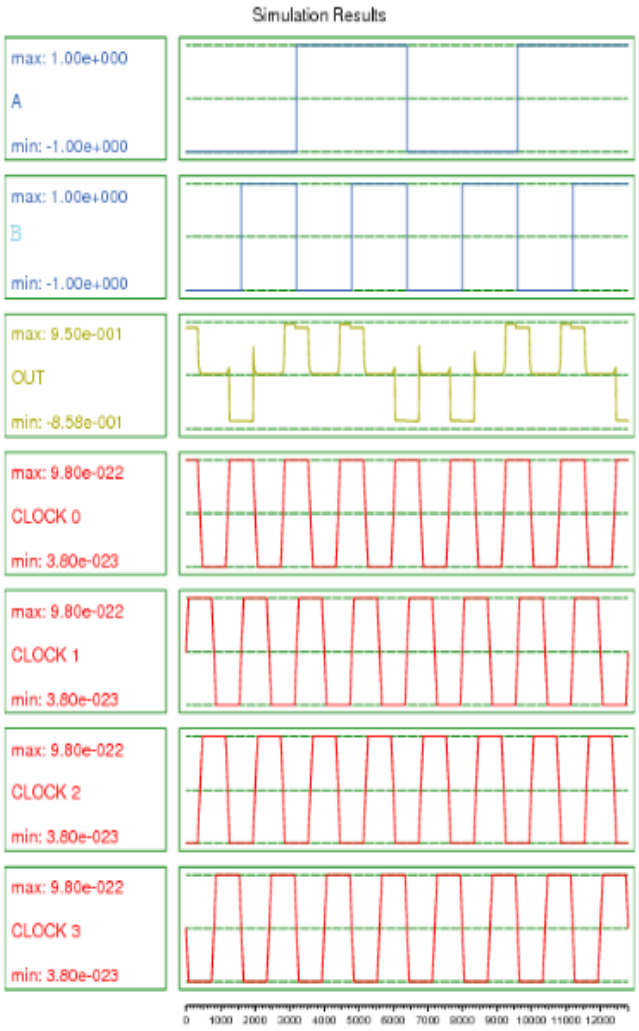



Fig 13. Simulation results of controlled inverter

## 6. CALCULATION OF KINK ENERGY

The kink energy is defined as the energy difference between two neighbouring or adjacent cells. Kink energy does not depend upon the temperature variation but depends upon the spacing between two neighbouring cells. To prove the robustness and stability of the design calculation of kink energy is very important. We have calculated the kink energy using the formula:-

$$U = K\frac{Q_1 \, X \, Q_2}{r}$$

Where U is the kink energy, $Q_1$ & $Q_2$ are the electronic charges , K is a constant given by
K= $K=1/4\pi\varepsilon_0\varepsilon_r=9 \times 10^9$ and r is the distance between them.

Therefore, $U=\frac{23.04 \times 10^{-29}}{r}$ J

For this calculation, all the cells have been assumed identical and square shaped whose each side having length 18 nm. Interspacing distance between the cells is equal to 2 nm.

The kink energy of the output cells of the controlled inverter is shown in the following fig 14.

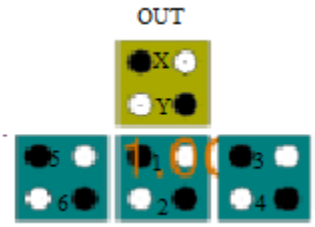



Fig 14. Kink energy calculation for output cells.

| **Calculation of Kink energy for electron 'x'** | **Calculation of Kink energy for electron 'y'** |
|---|---|
| U1=23.04 X $10^{-29}$)/(20 X $10^{-9}$)<br>=1.152 X $10^{-20}$ J | U1=(23.04 $10^{-29}$)/(18.11 X $10^{-9}$)<br>=1.27 X $10^{-20}$ J |
| U2=(23.04X$10^{-29}$)/(42.04 X $10^{-9}$)<br>=0.548 X $10^{-9}$ J<br>U3=(23.04X$10^{-29}$)/(28.28 X $10^{-9}$)<br>=.814 X 10 J | U2=(23.04X10-$^{29}$)/(26.90 X $10^{-9}$)<br>=0.856 X $10^{-9}$ J<br>U3=(23.04X $10^{-29}$)/(2.8 X $10^{-9}$)<br>=8.2 X $10^{-9}$ J |
| U4=(23.04X$10^{-29}$)/(53.74 X $10^{-9}$)<br>=0.428 X $10^{-9}$ J | U4=(23.04X$10^{-29}$)/(28.28 X $10^{-9}$)<br>=0.8147 X $10^{-9}$ J |
| U5=(23.04X$10^{-29}$)/(28.28 X $10^{-9}$)<br>=0.8147 X $10^{-9}$ J | U5=(23.04X$10^{-29}$)/(38.05 X $10^{-9}$)<br>=0.605 X $10^{-9}$ J |
| U6=(23.04X$10^{-29}$)/(38.05 X $10^{-9}$)<br>=0.605 X $10^{-9}$ J | U6=(23.04X$10^{-29}$)/(28.28 X $10^{-9}$)<br>=0.814 X $10^{-9}$ J |
| $U_{TOTAL}$=4.361 x $10^{-9}$ J | $U_{TOTAL}$=12.5 x $10^{-9}$ J |

## 7. CONCLUSION

In this paper, we have designed controlled inverter using Ex-OR gate. This is a new approach of designing controlled inverter with lesser QCA cells, less clock delays and reduced area which provides high device density, less hardware complexity and high speed computing. The simulation results have been captured and verified using the QCA Designer tool. The stability of the circuit has clearly been determined by calculating the kink energy.

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