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Accuracy configurable Adder

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Abstract - *Low power IC design uses approximate computing and has received research attention recently. Few accuracy configurable adder (ACA) designs have been developed to accommodate dynamic levels of approximation but these designs require large area overhead because of carry prediction and redundant computing. If error detection and correction circuitry is included larger area gets increased further. In this paper a simple ACA design without redundancy/correction circuitry is proposed and a very simple carry prediction is used. Here 16 bit adder is designed using simple accuracy reconfigurable adder (SARA) and DAR with SARA. The proposed technique DAR with SARA significantly improves accuracy-power-delay efficiency. Further simple RCA and SARA is used in Wallace multiplier delays are compared.*

Key Words: **Accuracy-configurable adder (ACA), approximate computing, delay-adaptive reconfiguration (DAR), low power design.**

1. INTRODUCTION

In advanced VLSI technologies power constraints are a well-known challenge. Low power techniques are already extensively studied. A new direction is approximate computing, where errors are intentionally allowed for power reduction. In audio, video, haptic processing, and machine learning in these applications small errors are indeed acceptable. Approximate computing research has been concentrated on arithmetic circuits. In computing hardware arithmetic circuits are necessary building blocks. Several approximate adder designs have been developed [1]-[3].

A few approximate designs have been developed to reduce the overall error by intentionally allowing errors in lower bits with shorter carry chain in addition operation. ACA starts with an approximate adder and it with an error detection and correction circuit. Its approximate adder contains significant redundancy, and the error detection/correction circuit further increases area overhead.

In this paper, we propose a new carry-prediction based accuracy configurable adder design: simple accuracy reconfigurable adder (SARA). It is a simple design with less area compared to error correction based configuration.

ACA designs can be generally categorized into two groups: error-correction-based configurations and carry-prediction-based configurations. Carry-prediction-based method is shown in Fig.1.

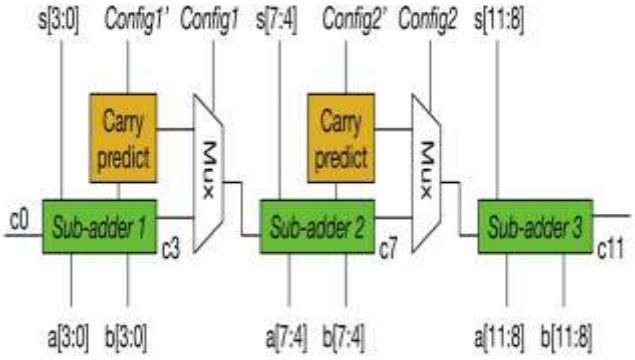


Fig-1: Carry-prediction-based configurable adder.

2. SIMPLE ACCURACY-RECONFIGURABLE ADDER:

An *N*-bit adder operates on two addends $A = (a_N, a_{N-1}, \ldots, a_i, \ldots, a_1)$ and $B = (b_N, a_{N-1}, \ldots, b_i, \ldots, b_1)$. For bit *i*, its carry-in is c_{i-1} and its carry-out is c_i.

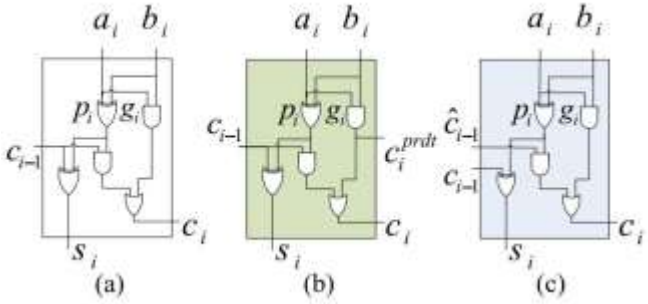


Fig-2: (a) Conventional full adder. (b) Carry-out selectable full adder. (c) Carry-in configurable full adder.

Conventional Full adder:

$$g = a_i \cdot b_i$$

$$p_i = a_i \oplus b_i$$

$s_i = p_i \oplus c_{i-1}$

$c_i = g_i + p_i \cdot c_{i-1}$

Carry Out selectable Full adder:

$c_i^{prdt} = g_i$

Carry in configurable Full adder:

$s_i = p_i \oplus c_{i-1}$

$c_i = g_i + p_i \cdot \hat{c}_{i-1}$

$\hat{c}_{i-1} = c_i^{prdt}$ in approximate mode
$\hat{c}_{i-1} = c_i$ in accurate mode

In SARA, an N-bit adder is composed of K segments of L-bit subadders, where K = N/L. Each subadder is almost the same as RCA except that the MSB of a subadder, which is bit i, provides a carry prediction as $c_i^{prdt} = g_i$

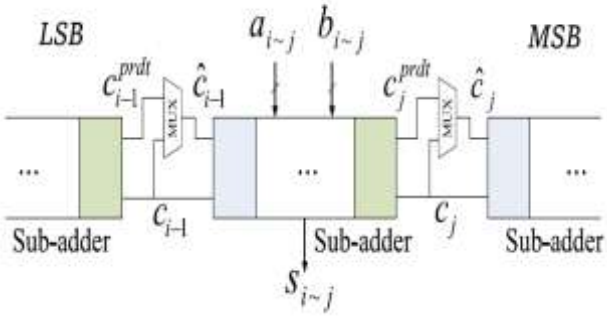
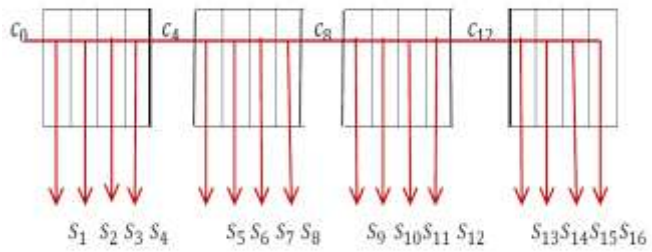
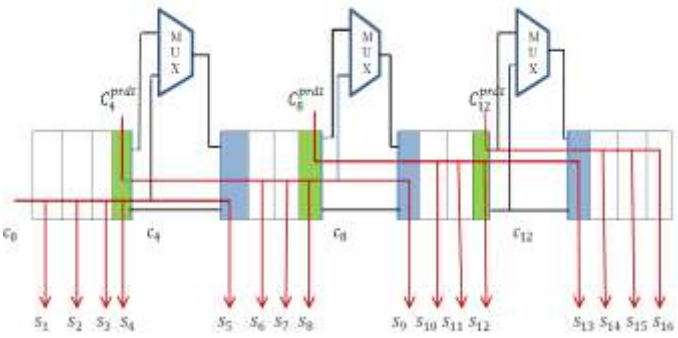


Fig-3: Design of SARA

The delay of sum bit depends on the carry chain propagated from its lower bits in multibit adder. When c_i^{prdt} is propagated, the delay of s_{j+1} is reduced as its path is shorten to be between bit $i - 1$ and $j + 1$.



LSB (a) MSB



(b)

Fig-4: Implementation of 16-bit adder in (a) RCA and (b) SARA.

As show in Fig-5, the 16-bit SARA working in approximate mode the sum s_9 uses the accurate carry c_8 from a lower subadder (bits 5 to 8). But c_8 is propagated from approximate carry c_4^{prdt} of another subadder (bits 1 to 4). In SARA the delay of s_9 is about six stages. In RCA, the delay of sum bit s_9 is nine stages. Comparing these two designs in SARA the delay of sum bit $s_9$is reduced by three stages.

DELAY-ADAPTIVE RECONFIGURATION OF SARA:

The accuracy configuration is decided by architecture/system-level applications. A self-configuration technique has been proposed for the scenarios where architecture/system-level choice is either unclear or difficult. The actual worst case path delay depends on addend values then self-configuration technique designed. A carry is propagated through several consecutive bits because of the actual path delay is large. When the actual carry propagation chain is short, there is no need to use approximation configuration, which is intended to cut carry chain shorter. A proposed a **DAR** technique: the output of a MUX in SARA is set to approximation mode only when a potentially long carry chain is detected.

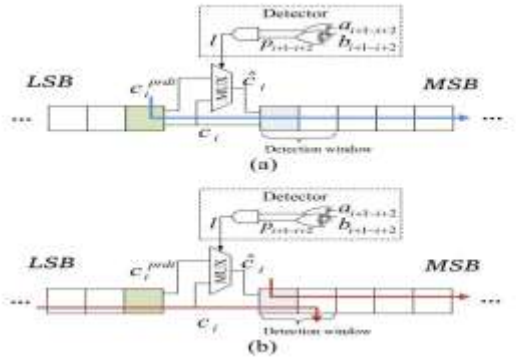


Fig-5: Design of DAR for SARA operating in (a) approximate mode and (b) accurate mode

The detection window size *W* decides the tradeoff between the accuracy and the effective carry chain length in accurate mode, which is *L* + *W*. When *W* increases, the error rate decreases while the critical path length in accurate mode increases.

EXPERIMENTAL RESULTS:

In proposed design, and evaluate the subadder bit-width of 1, 4, and 8 bits, referred to as SARA1, SARA4 and SARA8 respectively.

Table 1: Comparison of 16bit adder by different designs

	Area(LUT's)	Delay(ns)	Accuracy
SARA4_DAR2	27	2.689	High
SARA4_DAR2	26	4.521	High
SARA8	25	2.605	Moderate
SARA4	24	1.767	Moderate
SARA1	17	0.942	Less

APPLICATION:

Extension to Multiplier:

Multiplier is considered as a much bigger component of power consumption in datapath systems. In carryprediction based approximation uses generate bit to predict the carry from lower segments. The delay can be restrained to a smaller value with shorter critical path in carry propagation. Further extension of our technique to multiplier depends on the multiplication structure used in hardware implementation. There is a variety of hardware designs for multiplication, according to the structures of reduction tree.

Here the 8x8 wallace multiplier is implemented. It is an efficient hardware implementation of a digital circuit that multiplies two integers. Wallance multiplier is designed with ripple carry adder and Simple accuracy reconfigurable adder. When compared to RCA design with SARA Wallance multiplier delay is reduced.

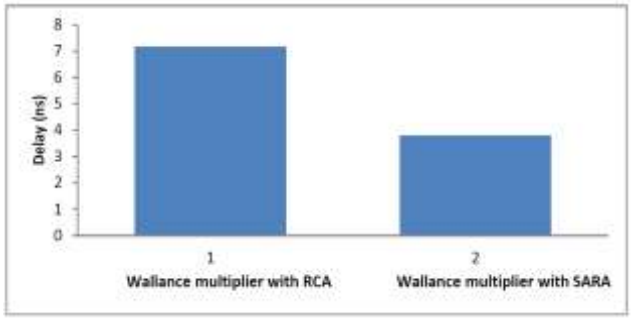


Chart -1: 8x8 Wallace multiplier with RCA and SARA

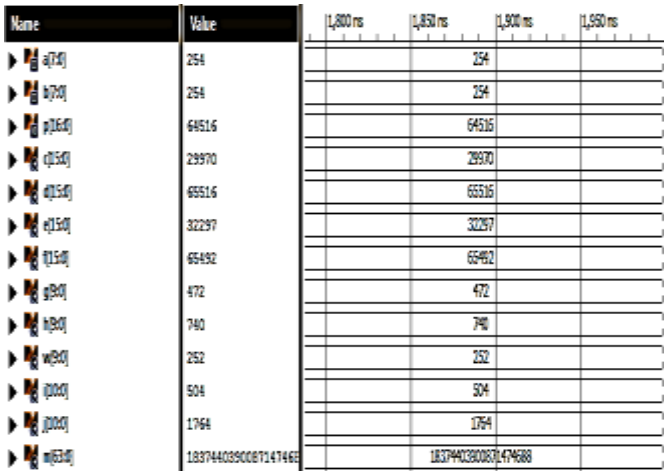


Fig-6: Simulation results of 8x8 Wallace multiplier by RCA

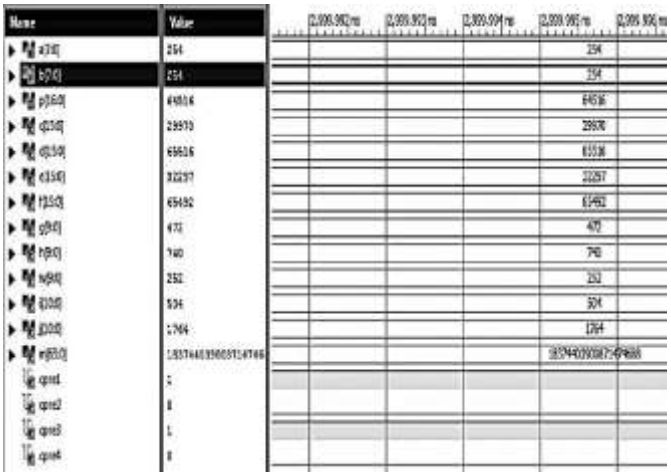


Fig-7: Simulation results of 8x8 Wallace multiplier by SARA

3. CONCLUSION

In this paper DAR with SARA design is proposed. SARA significantly reduces the power and area compared to the latest error correction configurable adder. Further the accuracy –power –delay efficiency is improved by including DAR technique. The efficiency of the adder is demonstrated by applying it in multiplier circuit.

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