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Design and Analysis of Current Starved and Differential Pair VCO for low Power PLL Application

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Abstract – *This paper aims for the design and analysis of current starved voltage controlled oscillator (CSVCO) and differential pair voltage controlled oscillator (DAVCO) for low power PLL applications with 180nm CMOS technology. Every circuit has been designed and simulated inside tanner EDA by SPICE under similar environment. Various parameters like frequency response, tuning range, and power dissipation of CSVCO and DAVCO have been analyzed and compared. The supply voltage for CSVCO and DAVCO are 1.8V and 2.5V respectively. The control voltage for CSVCO is varied from 0.5V to 1.0V, while from 0.5V to 1.3V for DAVCO. The average power dissipations for CSVCO and DAVCO are 42 microwatts and 1.42 milliwatts respectively. The high pace and locking all outputs of DAVCO has been assessed towards the lower energy utilization advantage of CSVCO.*

Keywords: VCO, PLL, Current Starved VCO, Differential Pair VCO, Frequency Gain.

1. INTRODUCTION

Function of closed loop frequency control systems work on the principle of detection of phase and/or difference of frequency between reference and output signals of transceiver. Voltage controlled oscillator used in Phase locked loop works as frequency synthesizers and clock recovery circuits. For long time, demodulation of FM signals has been done by PLL circuits and thus foster-seeley as well as radio detectors became obsolete. Various applications of voltage controlled oscillator results in different architectural designs for ex LC oscillator circuits, ring oscillator, relaxation oscillator etc. Differential amplifier ring oscillator employs less number of stages resulting in low power consumption. It has better speed and higher output oscillation stability. Due to these properties of differential amplifier work has been done in this paper. Other configuration such as partial positive feedback system has also lower power dissipation. LC oscillators are very important in generating higher frequency in microwave band, but there is circuit complexity in designing of inductors. LC oscillators require more area as compared to that of ring oscillators. An additional advantage of ring oscillator is wide tuning range too.

In this paper 180nm technology is used to analyze and compare ring oscillator of current starved and differential pair VCO architecture. The aim of paper is to design and perform the comparative analysis on the basis of tuning range, power dissipation, and tracking range of two different VCO designs i-e current starved VCO and differential pair VCO.

2. RELATED WORK

[1] Suraj Kumar Saw 2015, Current starved CMOS VCO with an ultra low power and low phase noise have been proposed. Power dissipation and circuit area are very less making it useful for wireless devices. Phase noise and transient response have been performed at 1MHz and phase noise comes out to be -104.0dBc/Hz with supply voltage of 1V.

[2] Deepak Balodi 2017, in this paper, frequency analysis of CSVCO and DAVCO has been done with 350 nm CMOS technology. Various parameters like tuning range , frequency response, and power dissipation of CSVCO and DAVCO has been compared under same environment.

[4] Shruti Suman 2016, PLL has been designed using ring VCO at supply voltage 3V with 180 nm CMOS technology. Proposed ring VCO has been used for implementation of PLL in GHz frequency range. Power dissipation of PLL is 28 milliwatts with frequency of 2.5 GHz.

[9] Rafiul Islam 2017, Ring oscillator with 3 stages has been designed with 90 nm CMOS technology. Supply voltage of 1.8V has been used for simulation. Control voltage has been varied from 0V to 0.6V. The linear tuning characteristics has been achieved from 4.52 GHz to 6.02 GHz. The power dissipation of the circuit is 0.295 milliwatts.

3. Methodology

The voltage Controlled oscillator is an electronic oscillator which is controlled by the input voltage. The voltage controlled managed ring kind oscillator structure is frequently used for VCO in CMOS technology. It includes numerous cells which form a closed loop. Preceding works submit few demanding situations inside the design of VCO which achieve high frequency for tuning range of wide nature and regular output swing linearity as well as

balanced design. The subsequent design of VCO are designed according to our need.

A. CURRENT STARVED VOLTAGE CONTROLLED OSCILLATOR (CSVCO)

The working of CSVCO is just like to that of ring oscillator. In the given figure M_2 and M_3 MOSFETs are implemented to work as an inverter. And the current sourcing feature had been received from MOSFETs M_1 and M_4.M_1 and M_4 MOSFETs control the current going to MOSFETs M_2 and M_3 forming an inverter. Thus inverter is starved by MOSFETs M_1 and M_4. The input control voltage at MOSFETs M_5 and M_6 controls the drain current of MOSFETs M_5 and M_6.The drain currents of MOSFETs M_5 and M_6 are reflected in every inverter.

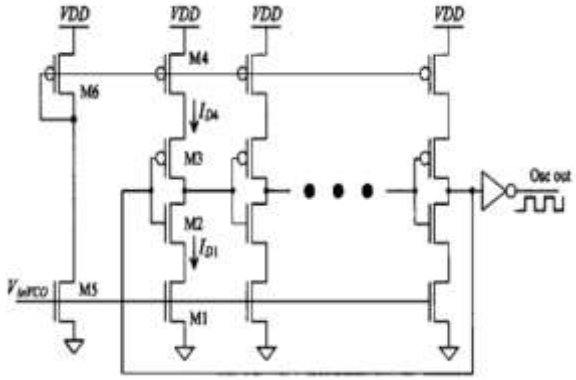

Fig - 1: Current Starved VCO

B. DIFFERENTIAL PAIR VCO

In the phase locked VCO structure, ring oscillator are used. Ring oscillator provides extensive tuning range and fantastically constant output voltage swing, these type of oscillators give operations at low voltage. Differential pair VCO is an oscillator of loop kind as shown in figure. Differential pair VCO gives the gain of high frequency. Firstly the delay cell is formed in the designing of this VCO . The postpone cell contains

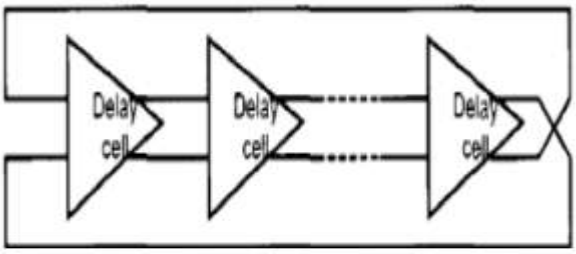

Fig - 2: Ring type Oscillator

a primary differential operational amplifier. The transistors of two PMOS put off cell had been aimed to work in the linear vicinity with the intention for acting like variable resistors. The output frequency is monitored using various variable resistances. It happens due to the fact that the frequency relies upon the interval of the time of the every put off cellular that's numerous by using the variable resistances. Rest transistors (PMOS) had been made to function in the saturation area. PMOS acts as the driving circuits hence we use the NMOS as energetic load. Schematic of the delay cells is indicated by the figure 2. The kind of the postpone cellular having mail limitation that it is unable to keep regular swing of output voltage. It happens due to the fact that when control voltage varies positive output voltage and negative output voltage may trade. It happens because when the control voltage changes, the resistance throughout the transistor (PMOS) usually vary. The trade in these points causes the variation the output swing and creates nonlinearity. The strategy for this disadvantage is to give biasing of inner circuitry instead of unique every level biasing circuit. It gives a easier layout. Current in every stage of differential oscillator is controlled by the voltage Vb1 and Vb2 of control circuit,. Hence it controls the delay of the every circuit thus increasing or decreasing the frequency of oscillation of every stage. More degree range bring about decreasing the range of the frequency because there is inversely proportional relationship between frequency range and two instances delay of each ranges as well as degree having less number. By the result of the speed-energy trade off, this is proper to lower wide variety ranges in hoop for volume, therefore in this design seven tiers differential pairs are used. In the given schematic it is seen that control voltage is put earlier to the differential stage which bias each differential stage of the differential VCO. The delay of each stage decides the output clock frequency. The delay is managed by the control voltage. The huge tuning variety of each stage gives the wide variety of frequency.

Few problems are there in this schematic that due to use of single tail current, the range of tuning restrained by manipulating range of voltage. The control voltage is generally greater than 0 and less than or equal to supply voltage (V_{dd}).

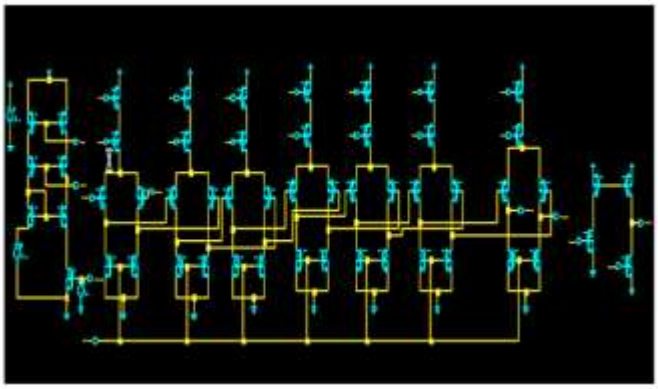

Fig - 3: Differential Pair VCO to be designed

If we select the small tail current then the output range of frequency of VCO is also small. And if we select the large tail current then the range of output frequency of VCO is also larger [8].

4. RESULT AND DISCUSSION

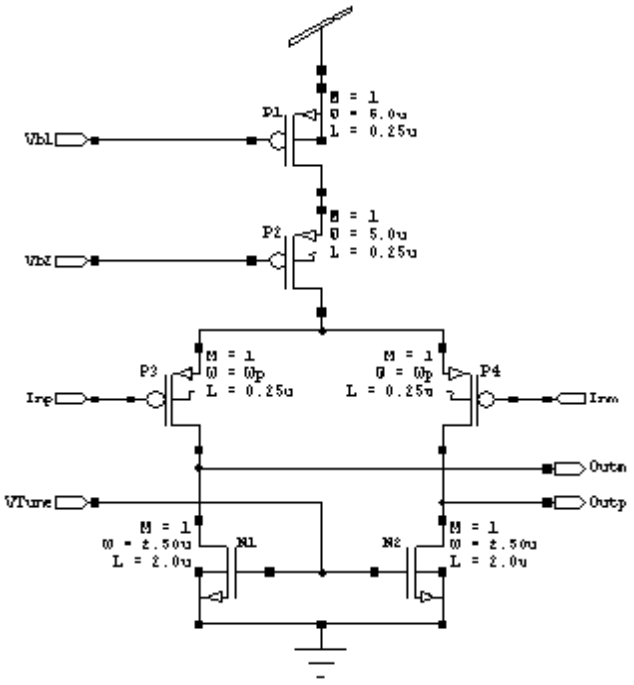

Fig - 4: 9 Stages of DA VCO Cell Diagram

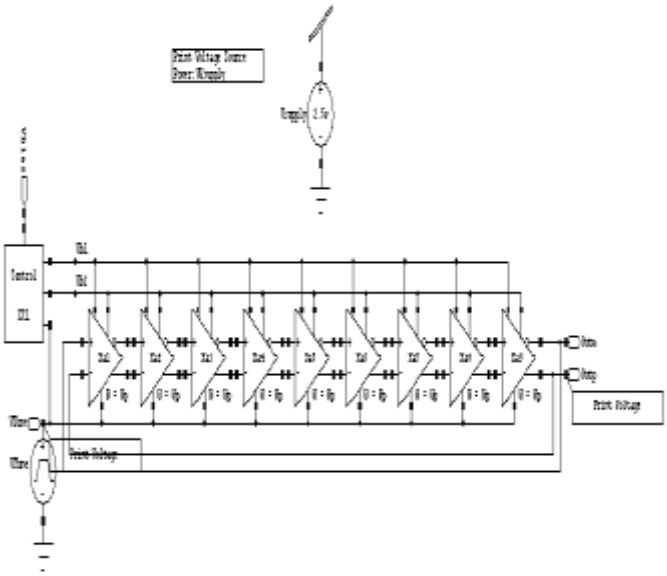

Fig - 5: 9 Stages of DA VCO Schematic Diagram

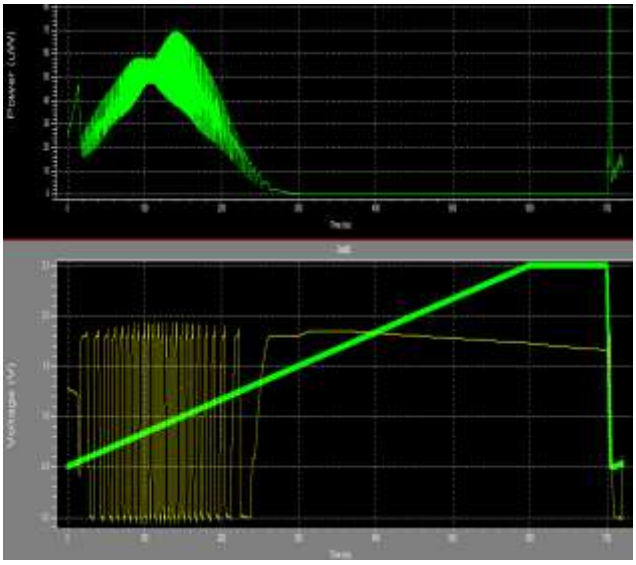

Fig - 6: Simulation Result of 9 Stages of DA VCO

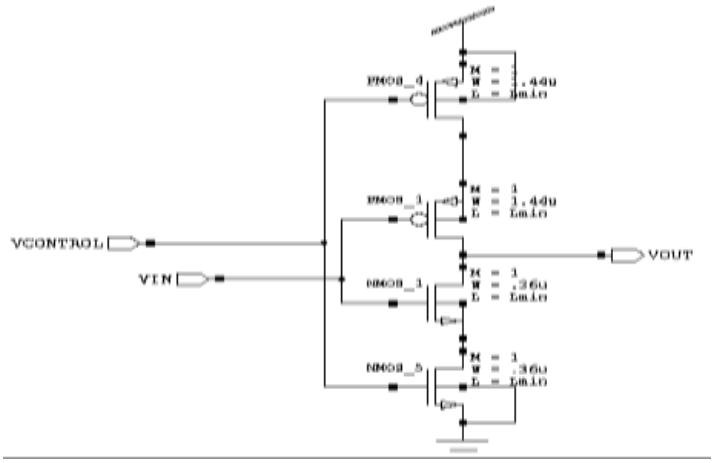

Fig - 7: 9 Stages of CS VCO Cell Diagram

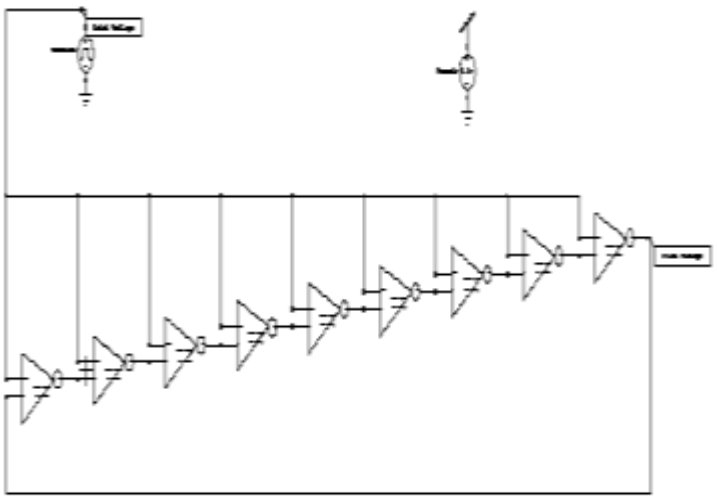

Fig - 8: 9 Stages of CS VCO Schematic Diagram

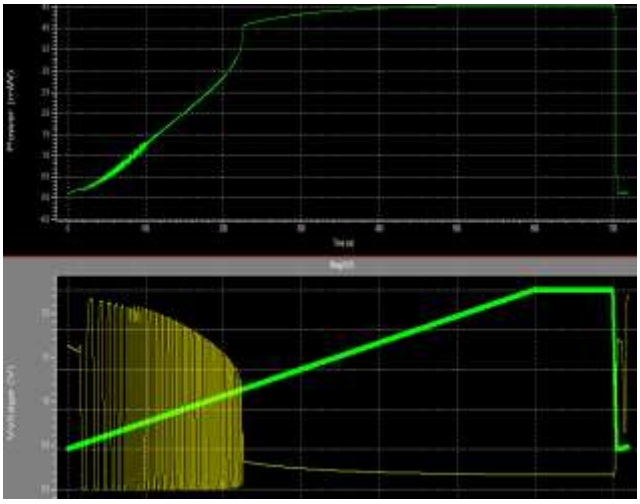

Fig - 9: Simulation Result of 9 Stage of CS VCO

A. FREQUENCY RESPONSE AND LINEARITY

The important characteristics of VCO is its linearity of the output oscillation's verses the input control voltage. The output oscillation frequency with respect to tuning voltage ($V_{control}$) is plotted in Figure 4 and Figure 5.Table 1 and 2 shows the frequency response of 9 stages DAVCO and 9 stages CSVCO at different control voltage ($V_{control}$).

Table - 1: Frequency Response of 9 Stages DAVCO

V Time (v)	Frequency (MHz)
0.5	104
0.6	130
0.7	210
0.8	357
0.9	484
1	595
1.1	666
1.2	690
1.3	740

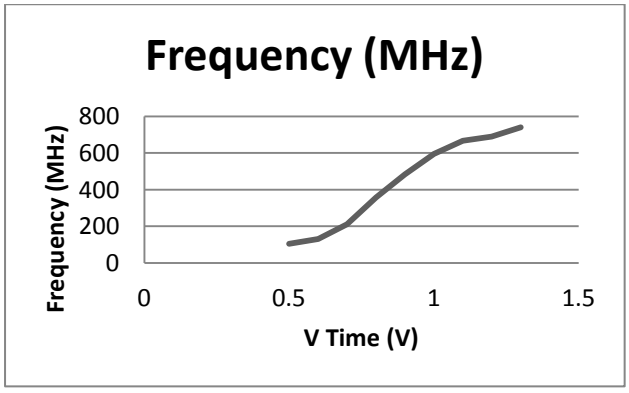

Fig - 10: Characteristic Curve of 9 Stages Differential Pair VCO

Table - 2: Frequency Response of 9 Stages CSVCO

Control Voltage (volt)	Frequency (MHz)
0.5	133
0.6	147
0.7	164
0.8	285
0.9	333
1	343
1.1	293
1.2	240

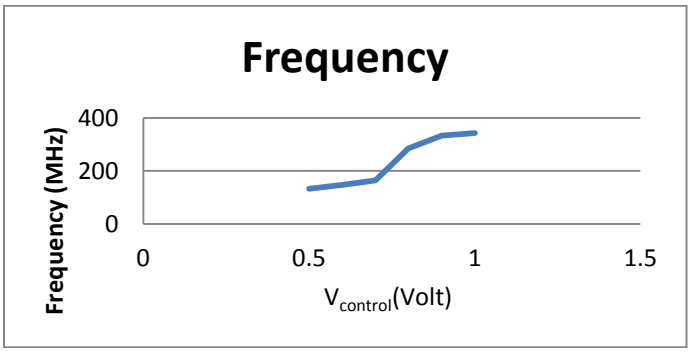

Fig - 11: Characteristic Curve of 9 Stages CSVCO

We can observe here that frequency gain of differential VCO is larger than that of CSVCO. The tuning range of differential VCO is also larger than that of CSVCO which is important advantage of differential VCO over CSVCO.

B. POWER CONSUMPTION

The power consumed by differential pair VCO at differential control voltage is given in Table 3.

Table - 3: Power Consumption of 9 Stages Differential Pair VCO

Tuning Voltage(volt)	Power Consumption(mW)
0.5	0.3
0.6	0.4
0.7	0.5
0.8	0.8
0.9	1.2
1.0	1.7
1.1	2.30
1.2	2.75
1.3	3.25

The average power dissipation of differential pair VCO is 1.47 milliwatt. The power consumed by the different components of differential pair VCO is given in Table 4.

Table - 4: Consumption of Power in PLL components using Differential Pair VCO

Components	Power Consumption (mW)
Differential Pair VCO	1.47
Frequency Divider	0.27
PFD	0.28
Charging Pump	4.21

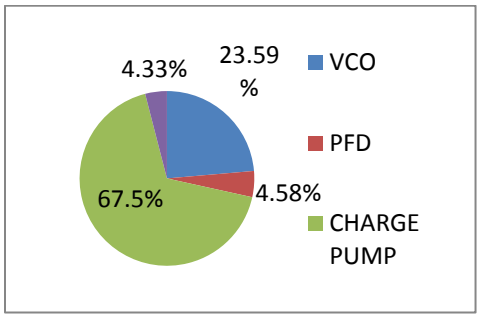

Fig - 12: Sharing of Power in PLL Using Differential Pair VCO

For PLL having differential pair VCO, the differential pair VCO consumes 23.59% of total power consumed by PLL, while power consumption by frequency divider is 4.33% which is minimum. Charge pump consumes maximum power which is 67.5%. 5% of total power is consumed by PFD.

The power consumed by the CSVCO at different control voltage is given in Table 5.

Table - 5: Power Consumption of 9 Stages Current Starved VCO

Tuning Voltage(volt)	Power Consumption (mW)
0.5	0.025
0.6	0.030
0.7	0.039
0.8	0.050
0.9	0.053
1.0	0.055
1.1	0.054
1.2	0.031

The average power consumed by the CSVCO 0.042 milliwatt. The power consumed by the different components of PLL using CSVCO is given in Table 6.

Table - 6: Consumption of Power in PLL Components Using Current Starved VCO

Components	Power Consumption(mW)
CSVCO	0.042
Frequency Divider	0.248
PFD	0.31
Charging Pump	0.582

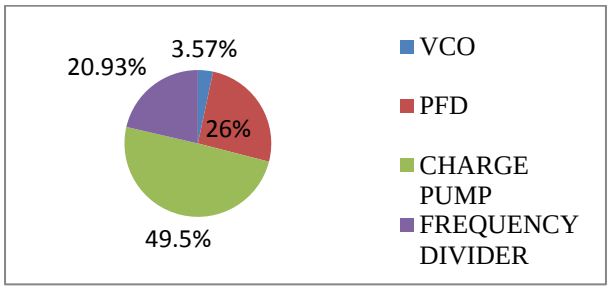

Fig - 13: Consumption of Power in PLL Using CSVCO

The power consumed by CSVCO is 3.57% of total power. The charge pump consumes 49.5% of total power while power consumed by PFD and frequency divider is 26% and 20.93% respectively.

5. CONCLUSION

Here we conclude that the power consumed by differential pair VCO is higher (i.e. 1.47 mW) as compared to the power consumed by CSVCO (i.e. 0.042mWatt). This occurs because of the larger number of transistors used in case of differential pair VCO. The low power consumption property is main advantage of CSVCO over differential pair VCO. We can also conclude that the frequency gain of differential pair VCO is larger (740MHz) as compared to that of CSVCO (i.e. 240MHz). Also, the differential pair VCO gives the wider tuning range (i.e. 0.5V to 1.3V) as compared to that of CSVCO (i.e. 0.5V to 1.1V). The frequency curve of the differential pair VCO comes out to be more linear than that of CSVCO. Hence for the frequency gain and linearity point of view, the differential pair VCO is proved to be better choice, While for the power consumption point of view CSVCO is most efficient design. The choice using both VCO depends upon the type of requirements. For example differential pair VCO is used in fast communication devices, while CSVCO is used in case of remote wireless circuits consuming low power.

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BIOGRAPHIES

Vaibhav Yadav received the B.Tech degree in Electronics and Communication Engineering from Babu Banarasi Das Engineering College, Abdul Kalam Technical University Lucknow, India and is currently working towards his M.Tech degree in Microelectronics with the research interest in VLSI and the enhancing the performance of VCO Circuits from Institute of Engineering and Technology, Lucknow, Uttar Pradesh.