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Comparison of Multiplier Design with Various Full Adders

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Abstract - *A multiplier has an important role in various arithmetic operations in the applications of digital signal processing which includes digital filtering and power analysis in the field of communication. The design of fast and low power multipliers has been a huge theoretical and practical concern for scientific researchers. In this paper the analysis of 4*4 Array and 4*4 Wallace tree multiplier and comparison is being done by using different full adders namely Conventional full adder, Transmission function full adder and Hybrid full adder. This work has been done in a schematic editor using Tanner tool v14.1 in 0.18nm CMOS technology. T-spice is used as simulator and W-editor is used to show the waveform of multiplier. The material area required to design a multiplier is reduced. Due to the reduction of material area, this causes the low power consumption, minimized area and time delay.*

Key Words: **4*4 Array Multiplier, 4*4 Wallace Tree Multiplier, Full Adder, Hybrid Adder**

1. INTRODUCTION

Adders and Multiplier designs are the important elements of VLSI Design. With advanced growing chip designing, many researchers and developers have taken much effort to design multipliers which initiates high speed, reduced power consumption and reduced area of multipliers, thus making them compatible for various high speed, low power, and compact VLSI implementations. Area, speed and power are the important parameters; the power is affected due to increasing speed and area. Here the two multipliers such as Array and Wallace tree multipliers designed to obtain an efficient multiplier. Due to its high degree of regularity, array multiplier structure is suitable for VLSI implementation.

The multiplier design is a central component of the digital signal processors. Therefore, the demand for multiplier-performance improvement is increased day to day, because multipliers are a major source of power dissipation factor. Reducing the power dissipation of multipliers is the required solution to achieve the overall power characteristics of various digital circuits and systems. In this check, power consumption for multipliers are explained and power comparisons of array and Wallace tree Multipliers are obtained for reduced power consumption, and various adder logics were used. The adders are implemented in multipliers for the reduction of power and the required transistor count. The adders such as Conventional CMOS full adder (CFA), Transmission Function full adder (TFFA), Hybrid adder were designed for increasing the performance of multipliers.

2. LITERATURE SURVEY

Pallavi Saxena et al (2015) [1] proposed a paper on "Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder". In this paper constraint carry select adder architectures are proposed using parallel prefix adders (Brent Kung Adder) is used to design linear Carry Select Adder. By using Carry look ahead adder to derive fast results but they leads to increase in area.

Sandeep Kakde et al (2015) [2] proposed a paper on "Design of Area and Power Aware Reduced Complexity Wallace Tree Multiplier". In this paper, the work has been done to reduce the area by using energy efficient CMOS full adder. By using the multiplier, the system complexity is increased.

Shradha Agrey et al (2015) [3] proposed a paper on "Comparative Analysis of Different Adders for Wallace Tree Multiplier". Booth algorithm is used to reduce the number of input bits required for the multiplication to be correct.

Rajaram S et al (2011) [4] proposed a paper on "Improvement of Wallace Multipliers using Parallel Prefix Adders". In this paper, employing parallel prefix adders (fast adders) at the final stage of Wallace multipliers to reduce the delay.

3. REVIEW OF FULL ADDER DESIGNS

Adders are basic blocks needed to design a multiplier. The full adder can be described by the concept as follows: Given the three 1-bit inputs A, B, Cin, it is required to calculate the two 1-bit outputs sum and Cout, where,

Sum = A xor B xorCin(1)
Cout = AB + B Cin + Cin A(2)

A. Conventional CMOS Full Adder

In Conventional CMOS Full Adder design, which contains 22 transistors, a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding additional two series of PMOS and NMOS transistors

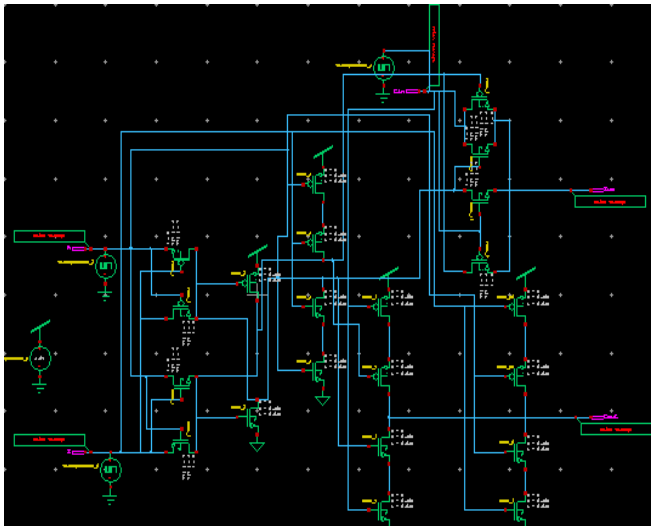

***Fig-1**: Conventional CMOS full adder*

B. Transmission Function Full Adder

Transmission function full adder logic design is a special type of pass-transistor logic circuit. The logic function is controlled by using complementary control signals were NMOS and PMOS transistors are connected in parallel. While applying logic signals either "0" or "1", then transistors are turned ON simultaneously. Thus, there is no voltage drop problem while the "1" or "0" is passed through it [2]. It contains 20 transistors. There is no need to use multiplexer for designing transmission function full adder, which leads to reduced power consumption.

The adders considered in this full adder were designed by using (22 transistors) conventional implementing techniques, i.e. [8] this technique uses only transistors and no input capacitors are used. Main drawback of conventional CMOS full adder is having multiplexer in its design. The use of multiplexer in this design causes increased area for the full adder design. Power consumption rate and execution of time will be automatically increased while using multiplexer.

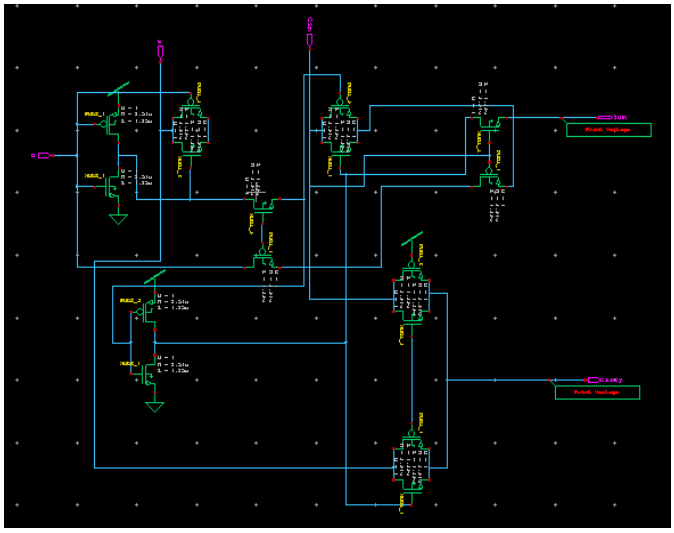

***Fig-2:** Transmission Function full adder*

C. Transistor Full Adder

The new improved design of 14T adder cell requires only 14 transistors to recognize the adder function shown in Fig. 3. It produces better results such as threshold loss, speed and power by inserting four extra transistors per adder cell [7]. If the transistor count increased from three to four per adder cell, then it reduces the main issue of threshold loss, which is already exists in the SERF by inserting one inverter in between XOR Gate outputs and it form XNOR gate [2]. For proposed design there is no need of gate design, number of full adders to be used to design the multiplier.

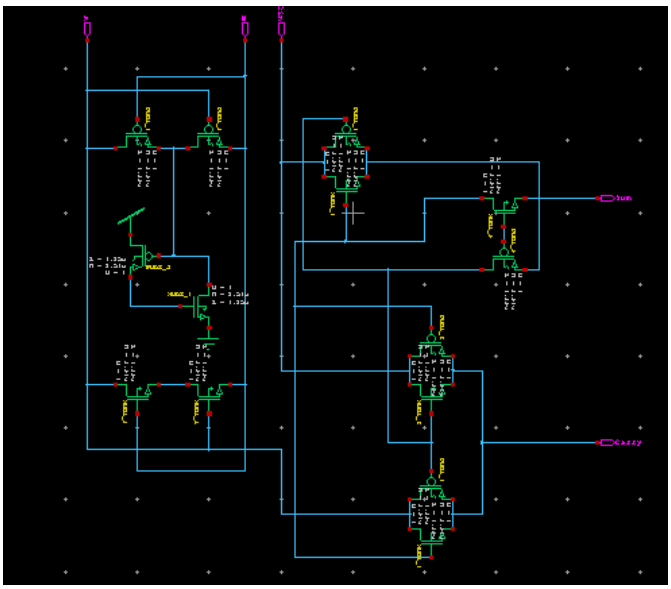

***Fig-3:** Transistor full adder*

D. Hybrid Full Adder

Previous conventional CMOS full adder is designed by using 22 transistors, Transmission Function full adder has 16 transistors and Transistor full adder has 14 transistors. From the design, number of parameters such as transient time, area and power consumption were analyzed. In proposed design the same hybrid full adder is designed using 12 transistors; it shows reduced power consumption and area [10]. From the analysis the Array and Wallace tree multipliers are designed using this proposed hybrid full adder. The control signal is given to the gate of n-mos, and its inverted signal is given as a functional to the gate of the p-mos device. Nmos pass transistor is good for transmission of '1'and poor for transmission of '0' p-mos pass transistor is good for transmission of '0' and reduced for transmission of '1'. The circuit of the 12 pass transistor adder is shown in Fig.5. Power consumption will be reduced to 0.8946 mW and the execution time taken for the hybrid adder is 0.45seconds [5]. This result shows better performance regarding speed and low power consumption [6]. The output voltage swing will be equal to the VDD, if a driver is used at the output of design.

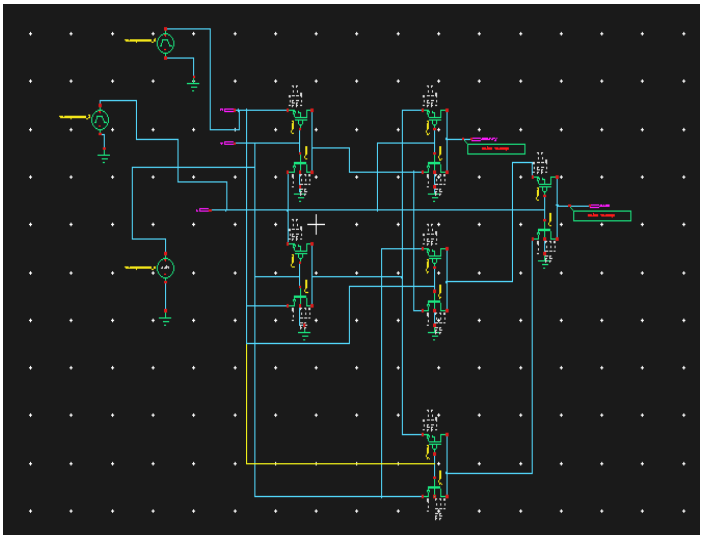

Fig-4: *Hybrid full adder*

4. OVERVIEW OF MULTIPLIER

The multipliers play an important role in basic arithmetic operations like addition, subtraction in digital signal processor applications. The recent development in the processor is to design a reduced power consumption of multiplier. So, the importance for low power multipliers increased gradually. Generally the computational performance of processors in DSP is affected by its multiplier performance. In this section basic Array Multiplier and Wallace Tree Multiplier were designed and the performance of each multiplier be evaluated.

A. Array Multiplier:

In an array multiplier, the counters are arranged in a sequential flow for all bit positions of the Partial Product parallelogram. An array multiplier structure as shown in Figure 5. It uses short connecting wires that go from one full adder to adjacent full adders at three directions such as horizontally, vertically or diagonally [8]. The equation given below explains the terms are summed by an array of n [n - 2] full adders and n number of half adders. The shifting of partial products for their alignment is performed by simple routing and. The number of rows in array multiplier identifies the length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders.

$$T_{critical} = [(N-1) + (N-2)]*T_{Carry} + (N-1)*T_{Sum} + T_{and} \quad (3)$$

Where Tcarry is the delay propagation between the input and Output carry, Tsum is the delay between the input carry and sum bit of full adder, Tcarry is the time delay of AND gate, and Nis the length of multiplier. The output of each row indicates width of multiplicand. The output of each row of adder acts as input to the next row of adders for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array acts as input of the next adders to be used.

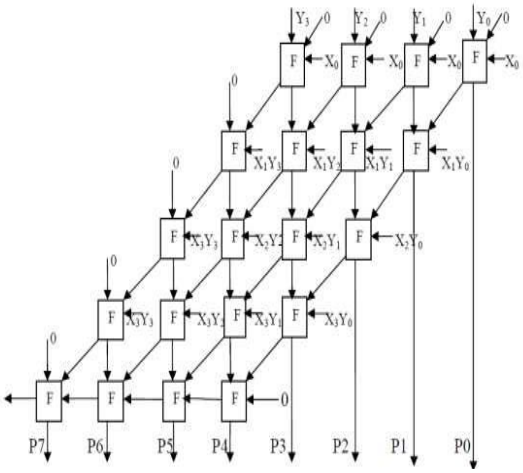

Fig-5: *Array Multiplier Structure*

B. Wallace Tree Multiplier:

Wallace trees were initially introduced in order to design the multipliers whose compilation time increases based on the logarithm of the number of bits to be multiplied should be increased rapidly. Wallace tree multiplier is based on tree structure [6]. In Fig.3, it shows 4 bit Wallace tree multiplier. Wallace method uses two-steps to process the multiplication operation,

(i) Formation of bit products
(ii) The bit product matrix is reduced to a 2-row matrix by using a carry-save adder (Wallace tree).

The time delay related with the array multiplier, the time taken by the signals to propagate through the AND gates and adders that forms the multiplication operation of array [5], [9]. The time Delay of an array multiplier depends on the intensity of the array and it is not on the partial material thickness. The delay of the array multiplier is given by,

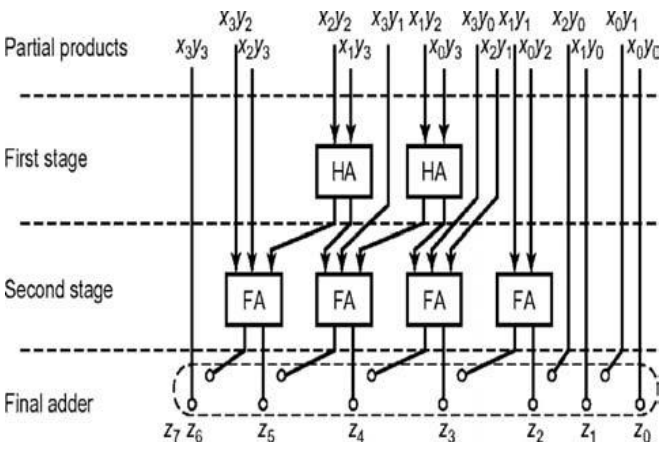

Fig-6: Operation of Wallace Tree Multiplier

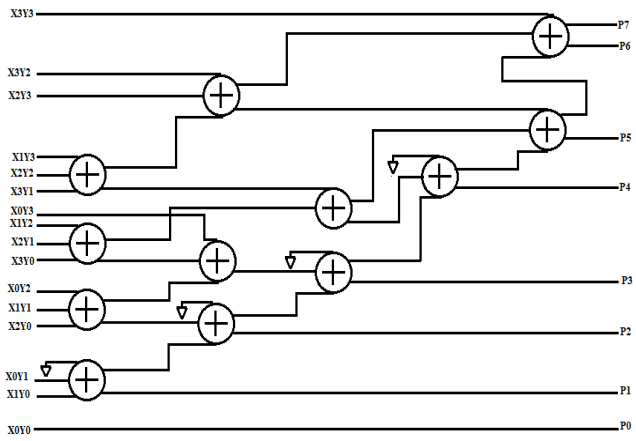

Fig-7: Structure of Wallace Tree Multiplier

5. SIMULATION RESULT OF MULTIPLIERS

Array and Wallace tree multipliers are designed using full adders with reduced transistor count [9]. The full adders such as Conventional CMOS full adder (CFA), Transmission Function full adder (TFFA), Hybrid adder are to be replaced as full adder in a multiplier design. Each full adder design has unique power performance and produce reduced power consumption at the multiplier design [1]. The simulation result of array multiplier and Wallace tree multiplier was designed by using TANNER V14.1.

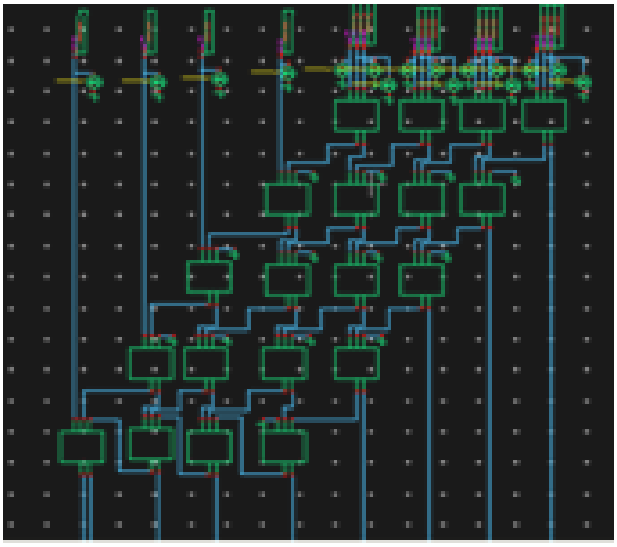

Fig-8: Schematic Design of Array Multiplier

There are 16 number of full adders needed to design an array multiplier. The connection of full adders is made in row by row for array structure. The full adder structures such as CFA, TFFA, and Hybrid full adder are to be placed as full adders in Multiplier, and the performance of each design to be analyzed [8]. Similarly the same full adders are placed as full adders in Wallace tree multiplier. Each full adder has its own characteristics to be performed for the operation of multiplier.

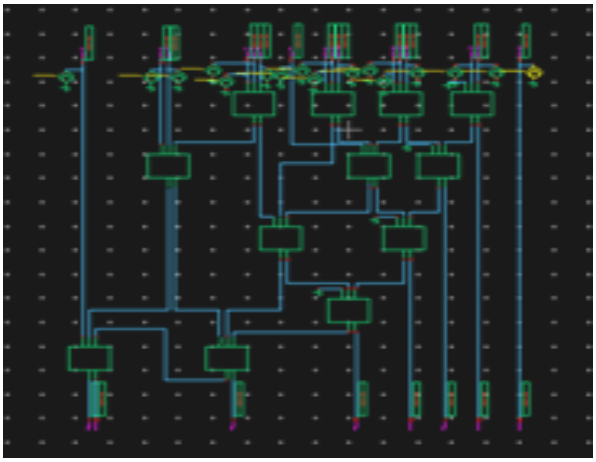

Fig-9: Schematic Design of Wallace Tree Multiplier

The performance evaluation for the above two multipliers are compared with various full adders. The efficiency of multiplier is depends on the number of transistors needed to design a full adder.

Table-1: Array Multiplier Using Different Full Adders

Replaced Full Adder	Power Consumption	Transient Time
Conventional CMOS Full Adder	41.381mW	0.75secs
Full Adder	22.264mW	0.59secs
Transistor Full Adder	17.661mW	0.69secs
Transmission Function Full Adder	11.605mW	0.72secs
Hybrid Full Adder	1.659mW	0.63secs

Table-2: Wallace Tree Multiplier Using Different Full Adders

Replaced Full Adder	Power Consumption	Transient Time
Conventional CMOS Full Adder	15.688mW	0.44secs
Full Adder	13.916mW	0.64secs
Transistor Full Adder	14.709mW	0.30secs
Transmission Function Full Adder	9.087mW	0.38secs
Hybrid Full Adder	0.8946mW	0.45secs

6. CONCLUSION

The power performance characteristics of Array multiplier and Wallace tree multiplier using Conventional CMOS full adder, Transmission Function Full adder, Transistor Full adder and proposed hybrid 12 transistor full adders were performed and analyzed. The main objective of VLSI design is to reduce the power consumption and area, here the proposed method of designing the hybrid adder exhibits better power performance than the existing Full adder designs. The number of half adders in an existing design of multipliers is replaced with full adders to reduce the complexity of design. Due to the reduction of area and power consumption in this proposed system will automatically reduce the transient time of 4*4 Array and Wallace tree multiplier over the existing designs. The performance evaluation for the above two multipliers are compared with various full adders. The efficiency of multiplier is depends on the number of transistors needed to design a full adder.

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BIOGRAPHIES

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