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Study of Unsymmetrical Cascade H-bridge Multilevel Inverter Design for Induction Motor

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Abstract - *This Paper purpose of the study of Unsymmetrical Cascaded Multilevel Inverter (MLI) using fixed frequency level shifted carrier based pulse width modulation technique. This new control scheme is applied to 7 levels to 9 levels Unsymmetrical Cascaded Multilevel Inverter (CMLI) design for induction motor load. These different firing angle control schemes in LSCPWM for multilevel unsymmetrical cascaded multilevel inverter are compared. This unsymmetrical cascaded multilevel by using only 2-H bridges with 8 switches we can get 7 level output voltage where as in symmetric cascaded MLI 7 level output voltage is obtained by using 3- H bridges with 12 switches. The results are observed by MATLAB/SIMULINK software.*

Key Words*: *Single phase Induction motor, Unsymmetrical CMLI, LSPWM, THD, PD, and IGBT

1. INTRODUCTION

Induction motor is the most widely used electrical machine in almost all simple, medium and high voltage industrial applications, because of its low cost and increased reliability. Development of high power and low cost power electronic devices in the recent past has provided a larger area of application for the ac drives. Hence, ac drives like induction motor drives along with power electronic converters have replaced the dc motor drives in industries. In recent era there is a huge capacity of power used in industries and other areas. Multilevel inverter has become popular to fulfill usage of power [1] generally simple inverter gives 2 or 3 level output voltage but multilevel inverter gives 3 or more output voltage levels. It produces a stepped output voltage with reduced harmonic distortion when compared to a 2 level inverter. Multilevel inverters are basically 3 types [2]

- Flying capacitor inverter (FCI)
- Cascaded inverter (CI)
- Diode clamped inverter (DCI)

The most commonly efficient inverter is cascaded 7 level and multilevel inverter. It provides higher output voltage and power levels. It's one of the mostly used methods used for drive application which meet the requirements such as high power rating with reduced THD and switching losses. The Unsymmetrical Multilevel Inverter increases the number of levels in the output and reduces the number of input DC sources required [3]. The IGBT is used as semiconductor switch for designing the inverter circuit. It has the high power rating, less conduction loss and less switching loss. DC sources are basically two types which are Unsymmetrical DC source and symmetrical DC source. Unsymmetrical DC source does not have equal magnitude of voltage whereas symmetric DC source has equal magnitude of voltage. Unsymmetrical cascaded MLI has less number of DC source voltage and switches as compared to symmetrical cascaded MLI. The advantage of an unsymmetrical cascaded has an increased number of voltage levels for a given module counts. The comparison between unsymmetrical cascaded 9 level MLI and 7 level MLI were done and based on the results obtained the most effective MLI is adopted that gives the reduced THD output and better performance for the single phase induction motor load.

Multilevel inverter topologies and different modulation strategies in [10]. Different multilevel inverter topologies are flying capacitor type, diode clamped and cascaded type inverters.

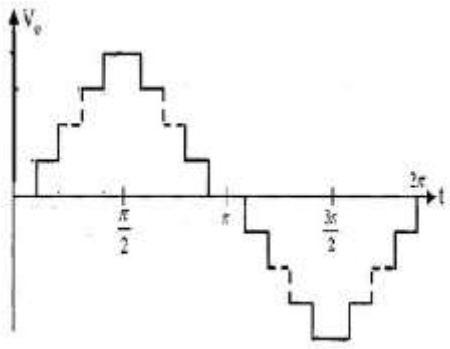

Fig 1: Generalized Stepped Voltage Waveform

There is a various modulation strategies used commonly are Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Elimination (SHE), and Space Vector Control (SVC). Multilevel inverters can achieve higher voltage levels without the need of a transformer and also the voltage stress across the devices remains half, low dv/dt of the output voltage, and low electromagnetic interference, resulting in low Total Harmonic Distortion (THD). So that, they are emerging as an attractive solution to medium-voltage high-power AC drives**.**

2. TOPOLOGY OF H-BRIDGE CASCADED MULTILEVEL INVERTER

The Topology of the unsymmetrical cascade 7 Level and 9 Level multilevel inverter is shown in Fig 2 seven-level symmetric H bridge multilevel inverter has three H-

bridges. The DC source for the three H-bridges H1, H2, H3 is Vdc. In this topology the output voltage of the individual H bridges is $-V_{dc}$, 0 or $+V_{dc}$. Therefore the output voltage of the inverter can have the values $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, which gives a five level output voltage. The switching states of symmetrical five level output voltage is given in the Table. 1. [5]

The number of voltage levels (m) in the phase voltage of symmetrical CMLI inverter can be found from

m = (2N+1)

Where N is the number of H-bridge cells per phase leg The maximum output phase voltage of these N cascaded multilevel inverters is

$V_{0, MAX} = NV_{dc}$

Calculated by[6]
Nsw = 4N

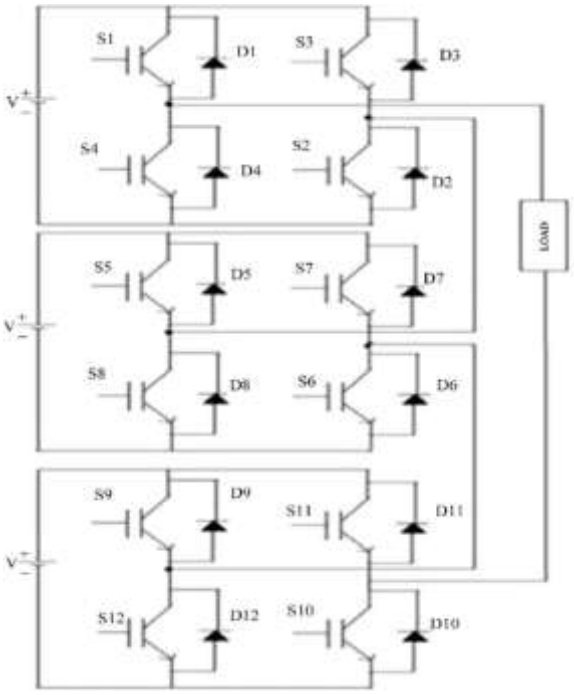

Fig. 2: Symmetrical cascaded seven level inverter Topology

Unsymmetrical multilevel have the same topology as symmetric multilevel inverters. They differ only in the rating of input dc voltages and control strategies. For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, a scheme is proposed which uses lesser number of bridges. A seven-level unsymmetrical cascaded H-bridge multilevel inverter has two H-bridges for each phase. The DC source for the first H-bridge (H1) is $V_{dc}/2$, while the DC source for the second bridge (H2) is V_{dc}. The switching states of unsymmetrical seven level output voltage is given in the Table. 1

The number of voltage levels (m) in the phase voltage of symmetrical CMLI inverter can be found from $m = 2^{N+1} - 1$, if $V_{dc} = 2^{j-1}V_{dc}$, j = 1, 2, 3,....N Where N is the number of H-bridge cells per phase leg\ The maximum output phase voltage of these N cascaded multilevel inverters is

$V_{0, MAX} = (2^{N+1} - 1)V_{dc}$

The total number of active switches used in the CML inverters can be calculated by

Nsw = 4N

3. THE OPRATION OF CASCADE MULTILEVEL TOPOLOGY

The Unsymmetrical cascaded multilevel inverter has 3 DC sources and 12 power switches magnitude of DC sources are 100V, 200V and 100V respectively. The sources are connected to 3 H-Bridge units which known as cascaded in single phase. This individual H-bridge the output voltage is $+V_{DC}$, 0 or $-V_{DC}$. Hence this desired output voltage for 9 level Unsymmetrical Cascade Multilevel Inverter are $+4V_{DC}$, $+3V_{DC}$, $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$. To get the respective output voltage the power switches are turned ON and turned OFF. By making of the proper combination of switches we got the desired output voltage. To get maximum output voltage +4V; the switches S1, S10, S9, S6, S5 AND S2 are ON and remaining switches are OFF at this time. For +3V; the switches S1 S10, S12, S6, S5and S2 are ON and remaining are OFF. Similarly all voltage levels can be analyzed by see the table given below Table number 1.

Table no. 1 Switching pattern for Unsymmetrical cascaded 7 level inverter

O/P	4V	3V	2V	V	0	-V	-2V	-3V	-4V
S1	1	1	0	1	0	0	0	0	0
S2	1	1	1	1	0	0	1	0	0
S3	0	0	0	0	0	1	0	1	1
S4	0	0	1	0	0	1	1	1	1
S5	1	1	1	0	0	0	0	0	0
S6	1	1	1	1	0	1	0	0	0
S7	0	0	0	0	0	0	1	1	1
S8	0	0	0	1	0	1	1	1	1
S9	1	0	0	0	0	0	0	0	0
S10	1	1	1	1	0	1	1	1	0
S11	0	0	0	0	0	0	0	0	1
S12	0	1	1	1	0	1	1	1	1

4. MODULATION TECHNIQUES

By using the modulation technique multilevel inverter has to synthesize a staircase waveform to have controlled output voltage. There are various modulation techniques available. So basically the control technique can be classified as the pulse width modulation (PWM) which is considered as the most efficient method. In this inverter, level shifted pulse width modulation [5] used. Here we are using phase disposition (PD) modulation technique. The reference signal has 50 HZ frequency and carrier waves have 2KHZ to 3KHZ frequency.

Here we uses triangle generator for the purpose of carrier wave. The modulation index is 0.97. The formula used for MI is

Modulation index = V_{ref}/V_{car}

Where V_{ref} is reference voltage and V_{car} is carrier

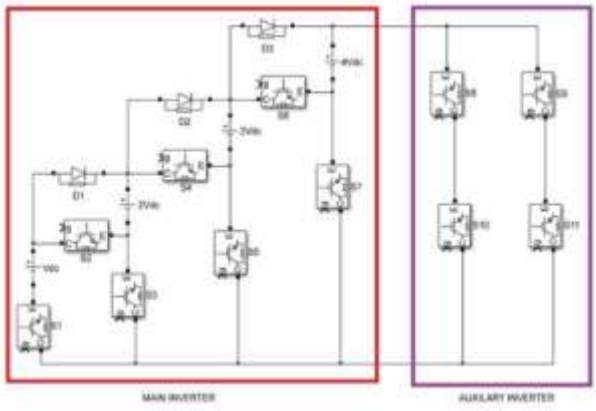

Fig 3: Structure of proposed multilevel inverter

The generated from above model of complete gate pulses which are shown in fig 4 which is shown below.

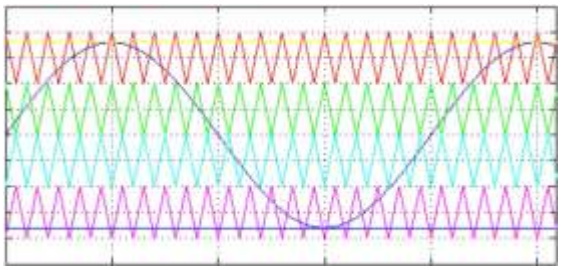

Fig 4: Reference and carrier waveform for PD 7 level MLI

5. SIMULATION OF MULTILEVEL INVETER

To study of analyze the performance of proposed cascaded seven level inverter, respective inverter together with induction motor has been studied in Matlab 2013 and 2014 simulation environment by imposing various modulation technique in order to study the experimental results and total harmonic reduction percentage. Simulink offers an embedded set of tools, for the simulation of electrical systems which was used to build converter circuits. The system used during the experimentation is Intel core Acer over windows 10 having RAM of and hard disk. Motive to work in the following simulation environment is the enhancement of efficiency. Simulink blocks be able to used to implement the control algorithm and they can be easily connected to Power System blocks. The matlab simulink environment is used here to simulate 7 level inverter using induction motor drive.

Parameter	Value
Voltage (V)	220
Frequency(Hz)	50
No. Of pole pairs	2
Speed (rad/sec)	156

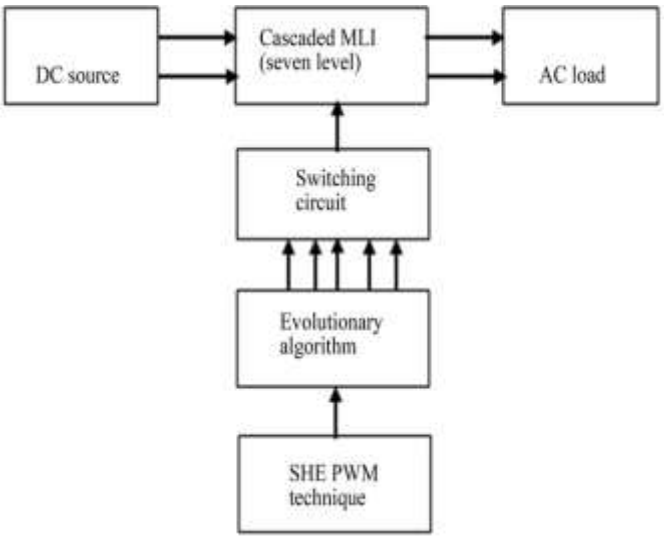

Fig 5: Unsymmetrical seven level inverter BLCOK diagram

5.1 Experimental setup

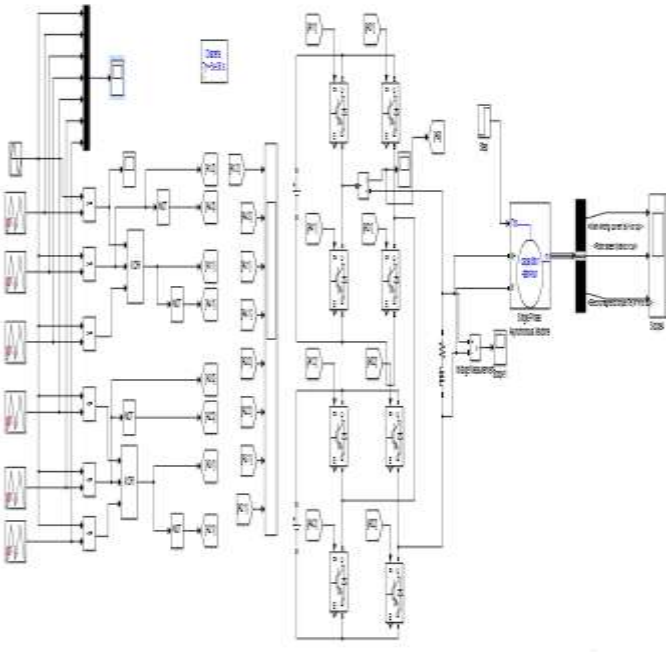

Fig 6: Simulation diagram of proposed 7-level multilevel inverter with induction motor

Figs. 5-6 show the phase voltage, load current, motor speed, torque, rotor current & THD of a seven-level inverter. Table 5 represents various parameters used during simulation of seven level inverter. The current waveforms are closed to sinusoidal. Fig 4.8 represents the Total harmonic distortion graph analysis of a proposed seven level inverter. In this case, the Total Harmonic Distortion is 1.83%.

6. SIMULATION RESULTS

The performance analysis has been carried using a single phase induction motor and unsymmetrical inverter has been used for analysis. The parameters of the motor are specified in Table number 2.

Table no.2 Switching pattern for unsymmetrical cascaded 7 level inverter.

The output voltage waveform and phase current of seven level Unsymmetrical cascaded MLI with capacitor start-run induction motor load for 4 cycles is shown in fig.6. and its FFT analysis is shown in fig.8. The same waveform of nine level unsymmetrical cascaded MLI with capacitor start-run induction motor load for 4 cycles is shown in fig.7. and its FFT analysis is shown in fig.10

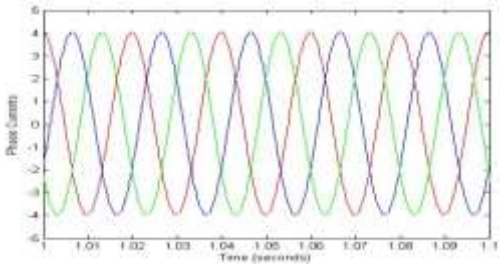

Fig 7: Output Current of 7-level inverter

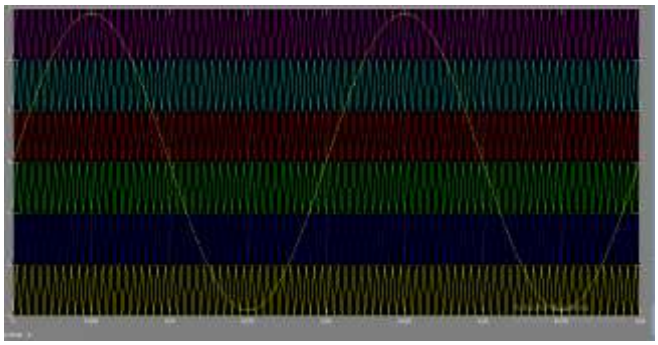

Fig 8: Simulation results of reference and carrier waveform for seven-level MLI

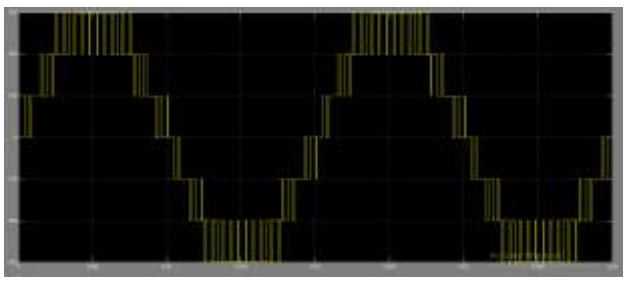

Fig 9: Simulation results of proposed system 7- level inverter for voltage with respect to time

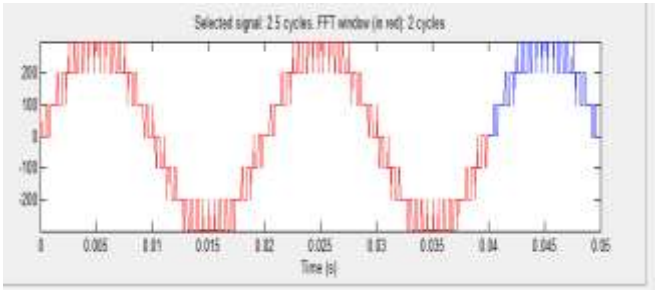

Fig 10: FFT diagram for two cycles for seven level inverter

Main concern of any multilevel inverter is to reduce total harmonic distortion; following is the graph showing a comparative reduction in total harmonic distortion by using phase disposition modulation technique

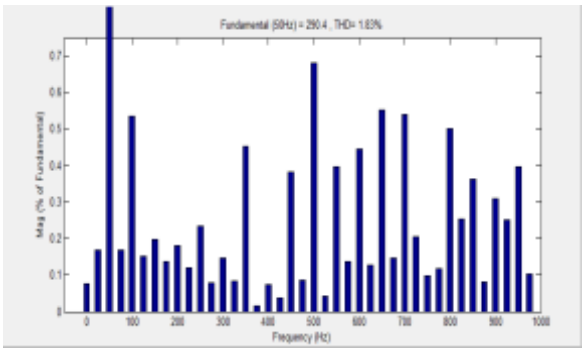

Fig 11: THD for output voltage of basic seven-level cascaded H-bridge inverter

Performance parameters of induction motor-

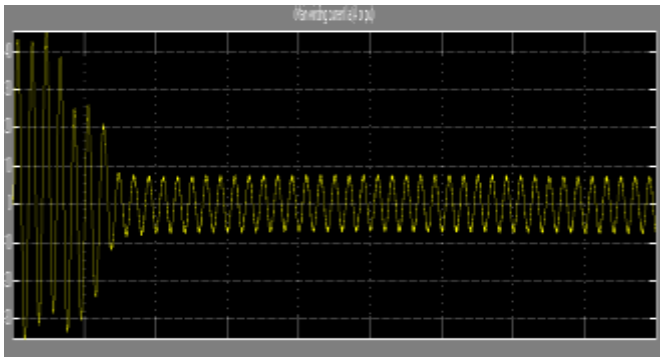

Fig 12: Main winding current of single phase induction motor

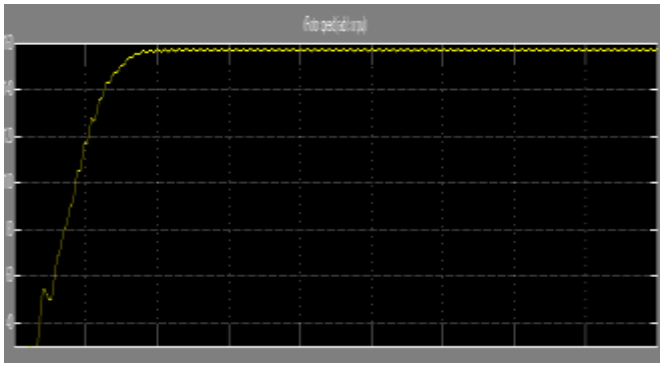

Fig 13: Speed of single phase induction motor

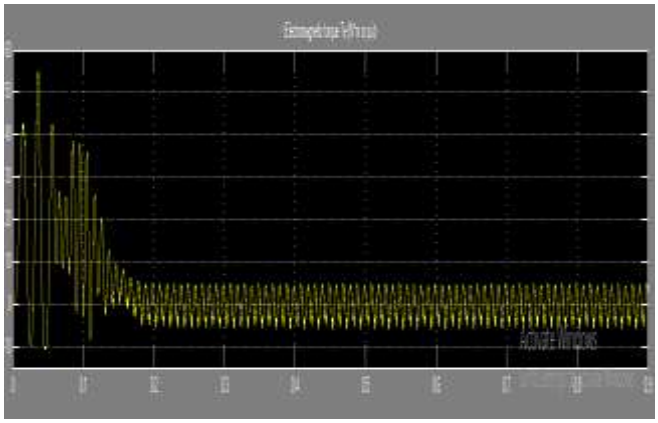

Fig 14: Torque of single phase induction motor for seven level inverter

The value of steady state and THD of the output voltage of 7 level unsymmetrical cascaded MLI is compared with the same output waveform of 9 level unsymmetrical cascaded MLI is shown in Table no.3. The variation of motor parameter of 7 level unsymmetrical cascaded MLI is compared with the 9 level unsymmetrical cascaded MLI is shown in Table no.4.

Table no. 3: Steady state value for Induction Motor

MLI	Main Winding Current	Rotor Speed	Electromagnetic torque	THD
7 Level	0.18 Sec	0.2 Sec	0.18 Sec	4.15 %
9 Level	0.13 Sec	0.15 Sec	0.13 Sec	1.18 %

Table no. 4: Variation of Induction Motor Parameters

MLI	Main Winding Current	Rotor Speed (rad/sec)	Electromagnetic torque
7 Level	+7 to -7	153	+5 to -3
9 Level	+8 to -8	158	+7 to -7

All simulation results are shown in above table no. 3 and table no. 4 respectively.

FUTURE WORK

This Thesis has covered some of the challenges concerning Multi-level inverter, as well as some concerns regarding induction motor drive using multilevel inverter.

- ne of the major applications of multilevel inverter is that it can be used in induction motor drive.
- ore numbers of level of a multilevel inverter is directly proportional to its complexity which can be studied using fault protection method.
- ue to the increased number of semiconductor devices and passive components: how to implement a fault protection technique in various faults scenarios remains as a main challenge.
- n industrial applications, how to reduce Total Harmonic Distortion with the increasing no of levels will continue be the main concern as range of power usage, increasing number of levels, consumption is much more in industrial area rather than domestic use.
- Where as in MLI use of more number of switches results in more power consumption so quality improvement is another concern.
- n other phase focus on modulation technique's effective usage will be other concern as it plays an important role in THD reduction.

So the following areas are under matter of concern for further research for comparative study of further improvement

7. CONCLUSION

The paper deals with a comparison of cascaded 7 level and 9 level multilevel inverter for Asynchronous motor. Indeed, unsymmetrical 7 level and 9 level multilevel inverter have been compared in order to find an optimum motor speed, torque and main winding current with lower switching losses, Total harmonic distortion and optimized output voltage quality. The steady state condition of motor output has reached earlier in case of unsymmetrical cascaded 9 level inverter as compared to 7 levels MLI.[9] The simulation result shows that the unsymmetrical 9 level multilevel inverter provides nearly sinusoidal output voltage with reduced Total harmonic distortion and optimized motor output. In addition unsymmetrical 9 level multilevel inverter has less switching losses with improved output voltage quality.

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