Comparison of Power Dissipation in inverter using SVL Techniques

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Abstract - *As technology scales the size of chip, leakage power has become a important component in chip design. Leakage power is an essential parameter to be taken into account while designing low power devices .Large amount of leakage power is an serious & undesirable factor in portable electronics devices. High power consumption raises the cost and also reduces the battery life of the devices. So it is essential to reduce the dynamic as well as the static power consumption. Increasing the threshold voltage reduces the leakage power of the circuit. Low energy consumption in devices requires very low power circuits. This paper compares the inverter circuits i.e static CMOS inverter & Domino inverter with Upper & lower Self controllable Voltage Level (SVL). Power Consumption & power Dissipation of Upper SVL Domino circuit is found to be less . As power dissipation is reduced , consequently there must be a reduction in leakage power. All the simulations have been carried out in Microwind tool at 90 nm technology , Vdd Supply of 1.2 volt is given , input sequence used is 01010.The other name of Self controllable Voltage Level is Adaptive voltage level circuit (AVL).*

Key Words: Static CMOS, USVL (upper selfcontrollable voltage level) ,LSVL (lower self controllable voltage level), Leakage current, Power dissipation.

1. INTRODUCTION

The latest trends in VLSI technology needs a reduction in power supply voltage (Vdd) to reduce dynamic power in deep sub-micron (DSM) regimes. However, a reduction in Vdd decreases the threshold voltage (Vth). This reduction in Vth causes the leakage currents to increase exponentially and they become a important contributor to total power dissipation in VLSI chips. The subthreshold leakage current I_{leak} is given by the expression

$$I_{leak} = I_0 \exp[(Vgs - Vth)/nVT] \quad \text{--- (1)}$$

where $I_0 = \mu_0 C_{ox} (W/L) V^2$ e1.8,

C_{ox} = gate oxide capacitance, (W/L) = width to length ratio of the leaking MOS transistor., μ_0 = zero bias mobility, Vgs = gate to source voltage, V_T = thermal voltage which is about 26mV at temperature T= 300K and n is the subthreshold swing coefficient given by 1 +(C_d/C_{ox}) where C_d is the depletion layer capacitance of the source/drain junction. The equation (1) says that the leakage current is exponentially proportional to (Vgs -Vth), Which implies leakage can be reduced by increasing Vth or reducing Vgs. Domino logic is one of the effective circuit configurations for implementing high speed logic designs. Domino circuits provide the advantages of faster transition and glitch-free operation.

1.1 DOMINO LOGIC

Dynamic circuits such as domino logic circuits are used in high performance microprocessors for obtaining high speeds that are not possible with static CMOS circuits . Their high speed is due to reduced input capacitance, small switching thresholds and circuit implementations that typically use fewer levels of logic due to the usage of efficient and wide complex logic gates. But the penalty to be paid for speed improvement is the increased power dissipation, mainly due to the necessary clocking and increased noise sensitivity. Hence, this imposes the challenges in the design of dynamic circuits.

1.2. DOMINO INVERTER

Domino style incorporates clk inputs to all gates.The operation of these gates is divided into 2 phases. The phases are precharge & evaluation . In the precharge phase gate outputs are charged to high level voltage because PMOS transistors are controlled by clock input which in this phase is low .In the evaluate phase, the outputs of the gate can conditionally change to low voltage level. The logic of the gate is implemented only with NMOS transistors those transistors dictate if the outputs will be connected to the low voltage level to be discharged or not.Here Domino Inverter is implemented in 90 nm technology using Microwind. When clkdata is low ,in precharge state Pmos1 conducts output is driven depending on clk data i.e pmos2 conducts so output is charged to Vdd, in evaluate phase clock1 is high so nmos2 conducts & nmos1 doesn't conduct so out1 retains the charge. When clkdata is high nmos1 conducts ,in precharge phase pmos1 conducts, so output is reduced as it discharges since pmos2 is off & in evaluate phase nmos2 conducts so output is pulled down to 0.The schematic diagram is shown in fig 2 .Vdd Supply of 1.2 volt is given, input sequence is 01010.

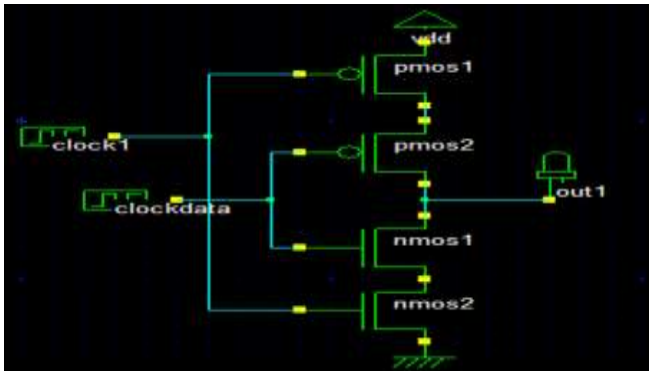

Figure -1: A Domino Logic inverter Circuit

2. SELF CONTROLLABLE VOLTAGE LEVEL

SVL stands for Self controllable Voltage Level. Self controllable voltage level (SVL) is technique for leakage reduction within the device. SVL is a technique which can be set either at the top of the load circuit, or bottom of the load . Upper self controllable voltage level (USVL) technique is applied to reduce the supply voltage and Lower self controllable voltage level (LSVL) system is utilized to boost up the ground node voltage.

2.1 LOWER SELF CONTROLLABLE VOLTAGE LEVEL (LSVL)

An LSVL circuit in general, consists of a single NMOS switch and m weakly connected nMOS switches connected in series which increases the source voltage appearing across the load circuit in active mode. Here m=2 is considered. A negative control signal (clk2) turns on pmos_3 & pmos_2 and turns off nmos_1. so that *VS* is supplied to the stand-by inverter through *2* p-SWs.The on-NMOS switch connects the load circuit and Vss in the sleep mode on request whereas the weakly-on PMOS transistors connect the load circuit and Vss in the active mode. Source voltage (*VS*) is increased by *mv*, so the substrate bias (i.e., back-gate bias) (*V*sub), expressed by

$$Vsub = - mv \quad ----(2)$$

$$Vs=Vss+2v \quad ----(3)$$

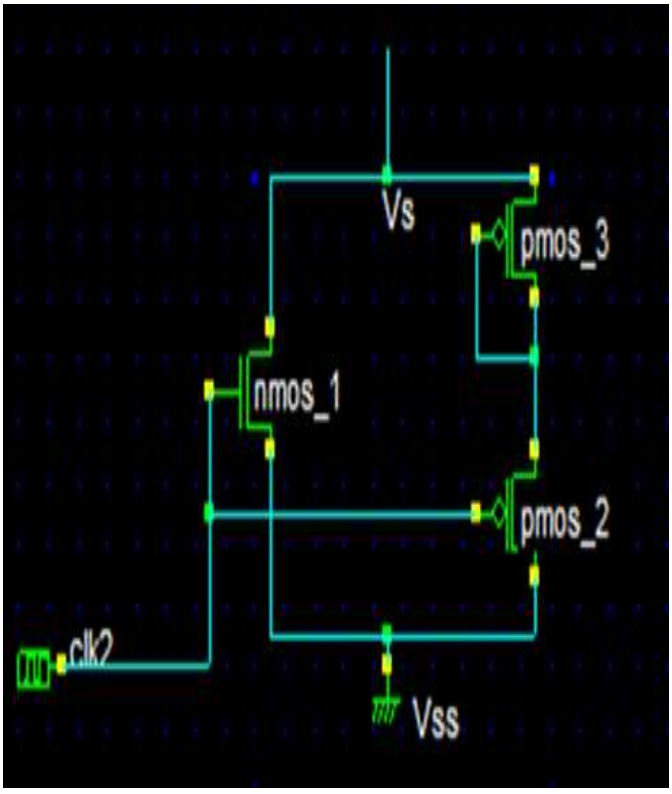

Figure -2: Lower Self controllable Voltage Level Circuit

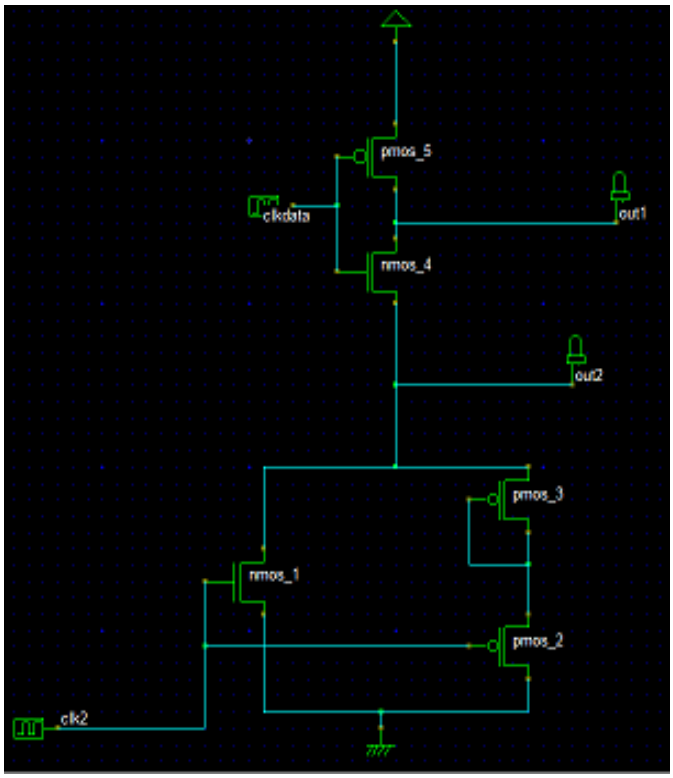

Figure -3: Lower Self controllable Voltage Level Circuit with static cmos inverter as load

2.2 UPPER SELF CONTROLLABLE VOLTAGE LEVEL

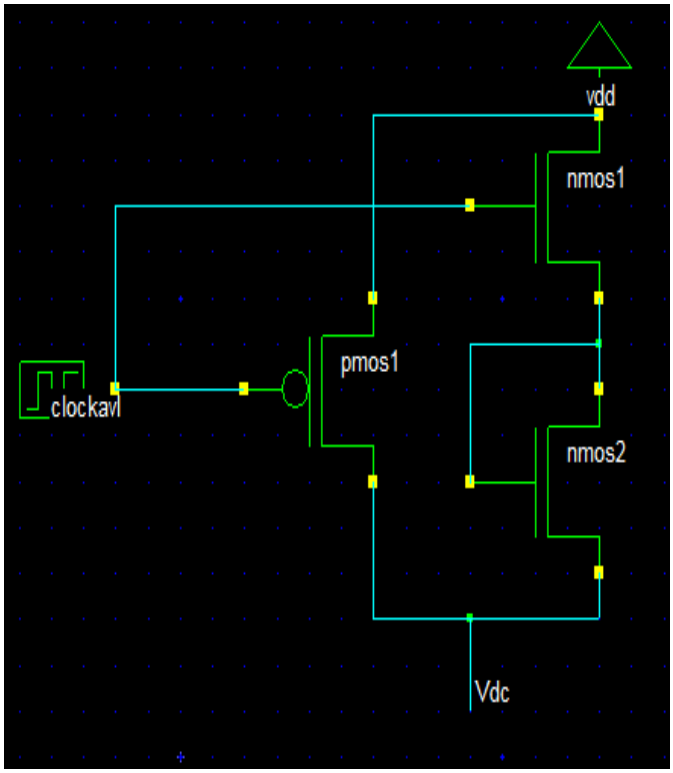

Figure- 4: Upper Self controllable Voltage level

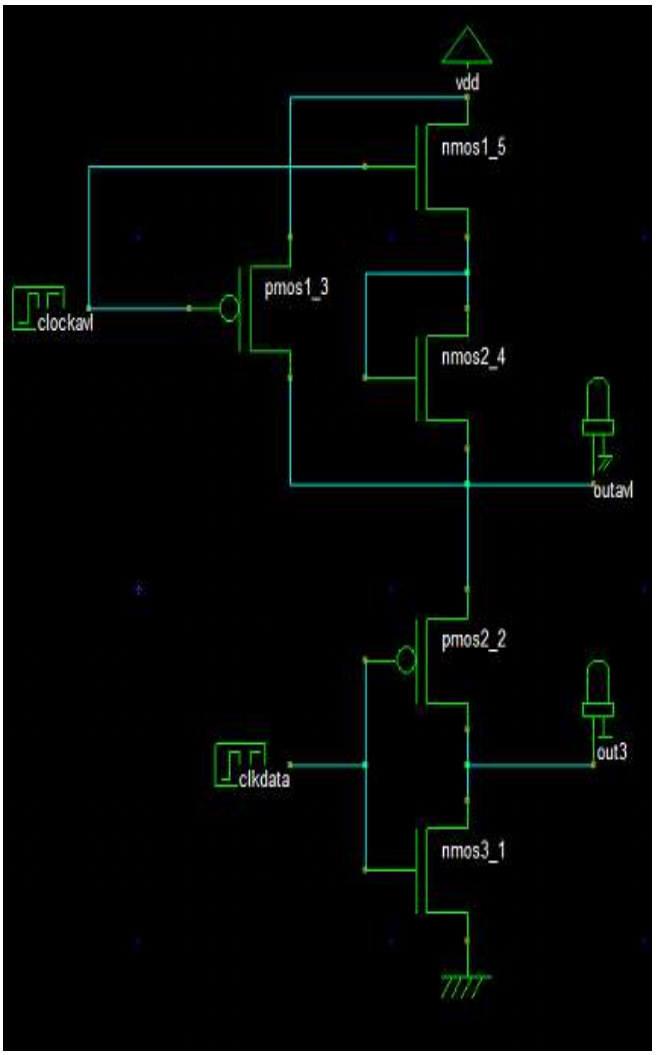

Figure-5: Upper Self controllable Voltage level with static cmos inverter as load

An USVL circuit, in general, consists of a single PMOS switch and m weakly connected nMOS switches connected in series.Here m=2 is considered. When gate voltage of standby inverter is "0" ,pmos2-2 is turned on & nmos3_1 is turned off. When clockavl turns on nmos1_5 , nmos2_4 & turns off pmos1_3, Vdd is supplied to inverter through 2 nmos.

Now, the drain volltage of off nmos is

$$Vdsn = Vdc - 2v \qquad \text{-----(4)}$$

v is voltage drop in single nmos.Hence, Vdsn is reduced which in turn increases the barrier height of the off-Nmos. Therefore Drain Induced Barrier Lowering (DIBL) effect is reduced and therefore the threshold voltage of the nMOS transistor is increased. This results in a decrease in sub-threshold leakage current of the nMOS transistor in the load circuit.

2.3 LOWER SELF VOLTAGE LEVEL CIRCUIT WITH DOMINO INVERTER AS LOAD

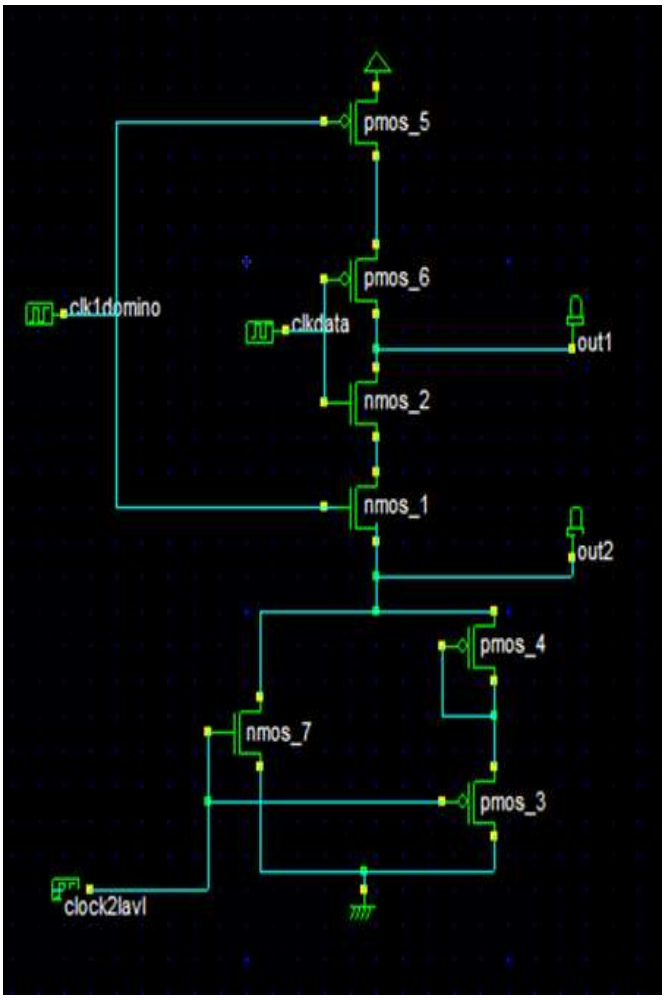

Figure -6: Lower Adaptive Voltage Level Circuit with Domino Inverter as load

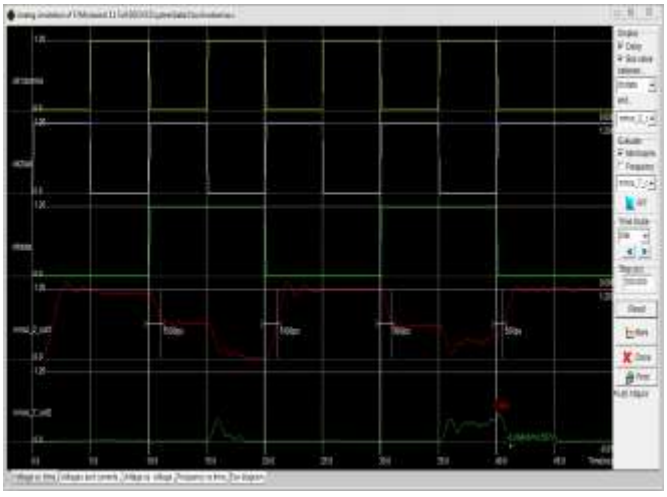

Figure -7: Voltage waveforms & power consumption Lower Adaptive Voltage Level Circuit with Domino Inverter as load

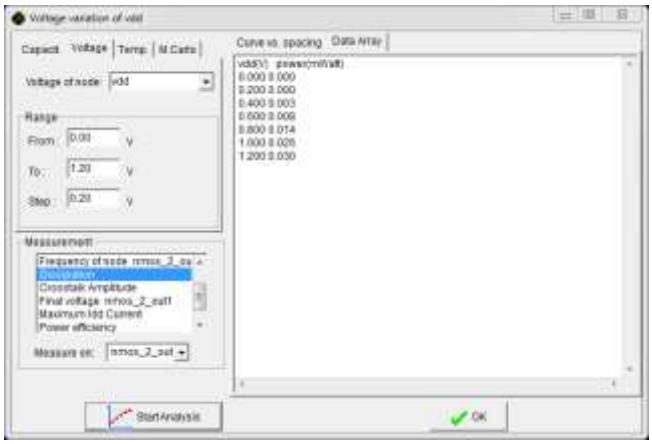

Figure -8: Power dissipation of Lower Adaptive Voltage Level Circuit with Domino Inverter as load

2.4 UPPER ADAPTIVE VOLTAGE LEVEL CIRCUIT WITH DOMINO INVERTER AS LOAD

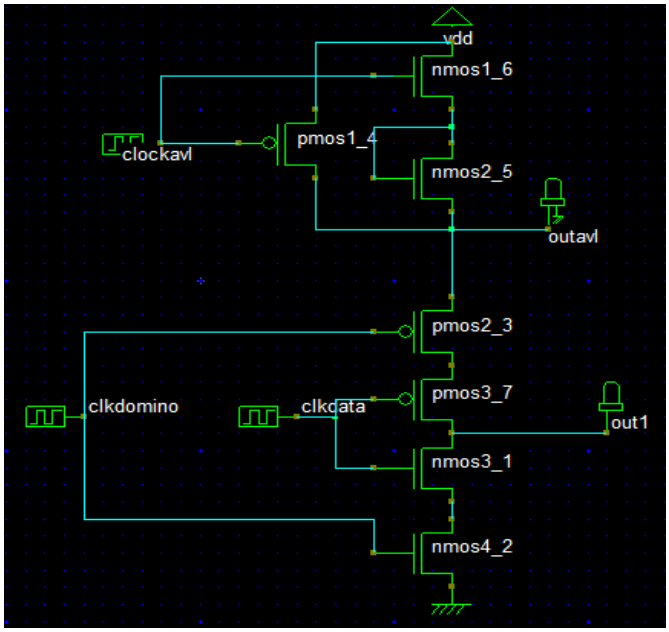

Figure -9: Upper Adaptive Voltage Level Circuit with Domino Inverter as load

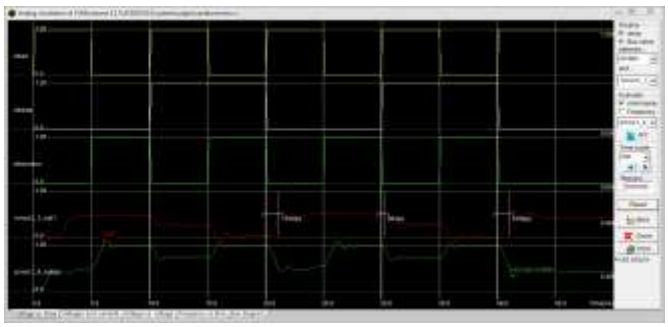

Figure -10: Voltage waveforms & power consumption Upper Adaptive Voltage Level Circuit with Domino Inverter as load

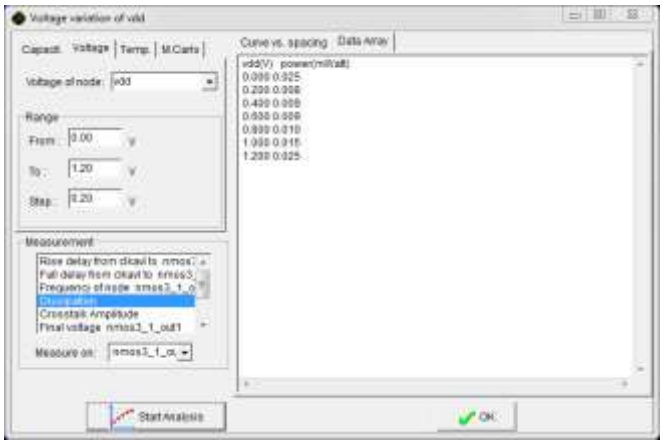

Figure -11: Power dissipation of Upper Adaptive Voltage Level Circuit with Domino Inverter as load

TABLE-1: SIMULATION RESULTS

Parameters	Power Consumption (µW)	Power Dissipation (mW)	Iddavg (mA)	Voltage at node between load & loadVs (V)	Delay (ps)
INVERTER	39.254	0.039	0.033	Vss	900
LSVL with static CMOS inverter	38.160	0.038	0.032	0.722	1000
USVL with static CMOS inverter	28.440	0.028	0.024	0.546	1000
DOMINO INVERTER	34.513	0.035	0.029	Vss	1050
LSVL with Domino inverter	30.156	0.030	0.025	0.463	1000
USVL with Domino inverter	25.167	0.025	0.021	0.401	700

3. CONCLUSION

The simulation results reveal that Upper SVL with Domino inverter has less power consumption of 25.167 µW which is 35.88 % less than Static CMOS inverter.Power Dissipation is 0.025mW in Upper SVL with Domino inverter which is 35% less than Static CMOS inverter. Propagation Delay is also less i.e 700 ps.Domino inverter with USVL is better in performance than with LSVL . So it can be concluded that USVL is better choice.

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BIOGRAPHY

K. Kalai Selvi completed M.E in Optical Communication at Alagappa Chettiar College of Engineering & Technology, Anna University. Working as Assistant Professor in Government College of Engineering ,Tirunelveli, Tamil Nadu. Has 12 years of teaching experience.