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High Step-Up DC-DC Converter Based on Voltage Multiplier Cell and Voltage-Stacking Techniques for Renewable Energy Applications

S. KARTHICK[1], K. HARI[2]

[1,2]Assistant Professor, Department of Electrical and Electronics Engineering, Muthayammal engineering college, Tamilnadu, India.

Abstract - *A novel interleaved high step-up DC-DC converter based on voltage multiplier cell and voltage-stacking techniques is proposed for the power conversion in renewable energy power systems. The circuit configuration incorporates an input-parallel output-series boost converter with coupled inductors, clamp circuits and a voltage multiplier cell stacking on the output side to extend the voltage gain. The converter achieves high voltage conversion ratio without working at extreme large duty ratio. The voltage stresses on the power switches are significantly lower than the output voltage. As a result, the low-voltage-rated metal-oxide-semiconductor field-effect transistors (MOSFETs) can be employed to reduce the conduction losses and higher conversion efficiency can be expected. The interleaved operation reduces the input current ripple. The leakage inductances of the coupled inductors act on mitigating the diode reverse recovery problem. The operating principle, steady-state analysis and design guidelines of the proposed converter are presented in detail. Finally, a 1-kW prototype with 28-V input and 380-V output voltages was implemented and tested.*

Key Words: H**igh step-up DC-DC converter; interleaved operation; coupled inductor; voltage multiplier cell**.

1. INTRODUCTION

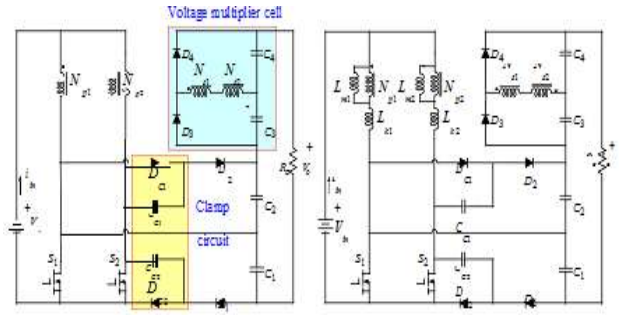
Nowadays, demand for clean or renewable energy sources has dramatically increased with population growth and the depletion of fossil fuel. Much effort has been made to explore renewable energy sources, such as photovoltaic (PV), fuel cell and wind energy systems. The renewable energy grid-connected system with PV and fuel cells calls for high voltage-gain and high-efficiency dc-dc converters because the low voltage generated by the PV and fuel cells needs to be raised to a high voltage for the input of grid-connected inverter. If the energy needs to be converted to a single-phase 220 V ac voltage utility grid, a 380–400 V dc bus voltage is required for the inverter. However, the outputs of PV and fuel cells are generally lower than 40 V due to safety and reliability considerations in home applications. Thus, a front-end DC-DC converter with about ten times voltage gain is satisfy the requirement.

Converter can be employed with operating an extreme large duty ratio. However, it causes several problems of high switching losses, severe output diode reverse-recovery losses, and electromagnetic interference (EMI). Furthermore, for a high output-voltage converter, therefore, the high-voltage rated MOSFETs and diode with large conduction resistance are necessary due to the voltage stresses non the power devices are equal to the output voltage. It will result in large conduction and switching losses. In practice, the voltage gain of boost converters is limited due to the parasitic parameters effect. These problems are the main limitations of disadvantages for the boost converter.

For coupled inductor-based converters the high voltage gain can be achieved by adjusting the turns ratio of the coupled inductor and duty ratio. However, the power loss and high voltage stress on the power switches occur owing to the leakage inductance of the coupled inductor. The switched-capacitor converters can also obtain high voltage conversion ratio. However, many switches are required for these converters, and thus it leads to complexity of design for the driving circuit. The high step-up converters without a coupled inductor or transformer are proposed in Several kinds of interleaved high step-up converters with voltage multiplier cells have been proposed in the interleaved converters with three-winding coupled inductors are proposed to achieve high voltage conversion ratio and low input current ripple. However, they are a little complex and difficult to design, which results in the circuit complexity and cost problem.

1.1 Proposed Converter and Operating Principle

The proposed converter circuit is shown in figure 1a, where s1 and s2 are the power switches, Dc1 and Dc2 are the clamp diodes, Cc1 and Cc2 are the clamp capacitors, D1and D2 are the output diodes, C1 and C2 are the output capacitors, 3 D and 4 D are the switched diodes, C3 and C4 are the switched capacitors, and o R is the load. There are two coupled inductors in the proposed converter. The coupling references are marked by "." and "∗". The circuit model of each coupled inductor includes an ideal transform



(a) **(b)**

Figure1. Proposed converter and its equivalent circuit. (a) Proposed converter; (b) Equivalent circuit.

are the primary and secondary windings of the coupled inductors, respectively, and the turns ratio of the coupled inductor is defined as n = Ns1 / Np1= Ns2 / Np2 . The dual passive clamp circuits are used to recycle the leakage energy and suppress the turn off voltage spikes on the power switches. The voltage multiplier cell is realized by the secondary windings of the coupled inductors with series connection, the switched diodes and the switched capacitors to increase the voltage gain.

In the operational analysis, the proposed converter operates in continuous conduction mode(CCM), and the gate signals of the power switches are interleaved with the same duty ratio greater than 0.5 and a 180o phase shift. The key waveforms are shown in Figure 2. There are six operating modes in one switching period. The equivalent circuits for each mode are shown in Figure 3. Mode 1 [0 1 t , t]: At t = t0 , the power switch S1 is turned on, and the power switch 2 S remains in the turn-on state. The leakage current Lk1 i rises quickly and its increasing rate is limited by k1 L . The magnetizing inductance m1 L still transfers energy to the secondary side of the coupled inductors charging the switched capacitor 3 C . The diodes 1 D , 2 D , 4 D , C1 D and C2 D are reverse-biased, and only the switched diode 3 D is conducting as shown in Figure 3a. The current falling rate through the switched diode 3 D is controlled by the leakage inductances k1 L and k 2 L , which alleviates the diode reverse recovery problem. This mode ends when the current through the diode 3 D decreases to zero at the instant t1 , and the diode 3 D is turned off automatically. At the same time, the current through k1 L becomes equal to that of the magnetizing inductance m1 L .

Mode 2 [1 2 t , t]: During the time interval, both the switches 1 S and 2 S conduct, and all diodes are reverse-biased as depicted in Figure 3b. The magnetizing inductances Lm1 and Lm2 as well as the leakage inductances Lk1 and Lk2 are linearly charged by the input voltage Vin. This mode ends at the instant t2, when the switch S2 is turned off.

Mode 3 [t2, t3]: At t = t2, the switch S2 is turned off, which makes the diodes DC2 and D2 turn on due to the continuity of the leakage current iLk2. The switch S1 remains in the turn-on state, as shown in Figure 3c. The energy kept by the magnetizing inductance Lm2 is transferred not only to the secondary side of the coupled inductors but also to the output capacitor C2 and the clamp capacitor CC2. The current through Lk2 decreases and flows through two paths. One path is through CC1, D2, C2 and S2, so that the clamp capacitor CC1 is discharged and the output capacitor C2 is charged. The other path is through CC2 and DC2, so that the clamp capacitor CC2 is charged. This mode ends when S2 is turned on. Energies 2018, 11, x FOR PEER REVIEW 4 of 16 the leakage inductances k1 L and k 2 L are linearly charged by the input voltage Vin . This mode ends at the instant t2 , when the switch 2 S is turned off.

Mode 3 [2 3 t , t]: At 2 t = t , the switch 2 S is turned off, which makes the diodes C2 D and 2 D turn on due to the continuity of the leakage current Lk 2 i . The switch 1 S remains in the turn-on state, as shown in Figure 3c. The energy kept by the magnetizing inductance m2 L is transferred not only to the secondary side of the coupled inductors but also to the output capacitor 2 C and the clamp capacitor C2 C . The current through k 2 L decreases and flows through two paths. One path is through C1 C , 2 D , 2 C and 2 S , so that the clamp capacitor C1 C is discharged and the output capacitor 2 C is charged. The other path is through C2 C and C2 D , so that the clamp capacitor C2 C is charged. This mode ends when S2 is turn on.

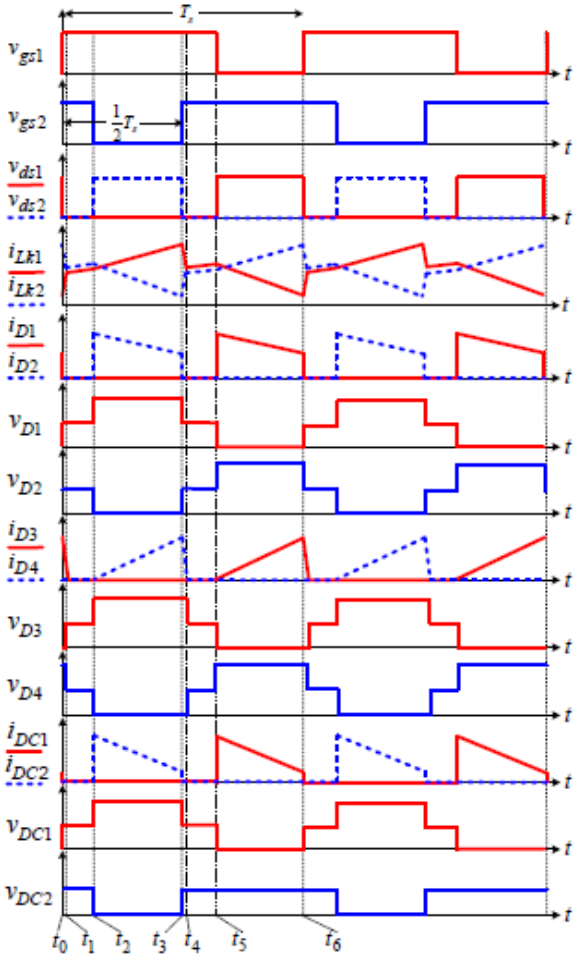


Figure 2. Key waveforms of the proposed converter.

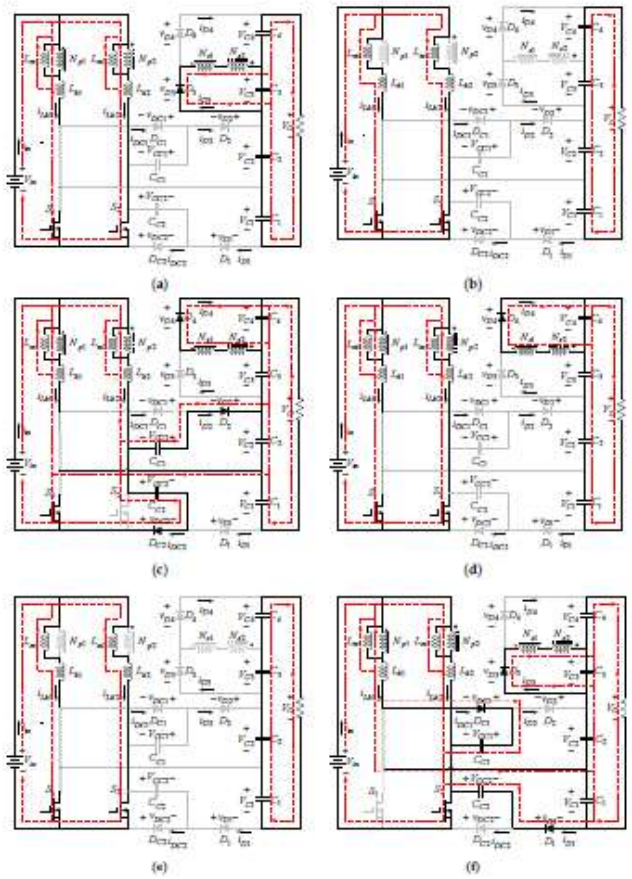


Figure 3. Operating modes of the proposed converter. (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4;(e)Mode 5; (f) Mode 6.

Mode 4 [t3, t4]: At t = t3, the power switch S2 is turned on, and the power switch S1 remains in the turn-on state. The diodes D1, D2, D3, DC1 and DC2 are reverse-biased, and only the switched diode D4 is conducting as shown in Figure 3d. The current through the leakage inductance Lk2 rises quickly, and the current through the leakage inductance Lk1 falls quickly. The stored energy in the magnetizing inductance Lm2 still transfers to the secondary side of the coupled inductors charging the switched capacitor C4. As the current through the leakage inductance Lk2 increases, the secondary side current of the coupled inductors decreases. The of the current through the switched diode D4 decreases and its falling rate controlled by the leakage inductances Lk1 and Lk2, which alleviates the diode reverse recovery problem. This mode ends when the diode current iD4 decreases to zero at t = t4, and D4 is turned off automatically. At the same time, the current through Lk2 becomes equal to that of the magnetizing inductance Lm2.

Mode 5 [t4, t5]: The operating state of modes 5 and 2 are similar. During this interval, all diodes are turned off, as shown in Figure 3e. The magnetizing inductances Lm1 and Lm2 as well as the leakage inductances Lk1 and Lk2 are charged linearly by the input voltage Vin. This mode is terminated as the switch S1 is turned off.

Mode 6 [t5, t6]: The switch S1 is turned off at t = t5, which turns on the diodes DC1 and D1. The switch S2 remains in turn-on state. The current-flow path of this mode is shown in Figure 3f. The energy stored in the magnetizing inductance Lm2 begins to transfer to the secondary side of the coupled inductors charging the switched capacitor C3 via the switched diode D3. The current through the diode D3 is controlled by the leakage inductances Lk1 and Lk2. The leakage current iLk1 decreases and flows to the clamp capacitor CC1 via DC1 and S2, meanwhile it flows to the output capacitor C1 and the clamp capacitor CC2 via D1 and S2. The time t6 is the ending of a switching period Ts when the power switch S1 is turned on again.

1.2. Steady-State Analysis and Design Guidelines

In order to simplify the performance analysis of the proposed converter, the following assumptions are made.

(1) Voltages on the capacitors are regarded as constant over one switching period due to their sufficiently large capacitances.
(2) All of the power devices are ideal. The on-resistance Rds(ON) and parasitic capacitances of the power switches are ignored, and the forward voltage drops of the diodes are neglected.
(3) The leakage inductances of the couple inductors are much smaller than the magnetizing inductances, and, therefore, they are neglected.
(4) The switching period is Ts. The power switches operate with the same duty ratio D and 180_ out of phase.

1.2.1. Voltage Gain

Since the time intervals of modes 1 and 4 are very short, only modes 2, 3, 5 and 6 were considered for the steady-state analysis. Based on the operating principle discussed in the aforementioned section, the charging voltage of the magnetizing inductance Lm is the input voltage Vin during the switch is in the turn-on state for time DTs, and the discharging voltage is the clamp voltage VCC1 or VCC2 minus the input voltage Vin during the switch is in the turn-off state for time (1- D)Ts. By applying the voltage-second balance to the magnetizing inductance, the voltages on the clamp capacitors CC1 and CC2 can be calculated analogously to the output voltage of the conventional boost converter, which can be derived from

$$VCC1 = VCC2 = 1/1\text{-}D\ Vin \qquad (1)$$

At modes 3 and 6, the voltages on the output capacitors C2 and C1 can be derived from Figure 3c,f, respectively. They can be expressed as

$$VC2 = VCC1 + VCC2 = 2/1\text{-}D\ Vin, \qquad (2)$$
$$VC1 = VCC1 + VCC2 = 2/1\text{-}D\ Vin \qquad (3)$$

Moreover, the voltage on the switched capacitors C4 and C3 can also be derived from Figure 3c,f,respectively. The results are given by

$$V_{C4} = nV_{in} - n(V_{in} - V_{CC2}) = n/1\text{-}D\ V_{in}, \quad (4)$$
$$V_{C3} = nV_{in} - n(V_{in} - V_{CC1}) = n/1\text{-}D\ V_{in}, \quad (5)$$

From Figure 3b,e, it can be found that the output voltage is the sum of VC1, VC2, VC3 and VC4. With the results of Equations (2)–(5), the output voltage can be derived from

$$V_o = VC1 + VC2 + VC3 + VC4 = 2n + 4/1\text{-}DVin. \quad (6)$$

Therefore, the voltage gain of the proposed converter is given by

$$Vo/Vin = 2n + 4/1 - D. \quad (7)$$

Equation (7) confirms that the proposed converter has a high step-up voltage gain without adopting an extremely large duty ratio. The curve of the voltage gain related to the turns ratio of the coupled inductor n and duty ratio D is shown in Figure 4. As the turns ratio of the coupled inductors increases, the voltage gain is extended significantly. When the duty ratio is only 0.6, the voltage gain reaches 15 with the turns ratio n = 1.

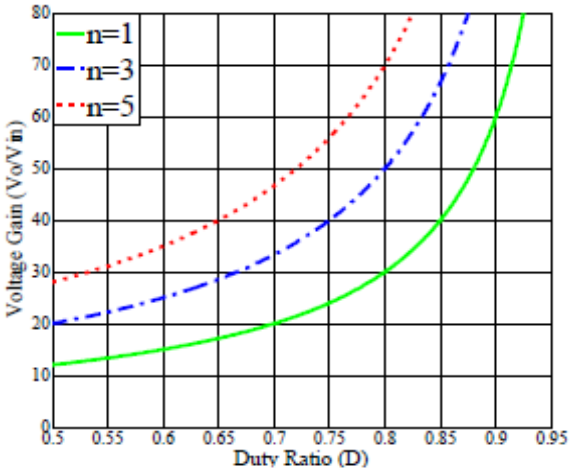


Figure 4. Voltage gain of the proposed converter verse duty ratio for several turns ratio n.

2. Experimental Verifications

To validate the performance and effectiveness of the proposed converter, a 1000 W laboratory prototype with 28-V input and 380-V output voltages was built and tested with the specifications and prototype with 28-V input and 380-V output voltages was built and tested with the specifications and parameters. The experimental results shown in the Figures 5-9 are measured under full-load conditions 1000 W. Figure 5 shows t waveforms of the interleaved PWM signals vgs1 and vgs2, the input voltage Vin = 28 V and the output voltage Vo = 380 V. The duty ratio is about 0.58. Thus, the high step-up voltage gain is realized without operating at an extremely large duty ratio. The waveforms of gate signals and the drain-source voltages vds1 and vds2 are shown in Figure 6. It can be seen that the voltage stresses on the power switches are about 63 V, which is only one-sixth of the output voltage. Thus, one can adopt low-voltage-rated devices to reduce the conduction and switching losses.

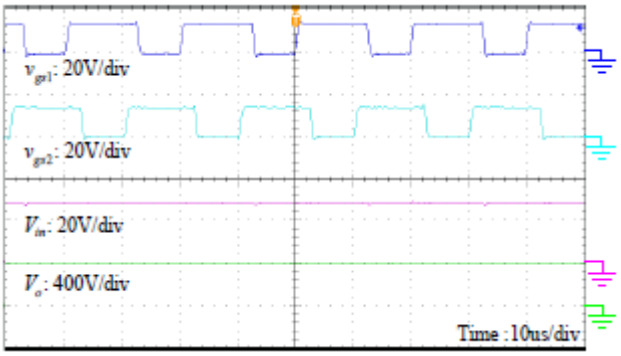


Figure 5. Measured waveforms of the gating signals and the input and output voltages.

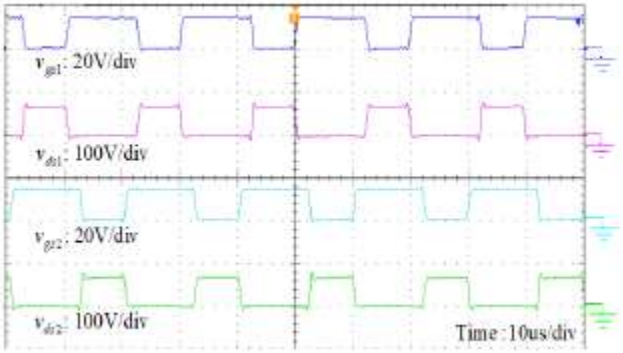


Figure 6. Measured waveforms of the gating signals and the drain-source voltages of power switches.

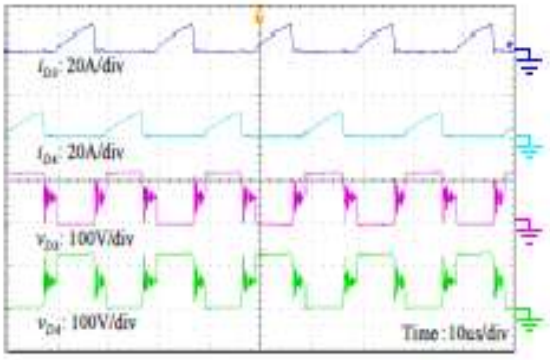


Figure 7. Measured waveforms of the voltages and currents on the switches diodes.

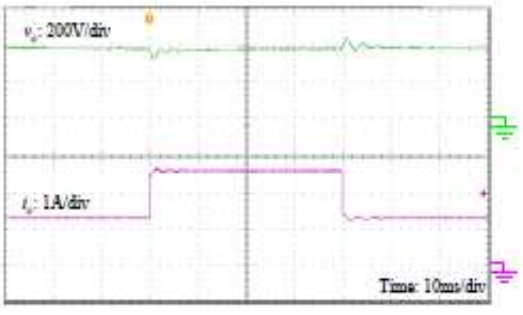


Figure 8. Output voltage response with step load change.

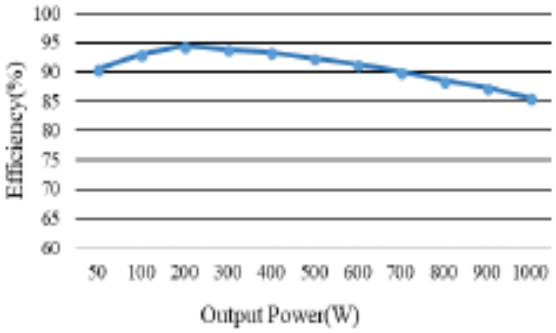


Figure 9. Experimental conversion efficiency of the implemented converter.

In order to obtain a regulated and constant output voltage in spite of input voltage variation and output load disturbance, the closed-loop control with type III compensator is implemented. There are three poles (one at the origin) and two zeros provided by this compensation. The experimental result under the step load change from half load 500 W to full load 1000 W and vice versa is illustrated in Figure 8. It can be seen that the transient voltage ripple of the output voltage is small and insensitive to the load change. This means that the compensator design can deliver a dynamic performance. The experimental conversion efficiency of the presented converter is given in Figure 9, which is measured by the power analyzer (HIOKI 3390). The full-load efficiency is about 86% and the peak value of efficiency is 94.5% obtained at the output power of 200 W.

3. CONCLUSION

A new interleaved high step-up DC-DC converter based onm voltage multiplier cell and voltage stacking technique is proposed. The high step-up voltage conversion can be achieved without working at extremely large duty ratio. The switch voltage stress is much lower than the output voltage such that the low-voltage-rated power devices with low on-resistance can be adopted to reduce the conduction losses. Dual passive clamp circuits help to recycle the leakage energy of the coupled inductors and clamp the voltage stress of the switches to a lower level. The interleaved operation reduces the input current ripple. The diode reverse-recovery problem is alleviated by the leakage inductances of the coupled inductors for most of the diodes. The operating principle, the steady-state analysis and design guidelines of the proposed converter are presented. Finally, a 1000 W prototype converter was built and tested to validate the converter's performance.

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