OPTIMAL CONTROL OF MULTILEVEL INVERTER TO MINIMIZE HARMONIC DISTORTION IN PHOTOVOLTAIC POWER GENERATING ARRAY

SHARAD CHANDRA RAJPOOT[1], ISWAR PRASAD PATEL[2], DEMAN KOSALE[3], PRASHANT SINGH RAJPOOT[4]

[1]Assistant professor (EE) G.E.C. Jagdalpur, Bastar, Chhattisgarh, India,
[2]M-tech scholar (EE) VEC, Lakhanpur, Ambikapur Chhattisgarh, India
[3]Assistant professor (EE) VEC, Lakhanpur, Ambikapur Chhattisgarh, India
[4]Assistant professor (EE) L.C.I.T., Bilaspur, Chhattisgarh, India,

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Abstract- In the present scenario power becomes major need for human life. Due to day-to-day increase in population and lessen of the conventional sources, it becomes necessary that we must depend on non-conventional sources for power generation. While moving, the vehicles posses some kinetic energy and it is being wasted. This kinetic energy can be utilized to produce power by using a special arrangement called "POWER HUMP". The Kinetic energy of moving vehicles can be converted into mechanical energy of the shaft through rack and pinion mechanism. This shaft is connected to the electric dynamo and it produces electrical energy proportional to traffic density. This generated power can be regulated by using Zener diode for continuous supply. All this mechanism can be housed under the dome like speed breaker, which is called hump.

The generated power can be used for general purpose like streetlights, traffic signals. The electrical output can be improved by arranging these power humps in series this generated power can be amplified and stored by using different electric devices. The maintenance cost of hump is almost nullified. By adopting this arrangement, we can satisfy the future demands to some extent.

Index Terms- speed breaker, controller, commutator, power hump, breaking system, OTEC (ocean thermal energy conversions).

1. INTRODUCTION

1.1 OVERVIEW

Due to the energy shortage, the integration of renewable energy sources to the electricity grid becomes a interesting research topic nowadays. The number of renewable energy sources and distributed generators is increasing very fast which also brings some threats to the power grid. In order to maintain or even to improve the power supply reliability and quality of the power system with distributed generation, it is necessary to have some new strategies for the operation and management of the electricity grid. Modern power electronic technology is an important part in distributed generation and the integration of the renewable energy to the power grid. It is widely used in the grid based system.

Since the output power of micro-sources (photovoltaic, wind energy etc.) is more or less dependent on the environment condition such as irradiance and wind, it is necessary to use some specific control strategies or to have some energy storage system (battery, super-capacitor etc.) in order to compensate for the fluctuations. One traditional way is to use different kind of converters to integrate the micro sources, energy storage and different types of loads into a common DC bus [2], [3], the basic structure is shown in Figure 1.

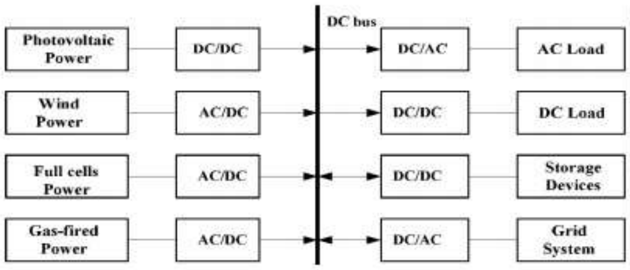

Figure 1. Connection of grid, micro-sources, energy storage systems and load

Some problems with this kind of structure are as follows:

• There are lots of power electronics converters in the system so the harmonics components would be very high, which increases the cost and size of the harmonics filter.

• If the voltage level is very high, the switching stress of the power electronic device would increase.

• The efficiency would be low due to the power losses in different converters.

To overcome the above shortcomings, a modular power electronics technology named multilevel inverter, which is very appropriate for the integrating renewable energy source is proposed in [4], [5]. The core idea of the multilevel inverter is to achieve the desired ac voltage from several levels of dc voltages.

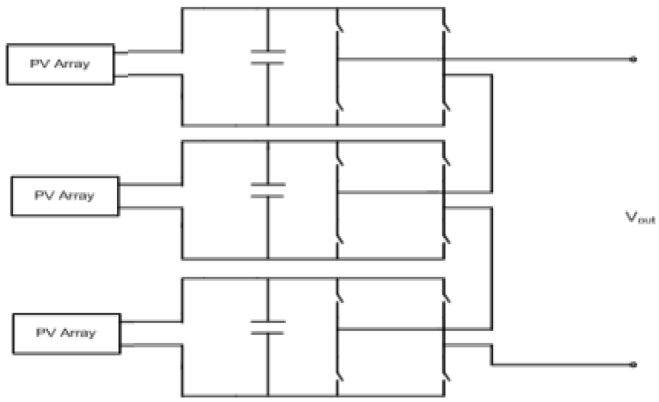

Fig. no. 2 PV array

1.2 Problem identification

Grid connected photovoltaic (PV) power conversion systems are getting more and more attention in the last decade, mainly due to cost reduction of PV modules and government incentives, which has made this energy source and technology competitive among other energy sources [13].

2. PV ARRAY MODEL

The output of the PV system is largely dependent on the outside environment conditions. In order to make the correct analysis of the photovoltaic system, a suitable simulation model must be chosen initially.

3. MATHEMATICAL MODEL

PV arrays consist of series and parallel connected PV modules. For each PV module, there are series and parallel connected PV cells. The PV cell is usually described by the equivalent circuit shown in Figure 3. It can be seen that one current source anti parallel with a diode, a shunt and a series resistance are included in the equivalent circuit [14].

The basic equation for the PV cell can be derived by the Kirchhoff's current law:

$$I = I_{sc} - I_d - I_{sh} \tag{1}$$

The diode current Id and the shunt branch current Ish can be expressed as

$$I_d = I_0\left[\exp\left(\frac{V + IRsr}{nKT_c/q}\right) - 1\right] \tag{2}$$

$$I_{sh} = \frac{V + IR_{sr}}{R_{sh}} \tag{3}$$

In (1), I_{sc} is defined as the photo current. The value of I_{sc} under reference conditions can be obtained by seeing the data sheet of the PV cell. The photocurrent under arbitrary environment conditions can be expressed as:

$$I_{sc} = I_{scR}\frac{R}{R_r}\left[1+\alpha_T(T_c - T_{cR})\right] \quad (4)$$

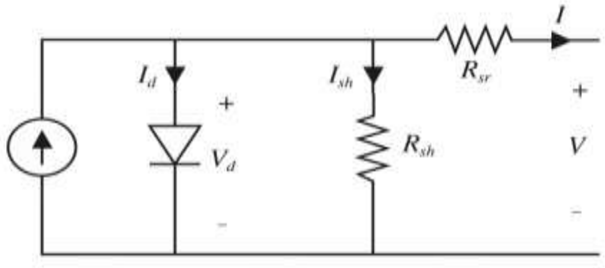

Fig. no. 3 PV cell equivalent

Where I_{scR} is the short circuit current at the reference solar radiation RR and the reference cell temperature which are selected as 1kW/m2 and 25◦C respectively in this thesis. The parameter αT is the temperature coefficient of photo current [14]. And the current Io is the dark current which is only the function of cell temperature:

$$I_0 = I_{oR}\left(\frac{T_c{}^3}{T_{cR}{}^3}\right)\exp\left[\left(\frac{1}{T_{cR}} - \frac{1}{T_c}\right)\frac{qe_g}{nk}\right] \quad (5)$$

In (5), I_{oR} is the reference dark current. The other parameters appeared from (2) to (5) are the electron charge q, the Boltzman constant k, the band-gap energy of the PV cell e_g, and the diode ideality factor n which is used to adjust the characteristic I – V curves. The constants in the above equations can be obtained from the data sheet provided by the manufacturer [14].

Cascaded multilevel inverter with separate dc source is proposed in this thesis for supplying the load with the solar PV panel. It is assumed that with a proper maximum power point algorithm the output of the PV array is a constant DC source and simulation is being carried out for 2 level , 3 level, 5 level and 7 level multilevel inverter and the results are being compared. The multilevel inverters requires too many semiconductor switches and thus its cost gets increased and thus the use of multilevel inverters are justified by showing the voltage and current burden on each switch and thus it is showed that in spite of the increased number of switches there will not be much cost difference as the burden on switches gets reduced low rating semiconductor devices can be used to implement the module. Also the control strategy is very much simple there will not be much cost difference. Also it is shown that voltage and current total harmonic distortion gets reduced on increasing the number of levels in a multilevel inverter.

3.1 Two level inverter

Figure 4 shows a single phase h bridge inverter having 4 switches. Generally an IGBT is used as a switch in an inverter. It is seen that an R-L load is being connected between the two legs of the inverter. A conventional two level inverter uses the two voltage levels at the output of the inverter they are the +V volt and –V volt. For output to be +V volt switch S1 and S2 are closed together and S3 and S4 are kept open. To obtain –V volt at the output S3 and S4 are closed together and S1 and S2 are kept open. The switching table of a Two level inverter is shown in table 1. The output waveform of a two level inverter is shown in figure 5.

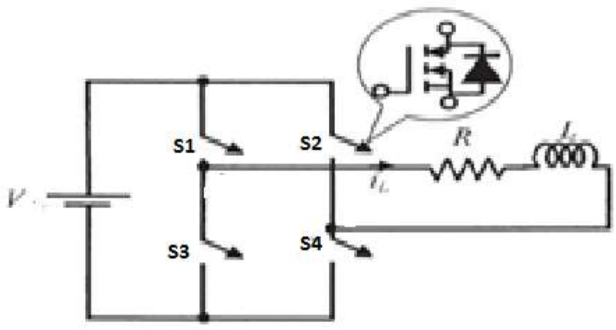

Fig. 4 A single phase h bridge inverter

Table 1 Switching Table of Two Level H Bridge Inverter

Voltage level	S1	S2	S3	S4
+V	1	0	0	1
-V	0	1	1	0

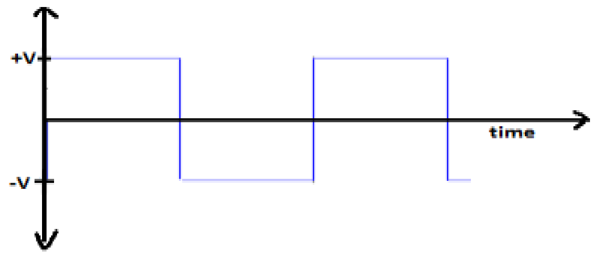

Fig 5 Output Waveform of a Two Level Inverter

3.2 Three level inverter

By manipulating the switching signals of the h bridge inverter of figure 1, three level inverter can be obtained. A three level inverter has three level of voltage at the output side namely 0 volt level, +V volt level and –V volt level. The switching table of a three level inverter is shown in table 2. The output voltage waveform of a three level inverter is shown in figure 6.

Table 2 Switching Table of a Three Level Inverter

Voltage level	S1	S2	S3	S4
0	0	0	1	1
+V	1	0	1	0
-V	0	1	1	0

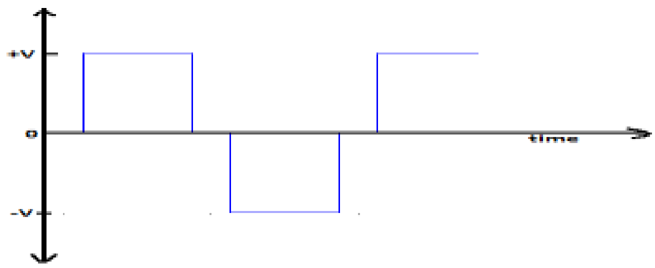

Fig 6 Output Waveform of a Three Level Inverter

3.3 Five level inverter

Figure 7 represents the circuit diagram of a five level inverter. It requires two cascaded connecter h level bridge having eight switches. The output voltage levels are 0 volt, +V/2 volt, -V/2 volt, +V volt and –V volts. The switching sequence to obtain 0 , +V/2, -V/2, +V and –V is shown in the table 3. The output waveform of a five level inverter is as shown in the figure 8.

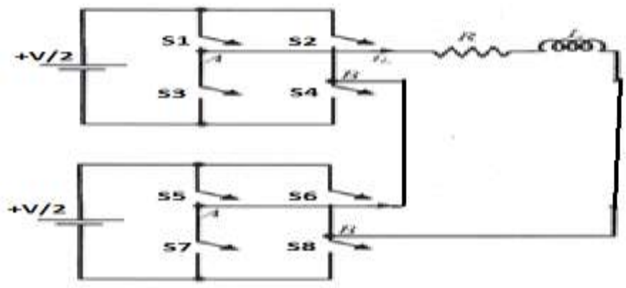

Fig 7 Circuit Diagram of a Five Level Inverter

Table 3 Switching Table of five Level Inverter

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	1	0	0	1	1
+V/2	1	0	0	1	0	0	1	1
-V/2	0	1	1	0	0	0	1	1
+V	1	0	0	1	1	0	0	1
-V	0	1	1	0	0	1	1	0

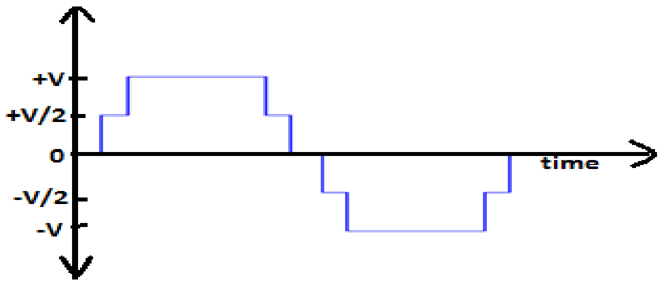

Fig 8 Waveform of a 5 Level Inverter

3.4 Seven Level Inverter

Figure 9 represents the circuit diagram of a 7 level inverter. It requires three dc voltage source and 12 switches. The voltage levels of a 7 level inverter are 0, V/3, 2V/3,V,-V/3,-2V/3 and –V volts. On proper switching these voltage levels at different instant of time is obtained to obtain the nearly sinusoidal signals. The switching sequence to obtain the desired voltage levels is shown in table 4. The output waveform of the 7 level inverter is shown in figure 10.

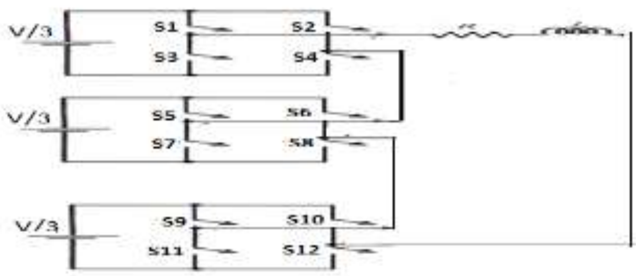

Fig 9 Circuit Diagram of a 7 Level Inverter

Table 4 Switching Table of a Seven Level Inverter

Volt	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	1	0	0	1	1	0	0	1	1
+V/3	1	0	0	1	0	0	1	1	0	0	1	1
-V/3	0	1	1	0	0	0	1	1	0	0	1	1
+2V/3	1	0	0	1	1	0	0	1	0	0	1	1
-2V/3	0	1	0	0	0	1	1	0	0	0	1	1
+V	1	0	0	1	1	0	0	1	1	0	0	1
-V	0	1	1	0	0	1	1	0	0	1	1	0

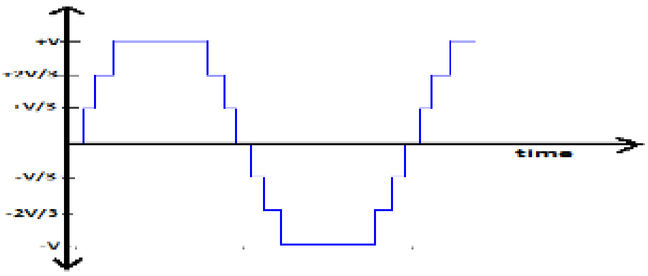

Fig 10 waveform of a 7 level inverter

3.5 Selective Harmonic Elimination

The basic idea of the selective harmonic elimination is to pre-determine the switching angle for each module to get the expected waveform of the output [8]. To explain its implementation in the cascaded H-bridge multilevel inverter, one example of five modules, eleven levels CHB multilevel inverter is shown in Figure 11.

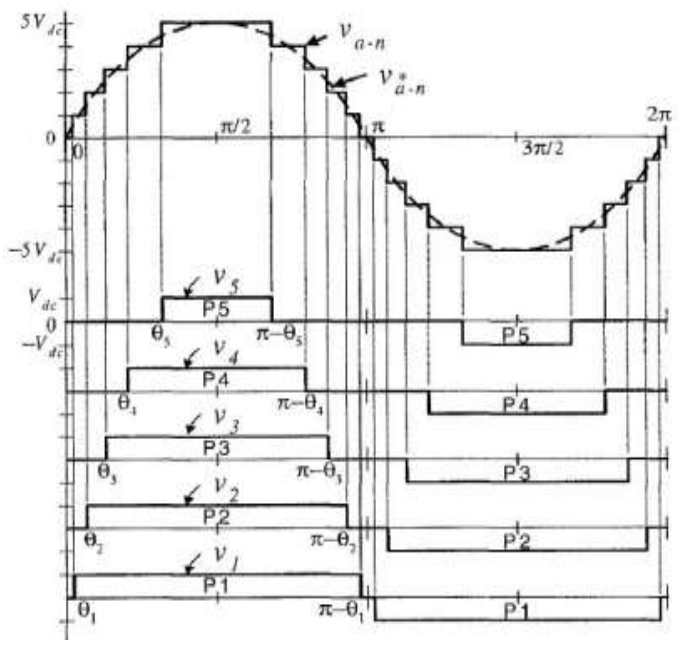

Fig 11 Output waveform of an 11-level cascade inverter

By using Fourier Transform, the output voltage V (ωt) can be expressed as

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [cos(n\theta_1) + cos(n\theta_2) + \ldots + cos(n\theta_5)] \frac{sin(n\omega t)}{n} \qquad (4.1)$$

where n is the harmonic order. Since the waveform is both half wave symmetry and odd symmetry, n = 1, 3, 5, 7, ... Usually, the normalized Fourier coefficients of the magnitude are used for further analysis. The normalized magnitude can be obtained by dividing V_{dc} on both sides of equation 4.1. Hence, the normalized Fourier coefficients for each harmonic order components are

$$H(n) = \frac{4}{\pi n}[cos(n\theta_1) + cos(n\theta_2) + \ldots + cos(n\theta_5)] \qquad (4.2)$$

where n = 1, 3, 5, ... Then by choosing the conducting angle θ1 → θ5 appropriately, it is possible to eliminate some target harmonic components [8]. Another point need to be mentioned is that the number of harmonic components which can be eliminated by this modulation method is one less than the number of the conducting angles since one degree of freedom should be given to the fundamental components of the waveform. In this case, the number of harmonics that can be eliminated is 4. Since the triple harmonic would not exist in the line to line voltage, the 5th, 7th, 11th and 13th order harmonics are chosen as the target harmonics that need to be eliminated in this case. The following equation can be obtained:

$$cos(5\theta_1) + cos(5\theta_2) + cos(5\theta_3) + cos(5\theta_4) + cos(5\theta_5) = 0 \qquad (4.3)$$

$$cos(7\theta_1) + cos(7\theta_2) + cos(7\theta_3) + cos(7\theta_4) + cos(7\theta_5) = 0 \qquad (4.4)$$

$$os(11\theta_1) + cos(11\theta_2) + cos(11\theta_3) + cos(11\theta_4) + cos(11\theta_5) = 0 \qquad (4.5)$$

$$os(13\theta_1) + cos(13\theta_2) + cos(13\theta_3) + cos(13\theta_4) + cos(13\theta_5) = 0 \qquad (4.6)$$

$$cos(\theta_1) + cos(\theta_2) + cos(\theta_3) + cos(\theta_4) + cos(\theta_5) = 5m_i \qquad (4.7)$$

where mi is reference modulation index which is defined as mi = Vref 5Vdc . One advantage of this modulation method is that the inverter is switching at the fundamental frequency which decreases the switching losses. However, the pre-calculation of the conducting angle requires the solution of non-linear equation. When the level of inverter increases, the number of the non-linear equations would also be very high. Then the solution for these equations would be inaccurate which may increase the distortion in the output voltage waveform [9].

3.6 Phase Shifted Pulse Width Modulation

Phase shifted PWM is one of the most commonly used modulation method in CHB multilevel inverter since it is very suitable for the modularity of the topology. For each module, the reference signal is the same. However, the carrier waveform (usually triangular waveform) for each module would have a phase shift to ensure the step characteristic of the output voltage. How many degrees is the phase shift between each module depends on the modulation method for the individual H-bridge inverter. If the unipolar modulation method is selected, the phase shift between each module should be 180◦/k to achieve the lowest output voltage distortion; if the bipolar modulation method is chosen, the phase shift between each module should be 360◦/k [10], where k is the number of modules. Three modules, seven levels CHB multilevel inverter with unipolar modulation method is shown in Figure 12.

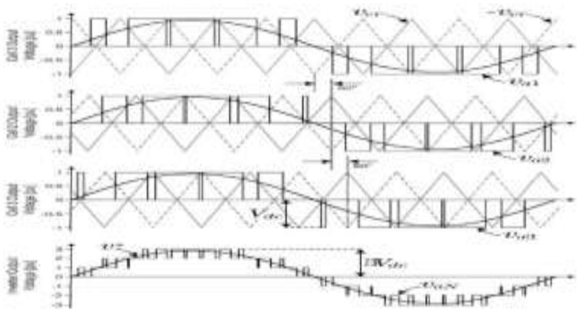

Figure 12 Three cell PS-PWM waveform generation

The output voltage of the inverter is as k times as the output voltage of each module which is one advantage of this modulation method since the switching devices need only withstand the voltage of their modules. Moreover, the frequency of the output voltage has k times as the switching frequency of each module which is beneficial in reducing the conducting losses of the inverter.

An open loop control structure using Fibonacci series control signal is being implemented in this paper. A sinusoidal signal is compared with a constant value whose value is determined using the Fibonacci series. From the switching tables it is seen that the switch in the lower limb is having gate signal such that it is complement of the upper limb gate signal for example gate signal of S3 which is the lower part of S1 is not of gate signal of S1. Now to obtain the desired signal a sinusoidal signal whose frequency is equal to 50 Hz is being compared to a constant value signal and gate signal is being generated.

Let the sine wale signal which is being compared with a constant value signal be denoted by F.

For a two pulse inverter there is only one constant value signal whose value is 0. If F is greater than 0 then switch S1 is ON.

If F is lesser than 0 then switch S2 is ON. The gate signals given to S3 and S4 are inverter gate signals of S1 and S2 respectively.

For a 3 level inverter the only difference is that S1 is ON when F is greater than 2 and S2 is on when F is lesser than -2.

For a five level inverter there are 4 more switches. The switching of S1 and S2 are similar to that of a three level inverter. Switch S5 is ON when F is greater than 5 and switch S6 is on when F is lesser than -5. Switch S7 and S8 are the inverted signals of S5 and S6 respectively.

For a seven level inverter S9 is On when f is greater than 9 and S10 is ON when F is lesser than -9. Switches S11 and S12 gets the gate signal of inverted values of S9 and S10 respectively.

Thus with the increase of each bridge the sinusoidal signal F is compared with the constant value which is obtained by Fibonacci series starting with 2. Such as 2,5,9,14,……. The amplitude of the sinusoidal signal has to be kept in such a manner that it should be the next number in Fibonacci series after the largest constant value of the constant signal used for controlling. For example the amplitude of F for 2,3,5 and 7 level must be 2,5,9, 14 respectively.

SIMULATION DIAGRAM AND RESULTS-

Simulation of inverter having different voltage levels are being done is a mat lab simulink using sim power system toolbox.

The simulation diagram of a two level inverter with control signals is being shown in figure 13. The magnitude of the dc voltage used is 230 $\sqrt{2}$ which is the peak value of a sinusoidal signal whose rms vale is 230 Volt.

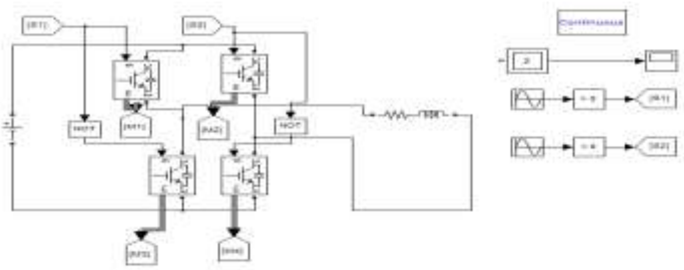

Fig 13 simulation diagram of a two level inverter

A load whose resistance is 10 Ω and inductance of 5 mili Henry is being connected to the output of the inverter to obtain the waveform of output voltage and current. Figure 14 shows the output voltage and waveform of a two level inverter.

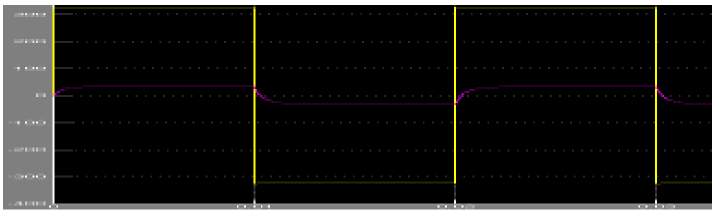

Fig 14 Output voltage and current of a two level inverter.(yellow line is waveform of voltage and the pink line is the waveform of the current)

Simulation diagram of a three level inverter with its control structure is being shown in figure 15. The outpul voltage and current is being shown in figure 16.

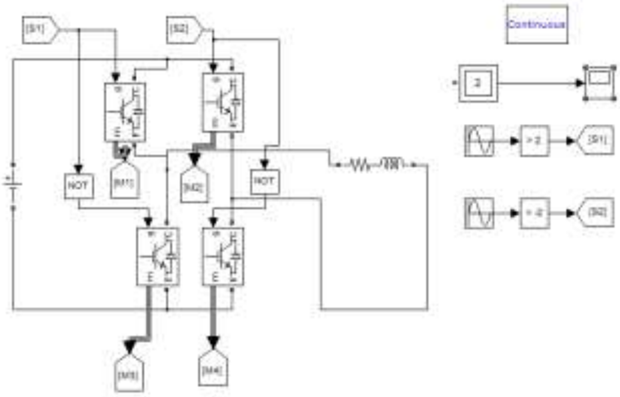

Fig 15 Simulation diagram of a three level inverter

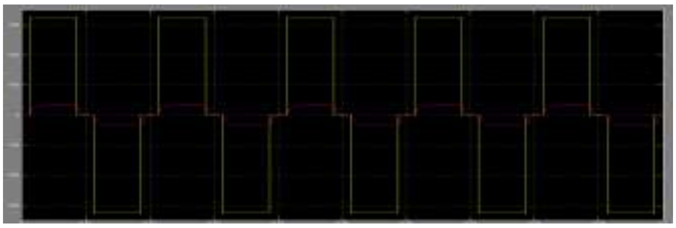

Fig 16 Output voltage and current of a three level inverter. (yellow line is waveform of voltage and the pink line is the waveform of the current)

Simulation diagram of a five level inverter with its control structure is being shown in figure 17. The output voltage and current is being shown in figure 18. Here the voltage source used is $\frac{230\sqrt{2}}{2}$.

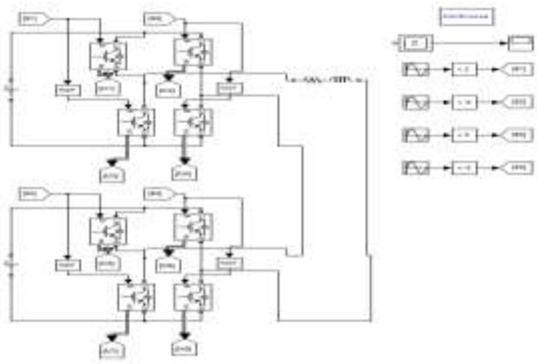

Fig 17 Simulation diagram of a five level inverter

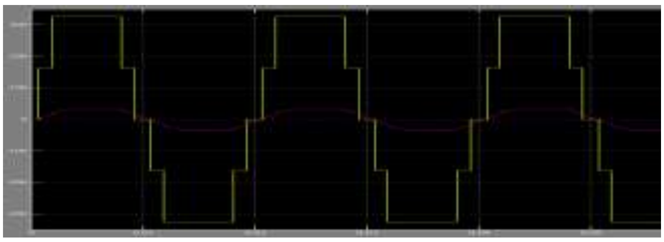

Fig 18 Output voltage and current of a five level inverter. (yellow line is waveform of voltage and the pink line is the waveform of the current)

Simulation diagram of a five level inverter with its control structure is being shown in figure 19. The output voltage and current is being shown in figure 20. Here the voltage source used is $\frac{230\sqrt{2}}{3}$.

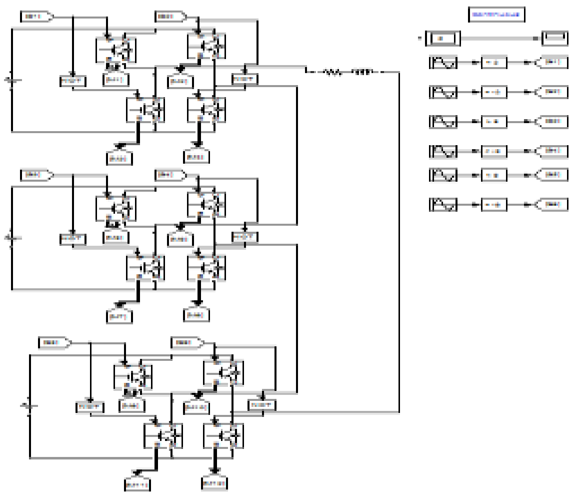

Fig 19 Simulation diagram of a seven level inverter

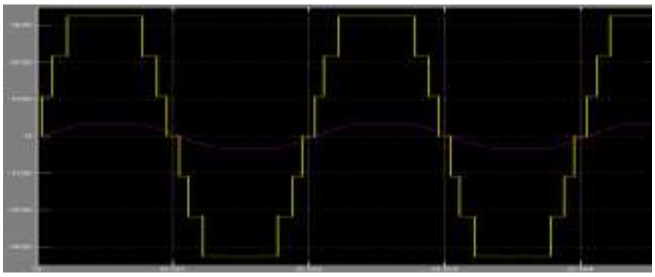

Fig 20 Output voltage and current of a seven level inverter. (yellow line is waveform of voltage and the pink line is the waveform of the current)

From the results obtained from all levels of inverter the voltage burden, current burden of the switches used, voltage harmonics and current harmonics of the output is compared in table 5

4. CONCLUSION:-

From the various results obtained from different waveforms of different inverters and comparing the results obtained as shown in table 5 it is concluded that on increasing the number of voltage levels in an inverter the power quality of the output obtained goes on increasing the total harmonic distortion of voltage as well as the current waveform is reduced and also voltage burden on each switch is being reduced to a large extent. On further increasing the voltage levels the output obtained can be made nearly sinusoidal so as to supply the load with a good power quality if it is being supplied by the photo voltaic array which is having DC voltage as the output

There are still some improvements which can be added to the system. First of all, it would be very interesting that the energy storage system such as battery or super-capacitor can be integrated into the system. This will make the system more reliable. When there is no radiation at all, the system can still provide power from the energy storage system.

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