Comparative Analysis of High Speed SRAM Cell for 90nm CMOS Technology

Saurabh Kumar Yadav

Student, Department of Electronics Engineering, IET, Lucknow, India – 226021

Abstract - *This paper work includes fundamental simulation calculation of low power SRAM cell for specific frequencies. The dynamic power may be expressed as: P=αCV2 f. We will take a look at the charging time and discharging time. The power consumption during charging and discharging with frequencies is observed. For this reason write operation on exclusive conditions and structures might be generated by way of simulation technique. 6T and 8T SRAM cellular dissipation during circuit dynamic switching activity are targeted to improve. In evaluation of traditional SRAM cell of 8T SRAM cell crosstalk voltage, values are placed for bit line, word line (WL) and outputs are achieved. With the assist of right sizing of Width (W) and Length (L) of the transistor these values can be managed. By means of right selection of sign WS in these 6T and 8T SRAM cell , we will block any single bit line from being discharged during write "0" ,in addition to write "1" mode. The assessment of 6T SRAM cell and 8T SRAM cell is in the end achieved in these paintings.*

Key Words: 6T RAM, 8T RAM, Low Power, SRAM, CMOS Inverter

1. INTRODUCTION

Semiconductor memories have role as most fundamental unit in VLSI layout. It is the most important unit in machine on chip (SOC) now a day. Almost all SOCs contain memories inclusive of flash memory (FM), Read only memory (ROM), static random get right of entry to memory (SRAM) and dynamic random get entry to reminiscence (DRAM). Memory stares facts in addition to commands used within the popular technology together with portable structures, computer unit and electronic devices. Memory is both volatile and nonvolatile. Volatile type memory loses data while power is switched off whereas nonvolatile memory stores statistics indefinitely. SRAM and DRAM are volatile memory which saves records via the use of transistors and capacitors respectively. Nonvolatile memories like ROM, Erasable programmable read only reminiscence (EPROM) and flash memory stores facts permanently. It may be programmable according to person desires. By ITRS, more than ninety four% if chip location will be covered by means of memory. As reported in ITRS road map, transistor devoted to memory shape in common embedded gadget is around 70% presently and expected to growth to 80% in future. Power is one of the crucial resources, as a result the designers try to lessen it at the same time as designing a machine. The major undertaking in portable electronics devices is to reduce their power dissipation. Power consumption of memory is main interest for any layout, notably ram is acknowledge to be main unit of any cipher device, Variation within the process parameter due to the fact of aggressive calling of technology create a let of problems in yield, reliability and checking out. Generally, it's far said that for every 10 diploma upward push in temperature the failure price of a VLSI chip become doubles.

In this work we consciousness at the dynamic operation and respective power dissipation in CMOS SRAM cellular. The charging and discharging of bit lines eat furthermore strength in course of the Write operation. While convenient charging, dis-charging bit lines 6T, 8T S-RAM cell are reserved to find transistor trail in pull down part. The outputs of those S-RAM cells are taken on distinctive frequencies given electricity deliver. The circuit is characterized by means of the use of the ninty nm era that is having deliver voltage of 1.5 V. Finally outputs are compared by regular S-RAM cell. The reduction in strength dissipation is discovered for 6T and 8T SRAM mobile. The end result of this work has practical reference fee for further take a look.

2. RELATED WORK

[1] A SRAM rated at 2W, 100 kHz, 480kb working at 2V, confirmed for 130nm C-MOS process. The 10T S-RAM mobile processing in 1k cells/bit-line which records structured bit-line leakage. Another similar scheme was given by T.H.Kim in 2008 which provides us good judgment with zero degree capturing, calculating limits in examine fenders. By applying sturdy re-verse brief channel impact at sub threshold location we can improve cell writ ability also it enhance row decoder performance as it helps in accelerating the modern day derivability in extended channel period. Sizing approach which we used gives result in equal write wl with voltage uplift by 70mV , it gives out a put off development 28 percentage at row de-coder as compared , traditional sizing scheme on 2V .The pseudo write problem caused in unselected columns is removed by utilizing a bit-line write back scheme.

A 130nm system is generated by implying a sub-threshold with rating .2V, 480kb.To resolve the examiner failure caused due to information dependent bit-line leakage a 10-T SRAM cellular is proposed. A good and convenient way to track good judgment low level of bit-lines with PVT variations the proposed scheme is VGND, the VGND scheme helps us to get most examine sensing margin. The strong RSCE placed inside sub threshold is quite helpful to improve cellular writ ability, it also reduce electricity

consumption, and enhance common sense performance, also improves circuit resistance against disturbing variations. The above mentioned and proposed techniques now we are ready to implement thoroughly functioning sub-threshold SRAM of 1k cell in step with bit-line working at .2V and 27C.

[2] A. Teman, 2011worked on digital circuits operating at low voltage which yields a better choice for competitive power reduction. Now days the frequently used SRAMs have limited choice as it operates inside the strong inversion regimes which leads system variation and mismatch, because of all these there are several improvement is trending in SRAMs operating at low voltage. In this process, we gift an unique 9T bit cell, which have major setback to supply feedback concept which internally weeks pull up modern at some point of write cycles and helps us to do write operations at very low voltage. Here we resolve the problem associating with low voltage operation without using an extra peripheral circuits and strategies. Whatever bit-cell model we proposed here working fluently on international and neighborhood variations at voltage lying in range 250mV to 1.1V.Along with this the other major setback associated with proposed bit-cell is that it have low leakage strength as much as 60% as compared to identically supplied 8T bit cell which we are using. An 8kbit SRAM array carried out, designed by lower electricity 40nm procedure, resulting full capability at very low power. This painting offered a singular feedback to 9T Supply SRAM bit cell. The technical ideas and working processes within the bit cell were mentioned. In our proposed model we are offering a static and dynamic metrics which are quite compatible with widespread used 8T bit cell. Several improvements and implementations were proposed and payoffs were defined. The proposed bit cell giving us strong operational range under international and neighborhood system variations for the duration of the entire variety of supply voltage lower 252 mV. We achieve given result without utilizing extra peripheral circuits. In addition, it is considered solid state, cellular affords inner leakage suppression, which gives a result in 15% to 61% decrease in static power consumption , to a 8-T mobile operating on equal supply voltage reading(depends at implementation). An 8kbit array S-F-S-RAM bit-cells became carried out, fabricated and experimented in low power 40nm CMOS procedure. Measurement result shows complete functioning in any respective voltages among V and 400mV (the limiting value of voltage have to take a look at chip).

[3] L. Chang, 2015 worked on SRAM cellular balance and it's a tough challenge to destiny technology as our main concern is to decrease energy supply voltage. By means of selecting the suitable cell lay-out, tool threshold voltage, beta fraction 6T-S-RAM may be optimized for optimal balance. In case of 8T-SRAM it giving great increment in stability by eliminating mobile disturbs at some stage in examine access so emphasis continued era scaling. So for we worked on the smallest 6-T [0.124μm2 halve of-cell), full 8-T (0.1998μm2) cell.

SRAM mobile design techniques were discussed to maximize mobile stability. But in case of 6T-SRAM may be optimized for stability, a great deal larger profits can be found out with 8T-SRAM mobile. As 8T-SRAM is more compatible it can allow for continued scaling beyond this that is viable with traditionally used 6T-SRAM with the addition of more FETs, it imposing a-30% location penalty.

[4] E. Vittoz, 2012 discussed a RF strength harvester which helps in optimizing for sensitivity and also wireless range, for the vital applications requiring intermittent verbal exchange. The RF electricity harvester operating at -32dBm sensitivity and 915MHz produces 1V output. This was performed by the use of a CMOS rectifier running in the sub threshold area and a community which have off chip impendence matching for reinforcing the received voltage. Rectifier performance are presented and confirmed with the equations through measurements of more than one rectifiers using one kind of transistors in a 130nm CMOS technique.

In this work, max sensitivity achieved by the proposed CMOS rectifier running in sub threshold. A particular IC is produced in a 130nm CMOS generation, and sensitivity of -32dBm of the rectifier is measured at 915MHz. Different kinds of CMOS rectifiers with numerous sorts of transistors and several numbers of tiers are in comparison to justify the equations, and a layout strategy is furnished.

3. 8T SRAM Cell

Architecture for 8T SRAM cell is just like which of traditional 6T S RAM cellular. Yet the skip transistors in 6T SRAM cell are changed by using Transmission Gates. Therefore, two greater transistors M7 and M8 are added to the circuit. The operating of TG8T SRAM cellular includes operation.

3.1 Write Mode

Both the bit traces are at reverse voltages when we acting a write operation which constitute if bit line BLB is at low then bit line BL is at excessive and vice versa (BL= 1 and B LB = zero or B L = zero and B LB = 1). Information writes at the output nodes Q and QB of lower back to again related inverter when WL turns into high and additionally WLB =0 which enables NMOS and PMOS transistors M5 and M6.

3.2 Read Mode

Both the bit lines are at high voltages additionally behave as an output and WL is raised to excessive and WLB at zero when we carry out the red operation which is simply reverse to the write operation.

The one in every of pre-charged bit lines start dis-charging and at that present statistics goes to be read since one of the output nodes (Q and QB) is at low.

Schematic of 8T SRAM mobile is proven in fig 1 (a) In that for lowering the strength dissipation we use more transistors M7 and M8, for controlling the M7 and M8 all through Write "zero" and write "1" operation WS signal is used.

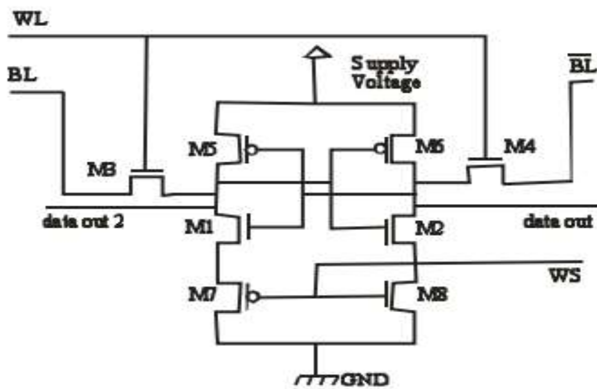

Fig - 1: 8T SRAM Cell

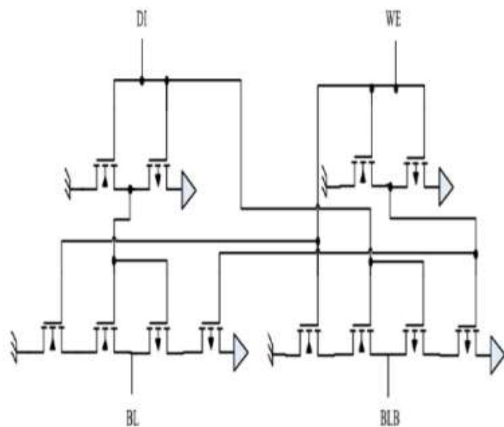

Fig - 2: Write Driver [11]

The given input address is decoded by the decoder and it also uses for the permission of selected WL word line, in the availability of many inverters. We've got dynamic decoder utilized. While in comparison from another form of decoders Dynamic decoders [30] has subsequent blessings. (a) (b) given layout, lesser time taking, design of decoder are easy, have wide Varity of transistors. [c] Electricity intake is small. [d] Place of decoder is quite suitable. Unique dynamic C MOS A ND gate decoder is us in as opposed to dynamic C MOS O R gate decoder, previous takes small area, much lower strength compare to latter. Word reminiscence, m: n dynamic C-MOS, AND gate decoder utilized, wherein m=log2.n. Schematic a two, four dynamic C MOS A ND gate decoder is proven by fig 3.

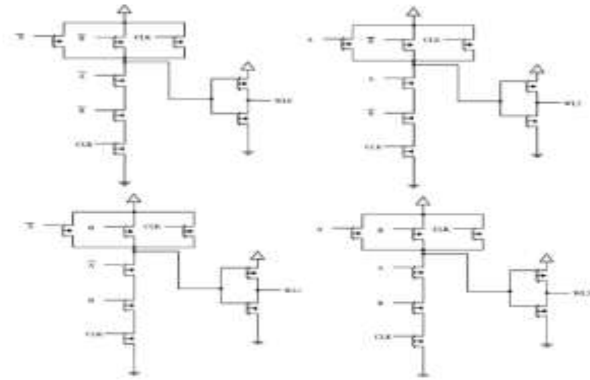

Fig - 3: Dynamic CMOS AND Gate Decoder [10]

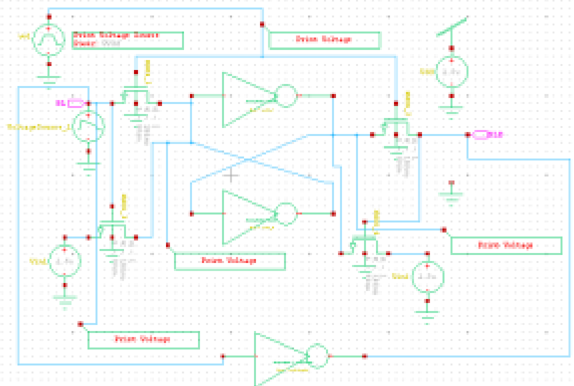

Fig - 4: Design of 8T SRAM using Tanner tool

In the fig 4 the design of 8T SRAM structure is shown. It has three CMOS inverters having 6 transistors and two additional transistors NMOS_3 and NMOS_4 thus we have total 8 transistors along with NMOS_1 and 2 transistors. The voltage source_1 (given at BL port) is the input signal that is to be used as write signal. This signal is given to the inverter through the NMOS_1.This is the inverter input named as InOut1.The inverter output is taken at InOut2 terminal connected to output of one of the inverter. InOut2 signal is passed through the NMOS_2 and taken at BLB terminal. The voltage Vdd = 1.5 volts and the read/write control signal i.e. 'vol' is given to both the NMOS 1 and 2.These read write control signal are used to save and read the voltage source_1 signal in this 6T SRAM structure. Voltage of 1.5volt is connected as vin1 and vin2 to the NMO# 3 and 4.

Fig 5 shows the dynamic power dissipation performance of 8T SRAM. It can be observed that during the static levels the power consumption is zero. The moments at which the read/write operation is performed the power consumption in form of spikes are observed for small moments. The power consumed here in read is 82micro watts and the power consumption in write is 120 microwatt thus the average power consumption can be taken as 101 micro watts.

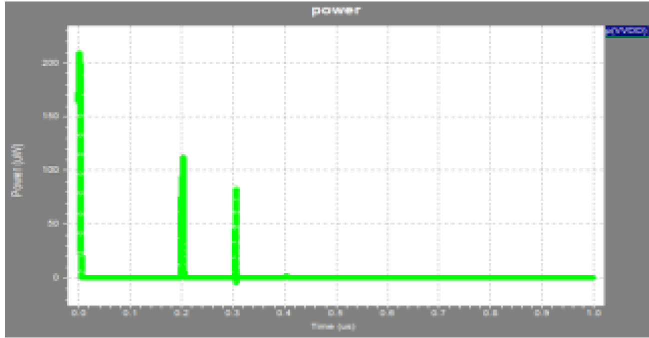

Fig - 5: Dynamic Power dissipation analysis of 8T SRAM

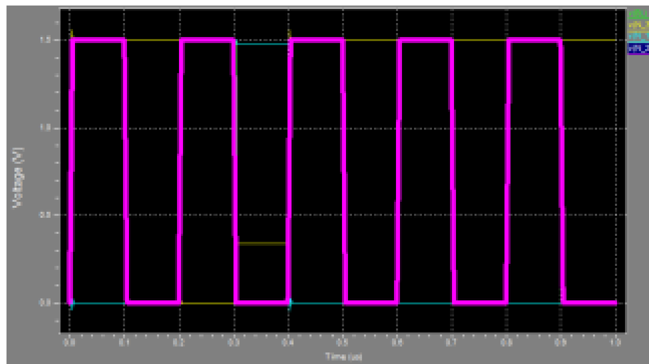

Fig - 6: Response for read/write Logic validation for 8T SRAM

After getting the power dissipation the logic validation is performed for read write operation as shown in fig 6. For this purpose different binary input are given at write control moments and there after read control is used to verify the successful write operation. Fig. 7 shows the magnified view of read write logic validation. Here initially binary input is low '0' and the write signal is given as read/write port is high. In this figure there are three waveforms named as v (inout2): blue (inout1): black and c (N2) red. Initially during write operation input is low and then it becomes read phase and we get zero as output then again write signal is given and input is '1' and the read signal is made high and read output is '1'.Thus it justifies that '01' given as input during write phase and '01' is exactly obtained at read phase.

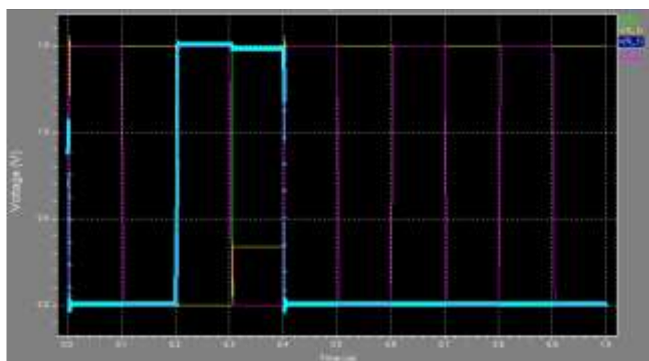

Fig - 7: Magnified view for read write logic validation for 8T SRAM

Static noise margin (SNM) is a key figure of merit for an SRAM cell. By nesting the largest possible square in the two voltage transfer curves (VTC) of the involved CMOS inverters it can be found. By the side-length of the observed square the SNM feature is defined, given by voltage in V. The state of the SRAM cell can be changed and henceforth information is gone whenever any external DC noise voltage is input in larger value than the SNM. The SNM at both 6T and STRAM are calculated at 90nm and 180nm CMOS technology. The input voltage values are observed at both inverters to obtain the voltage transition curve shown in figure 4.22 and 4.23.

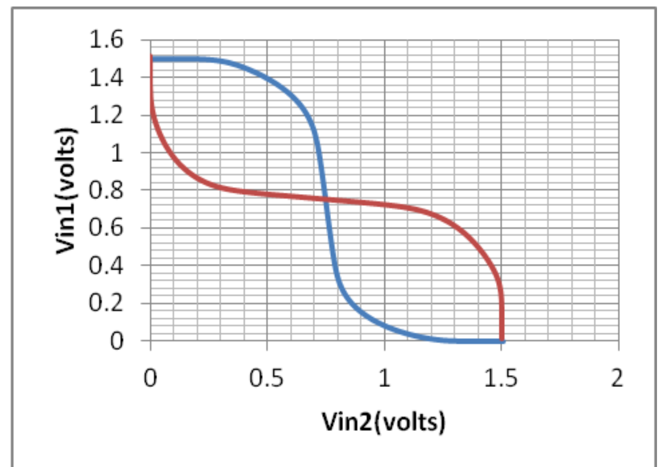

Fig - 8: Inverter voltage transition plot for calculating SNM at 90nm CMOS technology.

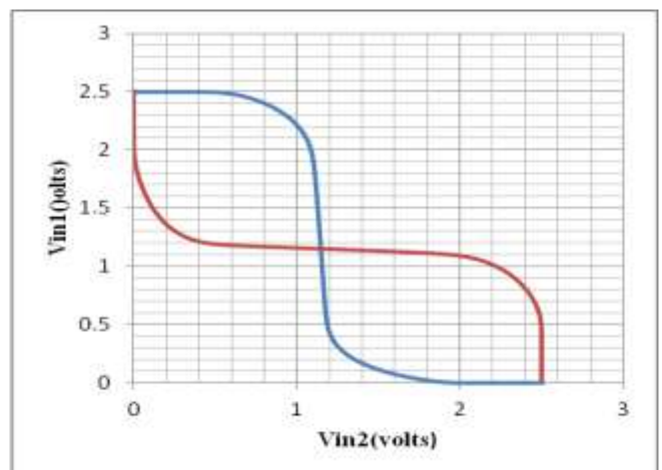

Fig - 9: Inverter voltage transition plot for calculating SNM at 90nm CMOS technology.

All the read out recorded for the 6T and 8T SRAM at 90 and 180nm CMOS technology are summarized in table 4.5.This table shows the observed power dissipation (microwatt) , delay (nano secs.), static noise margin (SNM) in volt and die area (sqr. micrometer).

Table - 1: Summarized results for 6T and 8T SRAM at 90nm CMOS technology

Technology 90nm				
	Power dissipation (μw)	**Delay (ns)**	**Static Noise Margin (V)**	**Die Area (μm^2)**
6T SRAM	254	4.2	0.4	0.1458
8T SRAM	101	5	0.4	0.1782

Table - 2: Summarized results for 6T and 8T SRAM at 180nm CMOS technology

Technology 180nm				
	Power dissipation (μw)	**Delay (ns)**	**Static Noise Margin (V)**	**Die Area (μm^2)**
6T SRAM	657	3.5	0.72	4.0176
8T SRAM	529	4.3	0.72	4.1472

4. CONCLUSION:

A 6T and 8T SRAM is designed using CMOS transistor and implemented in Tanner Tool design suite in 90nm and 180nm technology. The SRAM was analyzed by simulating it for parameters like power consumption, static noise margin, and delay and performance accuracy. From the SNM, robustness against noise is verified and analyzed during read and write operations transition phase. Performing analysis based on relationship between 6T and 8T in a statistical model to estimate the power consumption value for an SRAM of given size. As the technology is growing, the device dimension is reducing, results in variation of output voltage affecting SRAM cell stability to great extent. From the simulation results good SNM is obtained by scarifying the area. In future comparative analysis for other designs on more reliable tools like cadence etc. can be generated with optimization approach to follow up the trade off in between size, robustness and efficiency

REFERENCES:

[1]. T. H. Kim and J. Liu and J. Keane and C. H. Kim, “A 0.2 V, 480 kb Sub threshold SRAM With 1 k Cells Per Bit line for Ultralow-Voltage Computing,” IEEE J. Solid-State Circuits, vol.43, no.2, Feb. 2008, pp.518-529.

[2]. A. Teman and L. Pergament and O. Cohen, A. Fish, “A 250 mV 8Kb 40 nm Ultra-Low Power 9T Supply Feedback SRAM (SF-SRAM),” IEEE J. Solid-State Circuits, vol.46, no.11, Nov. 2011, pp. 2713-2726.

[3]. L. Chang and D. M. Fried and J. Hergenrother and J. W. Sleight and R. H. Dennard and R. K. Montoye and L. Sekaric and S. J. McNab and A. W. Topol and C. D. Adams and K. W. Guarini and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in Symp. VLSI Tech. Dig. Tech. Papers, Jun. 2005, pp. 128– 129.

[4]. E. Vittoz and J. Fellrath, “CMOS analog integrated circuits based on weak inversion operations,” IEEE J. Solid-State Circuits, vol. SSC-12, no. 2, Jun. 2012, pp. 224–231.

[5]. A. Wang and A. P. Chandrakasan, “A 180-mV subthreshold FFT processor using a minimum energy design methodology,” IEEE J. Solid-state Circuits, vol. 40, no. 1, Jan. 2005, pp. 310–319.

[6]. B. H. Calhoun and A. Chandrakasan, “A 256 kb subthreshold SRAM using 65 nm CMOS,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, 2006, pp. 628–629.

[7]. L. Chang et al., “Stable SRAM cell design for the 32 nm node and beyond,” in Symp. VLSI Technology Dig. Tech. Papers, 2005, pp. 128–129.

[8]. J. Chen and L. T. Clark and T. Chen, “An ultra-low-power memory with a subthreshold power supply voltage,” IEEE J. Solid-State Circuits, vol. 41, no. 10, Oct. 2006,pp. 2344–2353.

[9]. T. Kim and H. Eom, J. Keane and C. Kim, “Utilizing reverse short channel effect for optimal subthreshold circuit design,” in Proc. Int. Symp. Low Power Electronics (ISLPED’06), Oct. 2006, pp. 127–130.

[10]. Sandeep R. and Narayan T. Deshpande, “Design and Analysis of a New Loadless 4T SRAM Cell in Deep Submicron CMOS Technologies” Second International Conference on Emerging Trends in Engineering and Technology, ICETET-09.

[11]. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits”, TMH, 2003.

BIOGRAPHIES

Saurabh Kumar Yadav received the B.Tech degree in Electronics and Communication Engineering from Galgotias College of Engineering and Technology, Abdul Kalam Technical University Lucknow, India and is currently working towards his M.Tech degree in Microelectronics with the research interest in Digital VLSI and the enhancing the performance of Digital Circuit from Institute of Engineering and Technology, Lucknow, Uttar Pradesh.