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Hardware Co-Simulation of Classical Edge Detection Algorithms Using Xilinx System Generator

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Abstract - *Edge Detection is one of the most important and fundamental processes in the field of Image Processing and Computer Vision. It is a process of localizing pixel intensity changes. Classical edge detection methods such as Robert, Prewitt and Sobel are simple to design than Laplacian based methods. Hence, these are used in Real Time image processing applications quiet more often. The proposed designs for Classical Operators utilize minimum resources. At the same time, it also enhances maximum frequency of operation. Spartan-3E Starter Kit is used for prototyping purpose. JTAG Hardware Co-Simulation utilizes hardware in loop approach. An efficient way to implement image processing tools on reconfigurable hardware is to design algorithms using Xilinx System Generator.*

Key Words: **Image Processing; Edge Detection; Xilinx System Generator; JTAG Hardware Co-simulation; Spartan-3E FPGA**

1. INTRODUCTION

Digital Image consists of various pixels. Very few of these pixels actually carry information. By detecting edges in an image, one can preserve useful structural information and eliminate redundant data [1]. It is an efficient way for storage and bandwidth utilization. Edges can be characterized by sudden change in the pixel intensity. Thus, edges are components with high spatial frequencies. Any change can be located by mathematical tool named as derivative. In discrete domain, derivative is nothing but difference equations. By convolving image pixels with given masks this change can be located. Finding gradient implies taking derivative for one time whereas, for finding Laplacian derivative is taken two times. Edge profile can be categorized as step, ramp, ridge and roof. Gradient based methods find out maximum/minimum values whereas, Laplacian based methods find out zero crossing [2]. Gradient works well when image contains sharp intensity and low noise. Hardware implementation of these edge detection algorithms is essential in order to use it in real time [3]. Field Programmable Gate Array (FPGA) has advantages over Application Specific Integrated Circuit (ASIC) with no non-recurring expense (NRE), less time to market and high flexibility. A low cost Spartan-3E Starter Kit is used as a hardware platform for implementation. In hardware co-simulation approach normal Simulink blocks are executed in MATLAB environment that generates desired operation while JTAG simulation block loads bit stream file generated (*.bit) in FPGA using Hardware in loop [4]. Writing code in Hardware Description Languages (HDL) along with its test bench programming is very tedious job. Xilinx System Generator provides an efficient way to program FPGA by designing algorithm using blocks [5]. Using various compilation, HDL code and required Test bench are generated automatically along with various parameters such as minimum period, maximum frequency, power dissipation and resource utilization [6].

2. EDGE DETECTION ALGORITHMS

Edge Detection algorithms are broadly classified as follow:

-First Order Derivative Methods [Gradient Based]

- Robert Operator
- Prewitt Operator
- Sobel Operator

} Classical Operators

-Second Order Derivative Methods [Laplacian Based]

- Marr-Hildreth Edge Detector [LoG]

-Optimal Edge Detectors: Canny Algorithm

Classical operators include Robert, Prewitt and Sobel operators. Main advantage of these operators is that they are simple to design and have very low latency. These are also less susceptible to noise than Laplacian based methods. Gradient can be find out by convolving operator mask with image pixels. Masks are of different dimensions.

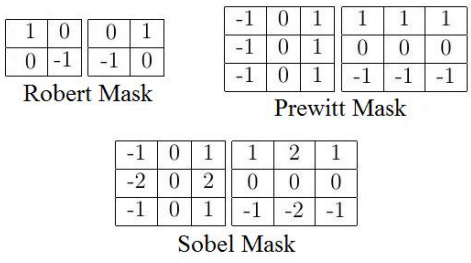

Fig -1: Horizontal & Vertical Masks for Classical Operators

Robert operator is having [2×2] mask whereas, Prewitt and Sobel have [3×3] mask. The Fig- 1 shows both horizontal and vertical masks for all classical operators.

3. SYSTEM DEVELOPMENT & PROPOSED DESIGNS

3.1 System Requirement

Xilinx System Generator (XSG) provides a common environment for MATLAB/Simulink and ISE Design Suit. XSG is invoked by configuring MATLAB R2011b with ISE Design Suit 14.4. Any image processing application can be implemented in XSG using three basic steps. These are image pre-processing, system generator blocks and image post processing. Gateway In and Gateway Out act as a connector between Simulink blocks and System Generator blocks. Various types of compilation can be achieved using system generator token [8].

Hardware co-simulation compilation is used to observe Software and Hardware output images simultaneously whereas Timing & Power Analysis compilation provides information related many parameters such as resources utilized, minimum period, maximum frequency of operation and power. Following steps give system generator flow-

- Configure ISE Design Suit with MATLAB/Simulink
- Design required algorithm using Simulink blocks
- Compile, simulate design to check its correctness
- Choose hardware co-simulation compilation
- Generate JTAG h/w co-simulation model
- Observe waveform, RTL diagram & HDL code
- Program FPGA with bit stream (*.bit) file
- Compile design to perform Timing & Power Analysis

3.2 Proposed Classical Operators Design

The only difference while designing all the classical operators is their gradient filters. Depending on the masks, horizontal and vertical filters are designed.

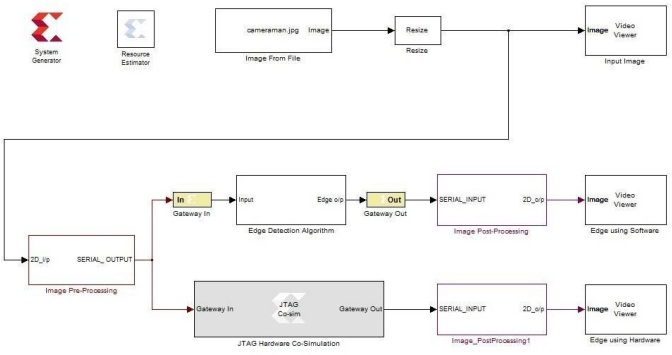

Fig -2: Proposed design for Classical Operators

Fig- 2 shows complete design for all the classical operators. The complete edge detection algorithm is designed in Edge Detection Algorithm block which is connected in between Gateway blocks. It consists of horizontal and vertical gradient filters followed by thresholding block. Thresholding block can be design as shown in Fig- 3. It uses Mux, Relational Comparator and Constant blocks. When gradient magnitude exceeds given threshold, it is considered as Edge. Image from file block inputs color/gray image and Video viewer block displays output binary image. JTAG Co-simulation block is logically equivalent to Gateway and Edge Detection Algorithm blocks. Using JTAG cable the design is implemented on the FPGA hardware.

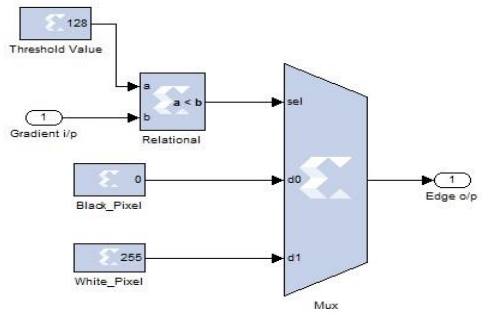

Fig -3: Design for Thresholding Block

3.3 Designs for Gradient Filters

Based on corresponding masks of Classical operators gradient filters are designed. These gradient filters mainly calculate gradient along horizontal and vertical directions. But in case of Robert operator gradient calculation is done in diagonal direction. Filters are designed using various basic Xilinx blocks such as AddSub, Register, Virtex2 Line Buffer etc. Fig-4 and 5 indicate Robert Diagonal Gradient Filters.

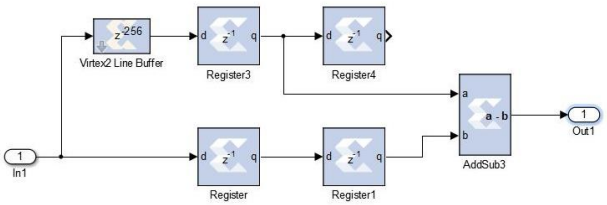

Fig -4: Horizontal Gradient Filter for Robert Operator

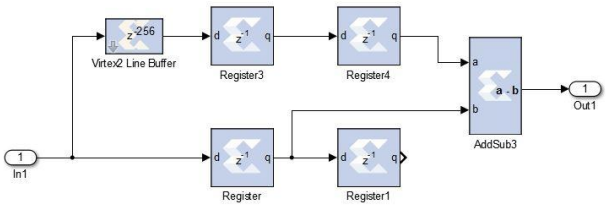

Fig -5: Vertical Gradient Filter for Robert Operator

As the size of mask decreases, it becomes more susceptible to noise. Thus, out of all classical operators Robert is more sensitive to noise. Prewitt operator on the other hand uses 3×3 mask. Fig- 6 and 7 indicate horizontal and vertical gradient filter designs for Prewitt Operator.

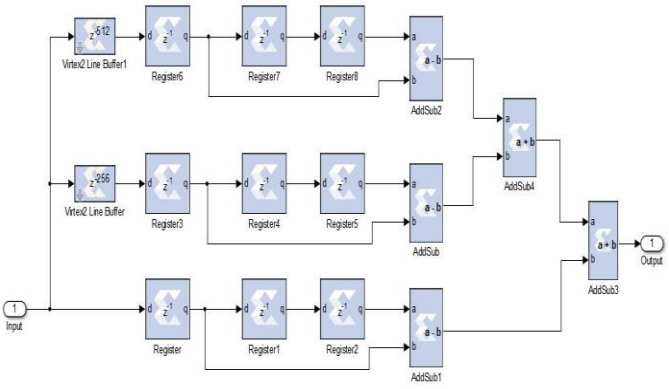

Fig -6: Horizontal Gradient Filter for Prewitt Operator

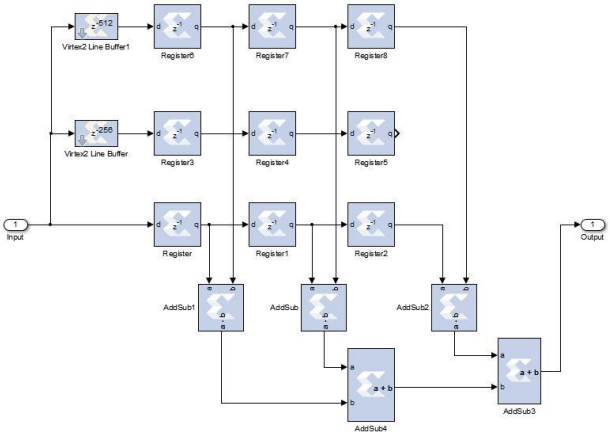

Fig -7: Vertical Gradient Filter for Prewitt Operator

Sobel operator also uses 3×3 mask in order to find out gradient magnitude. The only difference between Prewitt and Sobel is in later one, more weightage has been given to the Central pixel in order to locate maximum edges. In proposed design shift block is used for multiplication purpose. Shifting a bit one place to the left is logically equivalent to multiplying it by two. Fig- 8 and 9 indicate Horizontal and Vertical Gradient Filters for Sobel Operator.

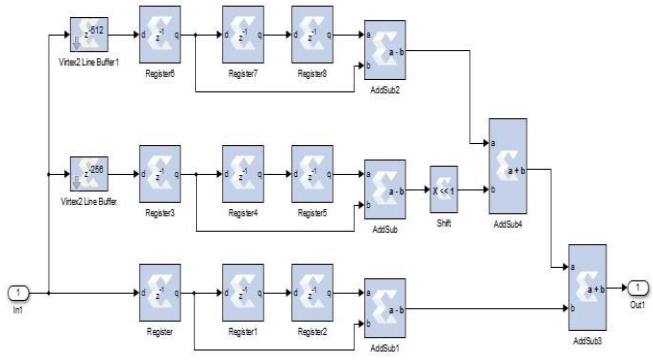

Fig -8: Horizontal Gradient Filter for Sobel Operator

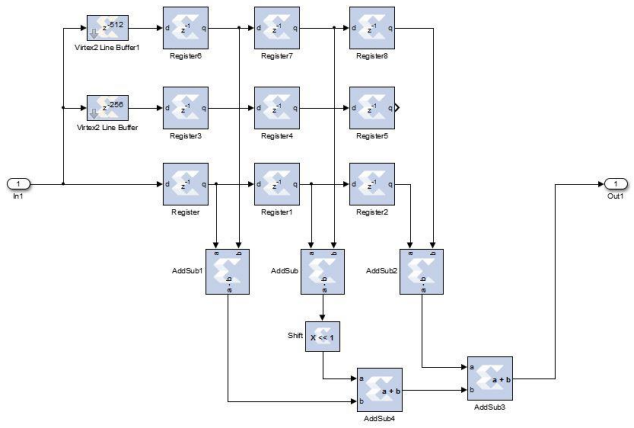

Fig -9: Vertical Gradient Filter for Sobel Operator

4. RESULTS AND PERFORMANCE ANALYSIS

4.1 Results for Edge Detection Techniques

The complete design is logically equivalent to JTAG Co-Simulation model. Preprocessing and post-processing blocks are designed Simulink blocks. Results are observed in MATLAB/Simulink environment whereas, performance parameters are observed with the help of timing & power analysis compilation. Fig- 10 shows results for all classical edge detection algorithms on 256×256 standard Coins image. From the analysis we can say that out of classical operators Sobel provides maximum edges followed by Prewitt and Robert. Thus, generally Sobel is used for gradient calculation in Canny algorithm as well.

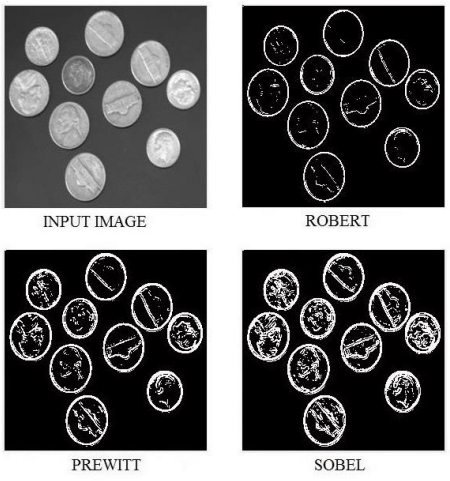

Fig -10: Results for 256×256 coins gray image

Table - 1 provides detailed resource utilization for all the Classical Edge Detection Algorithms and Table - 2 provides various Timing & Power parameters for 256×256 input image using inbuilt Tools [7].

Table -1: Resources Utilization for 256×256 image

LOGIC UTILIZATION	ROBERT	PREWITT	SOBEL
No. of slice flip flops	64	150	148
No. of 4 input LUTs	70	163	159
No. of occupied slices	65	152	167
Total no. of 4 i/p LUTs	87	189	186
No. used as a logic	70	163	159
No. used as a route-thru	17	26	27

Table -2: Timing and Power analysis for 256×256 image

Technique	Total Power (Watts)	Min. Period (ns)	Max. Frequency (MHz)
Robert	0.116	4.48	223.36
Prewitt	0.126	5.11	195.58
Sobel	0.127	5.01	199.60

4.2 Comparative Analysis for Classical Operators

Classical operators such as Robert, Prewitt, Sobel are designed for 512×512 Lena Color Image. Fig-11 shows results for all classical operators. Utilized resources are compared with the design given in literature. Both designs use same hardware platform i.e., Spartan-3E Starter Kit [9]. Table-3 provides resources utilized by proposed design whereas Table -4 provides resources utilized by design in [7].

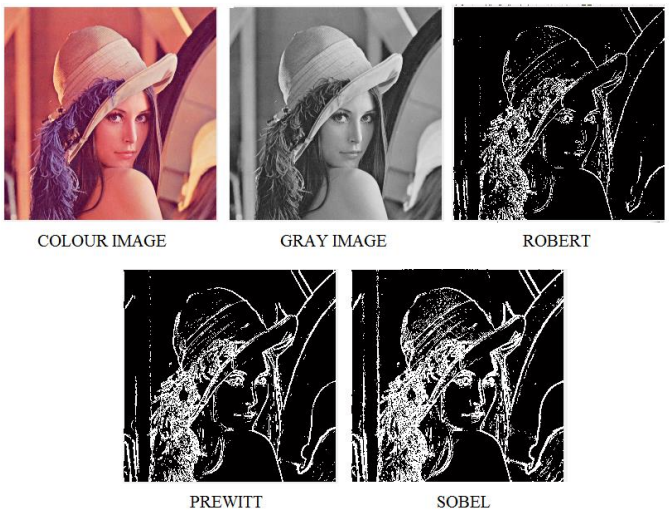

Fig -11: Results for 512×512 Lena color image

Table -3: Proposed design for 512×512 image

Technique	Slices	FFs	LUTs	IOBs
Robert	71	66	91	17
Prewitt	151	152	191	17
Sobel	167	152	188	17

Table -4: Design in [7] for 512×512 image

Technique	Slices	FFs	LUTs	IOBs
Robert	768	1237	1209	32
Prewitt	943	1357	1479	32
Sobel	945	1357	1604	32

From Tables-3 and 4, it is inferred that proposed design utilizes much less resources than that of design in [7]. To get better comparative view a graphical representation of both the designs is shown in Fig- 12. Parameters used in the comparison are occupied Slices, FFs and LUTs.

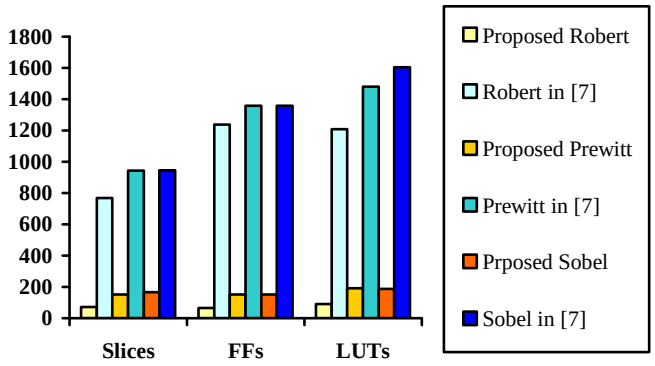

Fig -12: Comparative Analysis for Proposed Design and Design in [7]

5. CONCLUSIONS

The main objective of this paper was to design Classical Edge Detection algorithms which use minimum resources in order to maximize Frequency of operations. Designed Classical operators are more efficient in terms of resource utilization than previous work. These operators are implemented on Spartan-3E FPGA by utilizing hardware co-simulation compilation using XSG. Further, proposed work can be followed to make Canny algorithm design simpler than conventional one.

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