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NOVEL METHODS OF CLOCK GATING TECHNIQUES: A REVIEW

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ABSTRACT- *In this paper the different types of clock gating techniques are applied on 16 bit up-down counter. The various techniques are used for optimizing the power consumption of the sequential circuit designs. It is seen that the clock pulse consumes more power by regular charging and discharging of capacitor load. So, the clock pulse of 16- bit up down counter is gated by using clock gating methodology and designs are simulated for results. These clock gating techniques is implemented on RTL level at VIVADO 2016.4 for synthesis and simulation. The different clock gating techniques are compared to the normal implemented design.*

Keywords- RTL, VLSI, CMOS, Glitches, Gating

I.INTRODUCTION

With the advancement in deep submicron technology power consumption has became the major bottle neck particularly in sequential circuits. The various methodology and design are used to overcome from the faster drainage of battery. The clock gating methods provide effective solution for reducing power dissipation in VLSI circuits.

In VLSI circuit signal power is used for the synchronization of active components. Clock is the major component of power mainly because the clock is given to the most of the circuitry blocks and it switches in every cycle. Hence, the total power used by clock is a substantial component of total power dissipation in a digital circuit [1]. So different types of clock gating techniques is considered for estimation of dynamic power of the designed circuit.

II. LITERATURE SURVEY

The dynamic power is the power that is consumed by a device when it is actively switching from one state to another [2]. Dynamic power occurs due to switching of power consumed while charging and discharging of capacitor load in CMOS inverter [3]. The loads on a device and internal power, consumed internal to the device while it is charging state [4]. The power is directly proportional to the given supply voltage and clock frequency.

$$\text{Power} = V_{dd}^2 . C_L . f . \alpha \quad \ldots\ldots\ldots\ldots (1)$$

Where

V_{dd}= supply voltage

f= Input signal frequency

C_L= Capacitor load

α = Switching activity or activity factor

The dynamic power is the sum of transient power consumption and capacitive load power consumption. Transient power represents the amount of power consumed when the device logic states from bit 0 to 1 or vice versa. Capacitive load power consumption represents the power used to charge the load capacitance [5].

$$P_{dynamic} = P_{cap} + P_{transient} = (CL+C)\, V_{dd}^2 . f . N^3 \quad \ldots\ldots\ldots (2)$$

Where,

C_L= Load Capacitance

C= Internal capacitance

N= the number of bits that are switching

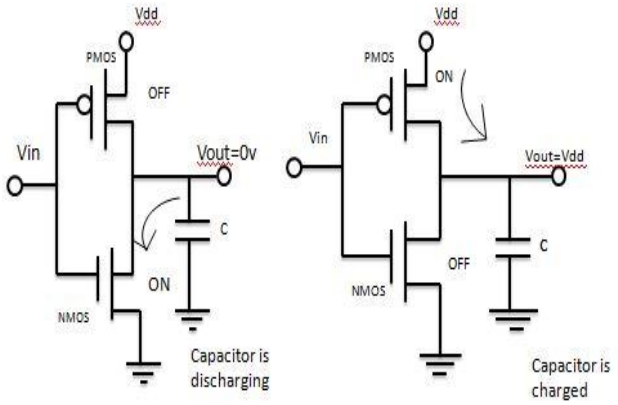

Fig.1.The Dynamic dissipation occurs in CMOS circuit [4].

The CMOS inverter consists of complementary MOSFET design of PMOS and NMOS as shown in figure 1. When the V_{in} is '1' PMOS is ON and NMOS is OFF, the current passes through capacitor charged it and get the output voltage $V_{dd.}$ When V_{IN} is '0' PMOS is OFF and NMOS is ON, The capacitor discharged at that time and gets 0 voltages at output. The power is dissipated through the discharging of capacitor load [4].

III. IMPLEMENTATION OF CLOCK GATING IN 16 BIT UP-DOWN COUNTER

The various types of clock gating methodology is used are as follows-

1. AND GATING-

In AND gating the simple AND gate with enable signal is used to gated the clock with 16-bit up-down counter as shown in fig (2) [5][6][7].

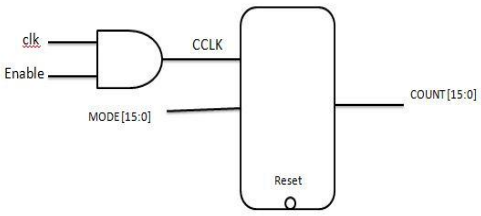

Fig.2. AND Clock gating technique or Latch free Clock gating [5].

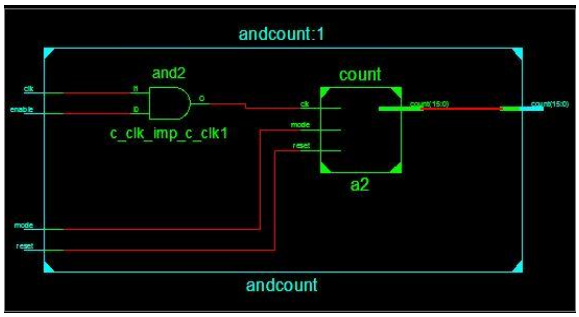

Fig.3. Synthesis of Latch free Clock gating

In the waveform of AND gating the glitches are seen. A glitch occurred when the signal propagate through combinational logic. Before reaching the final steady state value, sometimes intermediate value shows up at the output during the settling phase. It happens because of the different signal paths have different delays. So, when one input reaches the input of a gate while the other input is delayed, the wrong output may occur. Thus, the enable signal is low before the falling edge of clock the gated clock is also terminated at that point.

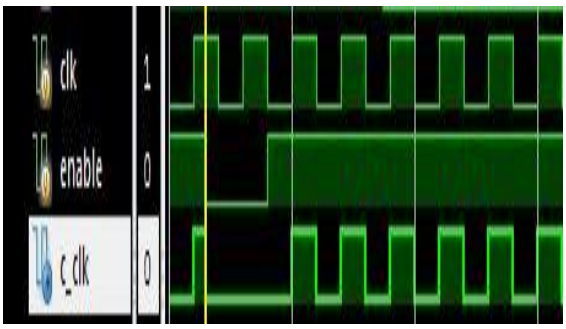

Fig.4. Glitches occurs in AND gating.

2. FLIP FLOP GATING-

The flip flop gating is a technique in which the D Flip-flop or T flip-flop is used with AND gate to gated the clock pulse for the module design. It is used to overcome from the glitches that occur in above design on gated clock. The flip flop implemented at positive edge clock with enable as an input and the output is used as input of AND gate. Then, the gated clock is given to the 16-bit counter [5]

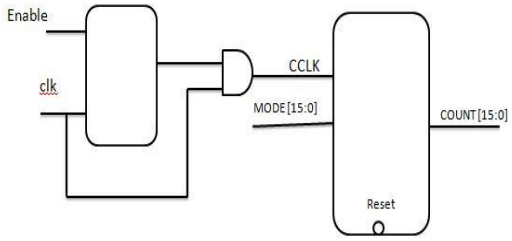

Fig.5. Flip-flop clock gating using d flip flop [5][6]

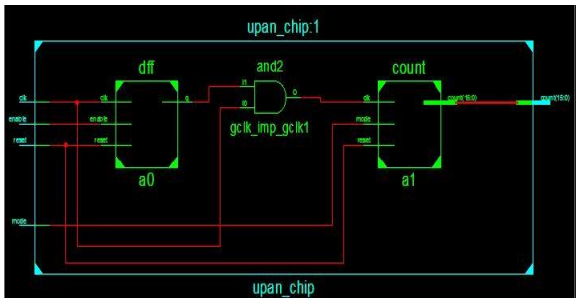

Fig.6. Synthesis of Flip-flop clock gating

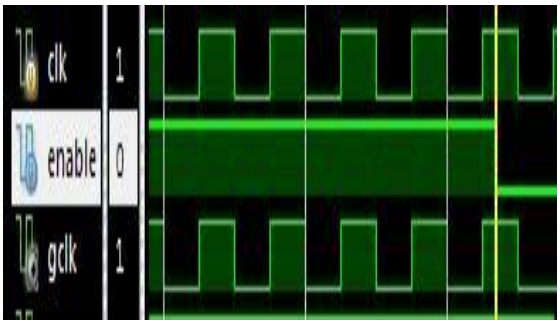

Fig.7. Glitch is removed

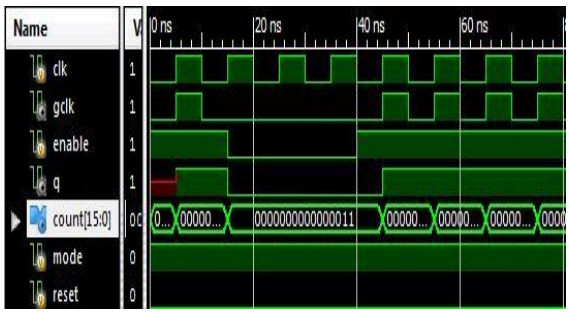

Fig.8. Simulation of Flip-flop Clock gating

3. ADAPTIVE GATING

In the adaptive clock gating technique, the clock enable signal is created. The output signal of flip-flop or the latch is taken as a input of XOR gate with enable signal the output of the XOR gate is the input of the counter module to supply the gated clock pulse of the system [8].

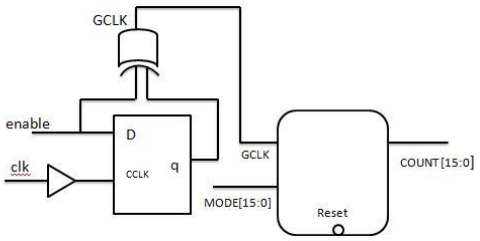

Fig.9. Adaptive Clock gating technique [8]

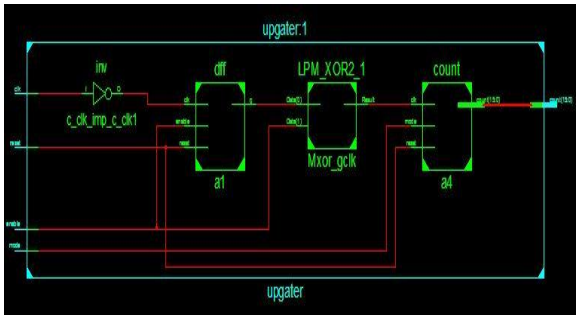

Fig.10. Synthesis of Adaptive clock gating

The signal clock is '1' when the current output and current input have different values. The clock is remains active in this period [8].

4. NEW APPROACH CLOCK GATNG

In this technique, the power is saved in such a way that even target device's clock is ON, the controlling device clock is OFF [7].

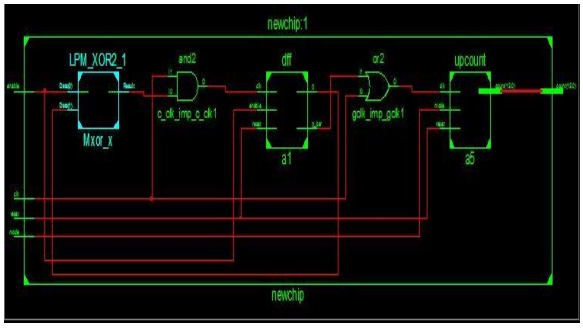

Fig.11. Top level Module design of new approach of clock gating

This design works when input 'enable=1' and simultaneously "GEN=o" hence XOR produces X=1. This goes to the first clock generation that generates the clock for the controlling device (flip-flop or latch). The logic on "AND" gate which have a global clock as an input at another input of a AND gate. The logic will generate a clock pulse that will drive controlling latch when X=1. The next clock pulse, when "GEN=1" in second clock generation logic which is OR gate which has Q and global clock at its input and when Q=0, it generates clock pulse that goes to target device. Since, GEN=1 the XOR gate will produce X=0. Thus, OR gate will produce at CCLK constant LOW until ENABLE turns OFF. This way GCLK will be running and CCLK will be at constant 0. This states that the latch will hold its state without switching [7].

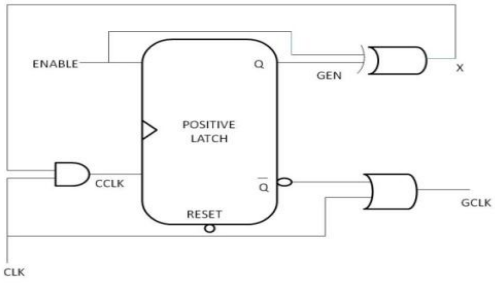

Fig.12. New approach clock gating design [5].

IV. RESULTS

The above mentioned designs are implemented in VIVADO 2016.4 and simulated to calculate the power dissipation in the designs having clock gating approach. The results are mentioned in Table 1.

TABLE 1. Comparison Table for Power Consumption through Clock Gating designs.

	Dynamic Power (W)	Static Power (W)	Total Power (W)
LATCH FREE	16.363	0.143	16.504
FLIP FLOP BASED	16.550	0.143	16.693
ADAPTIVE CLOCK GATING	16.371	0.143	16.514
NEW APPROACH	16.344	0.142	16.486

TABLE 2. Percentage reduction in static and dynamic power consumption having flip flop based design with respect to clock gating designs.

Clock gating technique	Percentage reduction in dynamic power (w)	Percentage reduction in static power (w)	Percentage reduction in total power (w)
Latch Free Based	1.12%	0%	1.132%

Adaptive Clock Gating	1.08%	0%	1.072%
New Approach	1.24%	0.69%	1.24%

The table 1 exhibits power consumption of various clock gating techniques. It can be easily seen from table 2 that the most suitable is new approach clock gating technique where the total power consumption is improved by 1.24%. The maximum power consumption is seen in adaptive clock gating where dynamic power consumption is 16.371 W and total power consumption is 16.514 W. The latch free clock gating is taken 16.363W as a dynamic power and 16.506W as its total power consumption that is greater than the new approach clock gating method and the flip flop taken 16.550W as dynamic power consumption is highest among all the clock gating design used in paper and its total power consumption is 16.693W. It can readily be shown in fig 13 and fig 14 that new approach clock gating method is most rigorous and has minimum static and dynamic power dissipation among the various methods used in analysis.

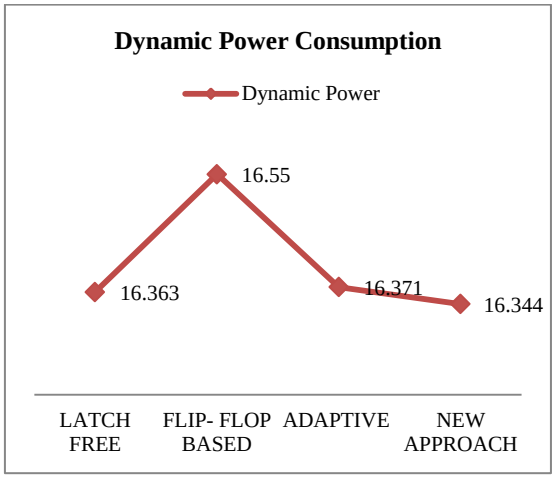

Fig.13. Bar Graph of Dynamic Power Consumption though Clock Gating

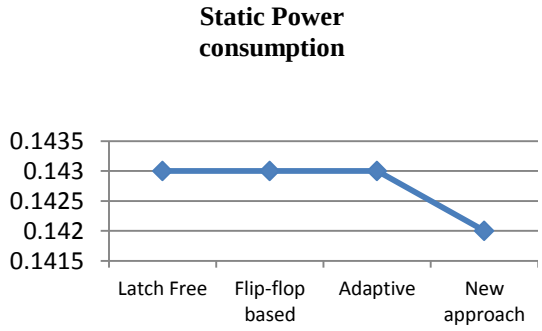

Fig.14. Bar graph of Static power consumption Though Clock Gating

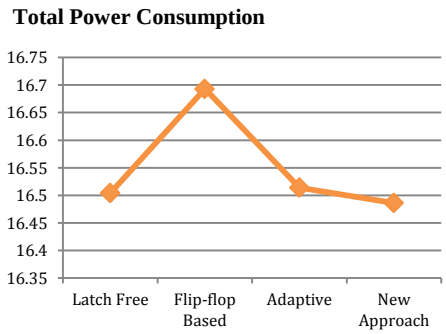

Fig.15 Bar Graph of Total Power Consumption Through Clock Gating Techniques

V. CONCLUSION

In this research paper five different types of design are implemented by clock gating techniques. The first design AND gating suffers from problems of glitches in its waveform. To overcome from this issue flip-flop based clock gating technique is used to gated the clock by flip-flop and "AND" gate which removes the problem of glitches. Then the adaptive clock gating is used but it holds the value in the waveform and works only on falling or rising edge of the clock. The new approach design fulfills all the parameters that we want and reduced the power dissipation by 1.24%. It gated the clock not only to the target device but also the controlling device and has the low power consumption in all design implemented in this paper.

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