

DESIGN AND SIMULATION OF A CMOS FUNCTION

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Abstract – Implementing the function $F = \overline{(A + B)}C$ using CMOS logic i.e. pull- up and pull- down combination and testing the implemented transistor based logical circuit using DSCH software aid.

Key Words: DSCH software, pull- up and pull- down network, CMOS, NAND, NOR.

1. INTRODUCTION

There are many transistor based functions which can be developed using CMOS logic. Significantly working with their design and accomplishing their switching performance via testing them using DSCH software, we able to study their working on all possible logical input combinations.

Here I am implementing the function $F = \overline{(A + B)}C$ and testing it using DSCH software.

2. FUNDAMENTAL OF CMOS DESIGNING

A CMOS function is fundamentally working on a basic combinational network of pull- up and pull- down network. The pull- up network is of pmos transistors and pull- down of nmos transistor combinations.

NAND combination of pmos transistors in the pull- up network should be in parallel connection and nmos transistors in the pull- down network should be in series.

NOR combination of pmos transistors in the pull- up network should be in series connection and nmos transistors in the pull- down network should be in parallel.

Every input of the function represents a transistor separately in pull- up and pull- down network and is designed based on the NAND and NOR combination of CMOS logic.

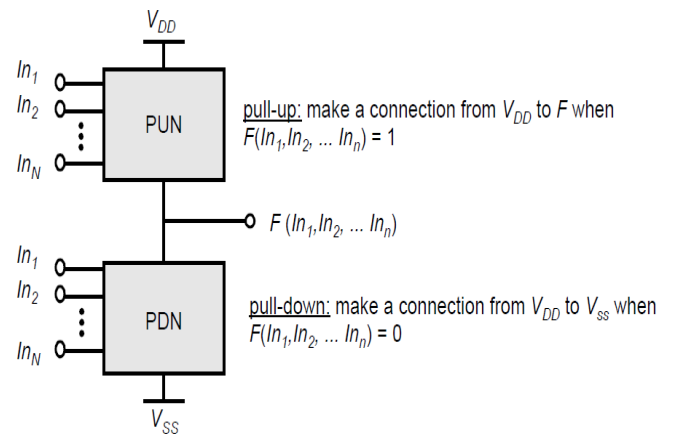


Fig.1. Pull- Up and Pull- Down Network

3. DESIGNING OF CMOS $F = \overline{(A + B)}C$

The function has three input variables i.e. A, B and C respectively. The function with a output F has A and B in NOR logic with along with them in NAND logic. Designing them with the fundamental of CMOS design topology.

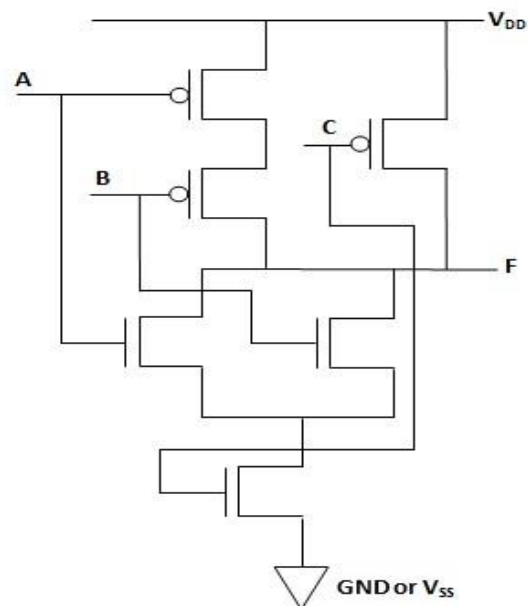


Fig.2. CMOS circuit for the function $F = \overline{(A + B)}C$

4. TRUTH TABLE OF THE CMOS FUNCTION

Input A	Input B	Input C	Output F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table.1. Truth Table for the function $F = \overline{(A + B)}C$

The truth table above shows all the possible logical input combinations which will be tested using DSCH software.

5. Analysis on DSCH Software

The CMOS circuit thus designed is implemented using DSCH software and the observance on the transistor switching behavior can also be seen for every input logical combination.

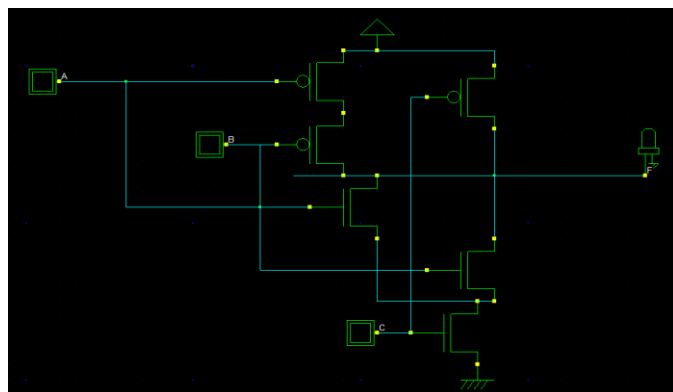


Fig.3. Implemented CMOS circuit for the function $F = \overline{(A + B)}C$ in DSCH software

1. With inputs A=0, B=0, C=0 and output F=1 i.e. ON

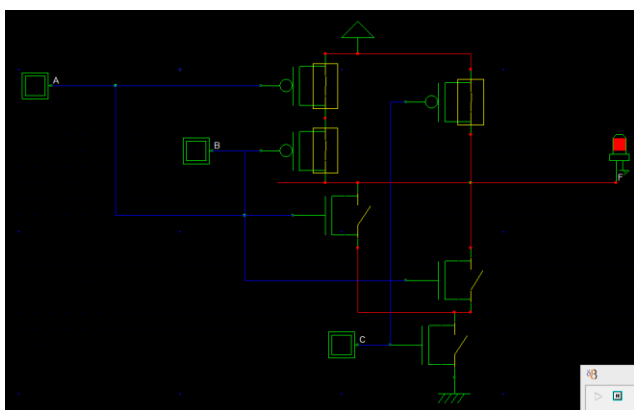


Fig.4.1.

2. With inputs A=0, B=0, C=1 and output F=1 i.e. ON

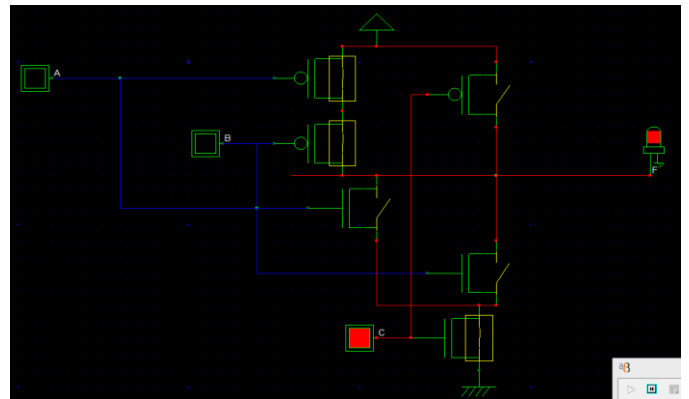


Fig.4.2.

3. With inputs A=0, B=1, C=0 and output F=1 i.e. ON

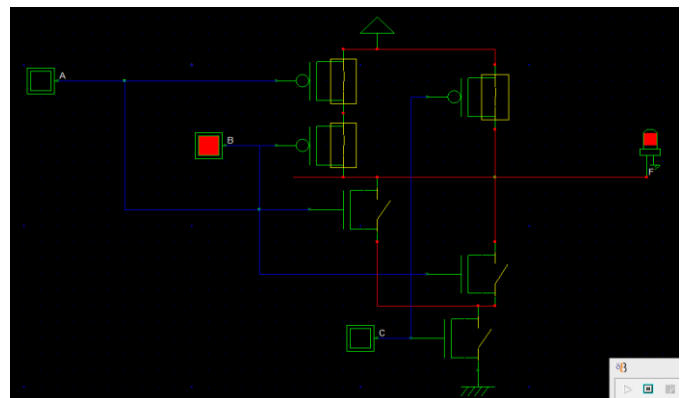


Fig.4.3.

4. With inputs A=0, B=1, C=1 and output F=1 i.e. ON

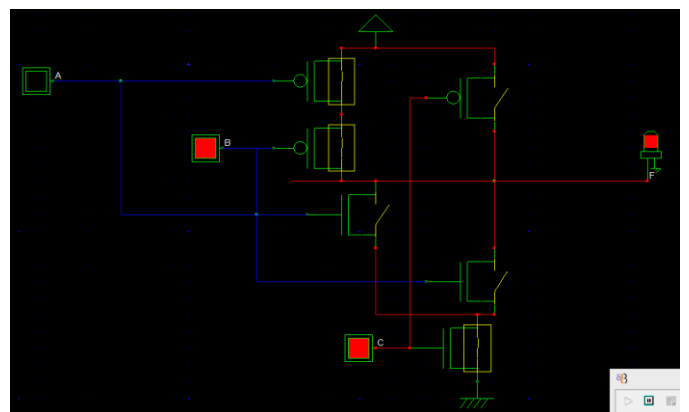


Fig.4.4.

5. With inputs A=1, B=0, C=0 and output F=1 i.e. ON

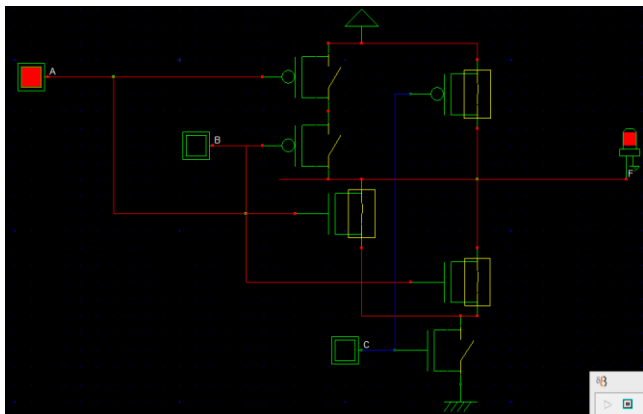


Fig.4.5.

8. With inputs A=1, B=1, C=1 and output F=1 i.e. ON

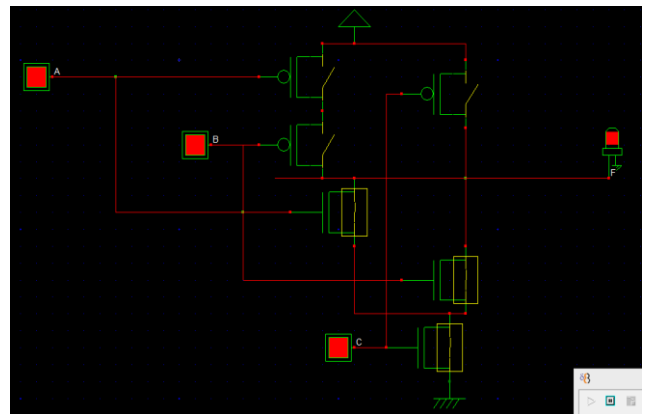


Fig.4.8.

6. With inputs A=1, B=0, C=1 and output F=1 i.e. ON

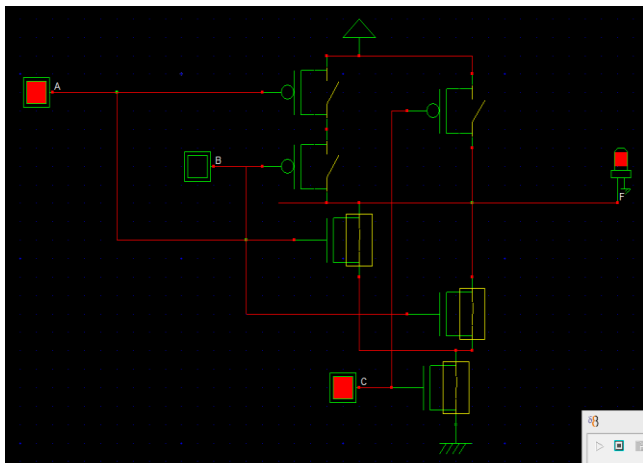


Fig.4.6.

7. With inputs A=1, B=1, C=0 and output F=1 i.e. ON

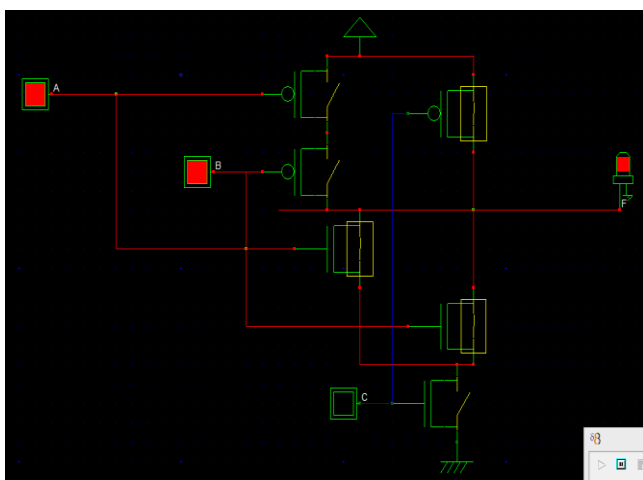


Fig.4.7.

6. FUTURE SCOPE

Engineers and Engineering students can easily be able to design their own CMOS circuits and implement it. It will become very easier to showcase their engineering work as per the global platform.

7. CONCLUSION

It is observed that designing of the CMOS circuit of the function $F = (A + B)C$ is accomplished and implemented as per various input possibilities. The circuit is found to be ON in all the input configurations. Through this the switching behaviour of transistors at different inputs is observed, leading to coverage of digital integrated transmission paths in digital electronics.

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BIOGRAPHY



Mr. H. Abdul Wasay, working as an Assistant Professor in Dept. of Electronics and Communication, Deccan College of Engineering and Technology. He's field of interest are Analog and Digital Electronics. He has lectured and thought various analog and digital electronic subjects. He has also organized, presided National conferences.