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Design of area efficient digital FIR filter using MAC

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Abstract - *Due to the explosive growth of multimedia application, the demand for high performance and low power DSP is getting higher and higher. Most widely used fundamental device performed in DSP system is FIR digital filter. Being the critical part of the theoretical advancement and implementation, FIR filter design continues to be a critical area of on-going research activities. for better performance it is good direction to optimize power consumption ,reduction in computational complexity as well as area optimization of FIR digital filter.*

Key Words: **FIR filter, Area optimization, MAC, FPGA.**

1.INTRODUCTION

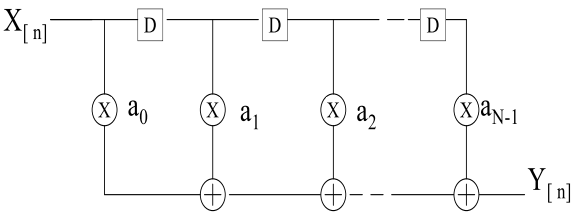
The speed of developments in electronic technology is taking place tremendously. Now days, Digital Signal Processing (DSP) is used in various applications such as speech processing, digital versatile disk, portable video systems/computers, digital audio, multimedia and wireless communications, video compression, digital set-top box, cable modems, digital radio, transmission systems, radar imaging, acoustic beam formers, global positioning systems, and biomedical signal processing. The field of DSP has always been driven by the advances in DSP applications and in scaled very-large-scale integrated (VLSI) technologies. Therefore, at any given time, several challenges are imposed on the implementations of the DSP systems. These implementations must satisfy the enforced sampling rate constraints of the real-time DSP applications and must require less space and power consumption. DSP computation is different from general-purpose computation in the sense that the DSP programs are non terminating programs. In DSP computation, the same program is executed repetitively on an infinite time series. The non terminating nature can be exploited to design more proficient DSP systems by exploiting the dependency of tasks both within iteration and among multiple iterations. in addition, long critical paths in DSP algorithms limit the performance of DSP systems. Digital filters are essential elements of DSP systems. Digital filters are classified into two categories as: Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter. Though FIR filters have linear phase property, low coefficient sensitivity and stability compare to IIR filter they have power consumption more than IIR filter. In many applications it is often advantageous to employ finite impulse response (FIR) filters, since they can be designed with exact linear phase and reveal no stability problems (Mitra, 2006). However FIR filters have a computationally more intensive complexity compared to infinite impulse response (IIR) filters with correspondent magnitude responses. During the past several years, many design methods have been proposed to reduce the complexity of the FIR filters.

1.1 Digital Filter

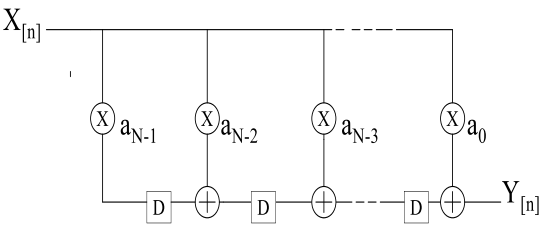
The output of a FIR filter is described by the following equation:

$$y[n] = a_0 x[n] + a_1 x[n-1] + \ldots + a_{N-1} x[n-N]$$

Where x[n] is the input signal,y[n] is the output signal. a_i are the filter coefficients, also known as tap weights, that make up the impulse response. The output y of a FIR system is determined by convolving its input signal x with its impulse response a.



(a)Direct form



(b)Transpose form

Fig -1: Various Realizations of FIR Filters

In general, there are two popular forms to realize FIR filters: direct and transposed shown in Fig. 1. In the direct form, there are delay units between multipliers. At a time, the present filter input, x(n), and N-1 previous samples of the input are fed to each multiplier input, and the filter output y(n) is the sum of product of every multiplier. In the transposed form, however, delay units are placed between adders so that the multipliers can be fed simultaneously. For the computation of FIR filter, we have to convolve the input data with filter coefficient; convolution process contains number of multiplication and addition.

2. LITERATURE REVIEW

Computational complexity of Digital Filter structures is given by total number of multipliers and total number of two input adders required for its implementation, which indicates cost of implementation. For the applications demanding low power and high speed Digital Filters, various approaches developed so far to reduce the number of multiplications and additions are discussed below.

Strength reduction at algorithmic level can be used to reduce the number of additions and multiplications. Applications involving multiplication by constant are common in digital signal processing. A first solution proposed to optimize multiplication by constant was the use of constant recoding, such as Booth's. This solution just avoids long strings of consecutive ones in the binary representation of the constant. Another solution proposed designing a digit-serial MCM operation with minimal area at gate-level and presents the exact formalization of the area optimization problem as a0-1 Integer Linear Programming (ILP) problem[3].

In the paper titled "Low-Complexity Constant Coefficient Matrix Multiplication Using a Minimum Spanning Tree Approach", Oscar Gustafsson, Henrik Ohlsson, and Lars Wanhammar proposed an algorithm for low complexity constant coefficient matrix multiplication based on differences. It uses a minimum spanning tree (MST) to select the coefficients, which warrants low execution time as an MST can be found in polynomial time In general, optimization techniques usually used for multiplier less filter design are complex, can require long run times, and provide no performance guarantees (Koter at al., 2003). Gordana Jovanovic Dolecek and Sanjit K. Mitra in their paper titled "Computationally Efficient Multiplier-Free Fir Filter Design", proposed simple efficient method for the design of multiplier-free.FIR filters without optimization. The method uses the rounding to the nearest integer of the coefficients of the equiripple filter which satisfies the desired specification. Considering that the integer coefficient multiplications can be accomplished with only shift-and-add operations, the rounded impulse response filter is multiplier-free [2].

In a FIR context, a MAC is the operation of multiplying a coefficient by the corresponding delayed data sample and accumulating the result. FIR usually requires one MAC per tap. High speed and high throughput Multiplier-Accumulator (MAC) unit that consumes low power, which is always a key to achieve a high performance digital signal Processing system. A low power MAC unit can be designed and implemented using block enabling technique to save power. In any MAC unit, data flows from the input register to the output register through multiple stages such as, multiplier stage, adder stage and the accumulator stage. Within the multiplier stage, further, there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. In block enabling technique, the delay of each stage is obtained. Every block gets enabled only after the expected delay. For the entire duration until the inputs are available, the successive blocks are disabled, thus saving power [8].

3. PROPOSED METHODOLOGY

In many applications it is often advantageous to employ finite impulse response (FIR) filters, since they can be designed with exact linear phase and exhibit no stability problems (Mitra, 2006). However FIR filters have a computationally more intensive complexity compared to infinite impulse response (IIR) filters with equivalent magnitude responses. This paper aims to design an area efficient digital filter on FPGA .which has following steps described below.

3.1 Filter Specification

The first step in designing digital filters is to obtain the filter specification. The specification is developed based on the technical requirements to the filter and the possibility of hardware realization. A filter specification is a technical specification that determines the pass-band and stop-band frequency ranges and acceptable attenuations in those ranges. There are four basic types of filter specifications, one for each of the four basic filter types: low-pass, high-pass, band-pass and band-stop. Generally, filter specifications determine pass band and stop band frequency ranges, desirable signal attenuations (gains) at those ranges, approximation methods for the filter design, and hardware implementation requirements. FDA tool is used to design and analyse the filter for specification as shown in figure 2.

Order N=17

Pass band Frequency Fpass = 9000Hz

Stop band Frequency Fstop = 11000Hz

Sampling Frequency Fs = 48000Hz

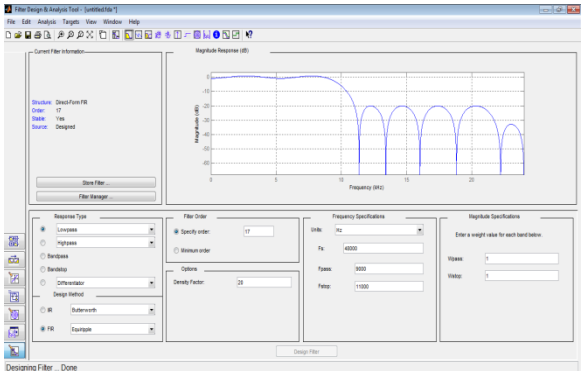


Fig-2 Filter specification in FDA tool

3.2 Filter Coefficient Generation

This design is exported to MATLAB workspace for generation of coefficient since coefficients are decimals, among them some are negative therefore binary representation of coefficient requires more bits as compared to integer. so coefficients are rounded to nearest integer value that can be represented in 8 bits only .This method reduces complexity of MAC unit considerably by avoiding design of two's compliment circuit further area requirement of multiplier is also reduced. Following table shows actual coefficient and rounded coefficient.

Table -1: Coefficient optimization by rounding to nearest integer.

coefficients	actual	After rounding off
h_0	-0.0602	5
h_1	-0.0240	2
h_2	0.0432	3
h_3	0.0348	3
h_4	-0.0196	2
h_5	-0.0916	7
h_6	-0.0130	1
h_7	0.1928	15
h_8	0.3879	30
h_9	0.3879	30
h_{10}	0.1928	15
h_{11}	-0.0130	1
h_{12}	-0.0916	7
h_{13}	-0.0196	2
h_{14}	0.0348	3
h_{15}	0.0432	3
h_{16}	-0.0240	2
h_{17}	-0.0602	5

3.3 Design of FIR filter using single MAC unit

In digital signal processing, the multiply–accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier accumulator (MAC or MAC unit). The operation itself is often called as a MAC or a MAC operation. The MAC operation modifies an accumulator as:

a□a □□□b□c□

This paper proposed an area efficient FIR filter by using a single MAC unit. Following block diagram shows construction of MAC based FIR filter.

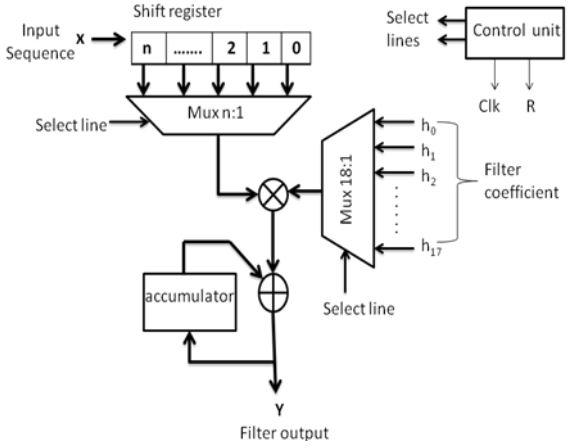


Fig -3: Proposed Architecture of FIR filter using MAC

The architecture of MAC based FIR filter involves design of following elements

a. **Shift register:** This is serial in parallel out shift register. The effect of each clock pulse is to shift the data contents (x) of each stage one place to the right.

b. **Multiplexer:** multiplexer or mux is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. Proposed architecture involves design of two mux one is to select data(x) and another to select filter coefficients (h). Selected input is depending upon the logic on selector pins.

c. **Multiplier:** The output of two multiplexer is fed to multiplier. this multiplier takes 8 bit input and produces 16 bit output.

d. Adder: It adds multiplier output with previous result stored in accumulator. Output of adder is taken as filter output for current sample and also fed to the accumulator for next input sample.

e. Accumulator: It is 32 bit D flip flop used to hold the result. with each clock existing value in accumulator is replaced by new one.

f. Control unit: This unit is of great importance as it controls all clock, reset signal associated with various elements as shown in fig 3 as well as logic on selector pins.

4. CONCLUSIONS

The FIR filters are widely used in signal processing and can be implemented using Programmable digital processors. The main focus of this paper is to introduce method of implementing an area efficient digital FIR filter. It can be achieved through filter coefficient optimization technique, using single MAC unit and by selecting parallel form(transpose) among two structures as it involves addition followed by multiplication thereby reducing hardware cost. Proposed work seems to be a good direction in area optimization of digital filter.

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