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Comparative Study of Delay Line Based Time to Digital Converter Using FPGA

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Abstract - *Many time-of-flight (TOF) applications need measurement of time difference between two events. A time to digital converter is suitable for these kinds of applications because it measures time difference between two pulses and gives time difference as a digital output code. However basic TDC needs much higher clock frequency to measure smaller time differences in terms of picoseconds. High clock frequency leads to major power dissipation and unstable clock which are not desirable. Different architecture of delay lines which can be used with TDC to measure smaller time interval with less clock frequency has been studied and compared in this paper. It is useful in improving performance of measurement. FPGA based TDC can be used because of fully digital structure of TDC and FPGAs provides flexibility and low cost.*

Key Words: Time to Digital Converter (TDC), Field Programmable Gate Array (FPGA), Vernier Delay line, Low Resolution, Time of Flight (TOF) applications, time interval measurement.

1. INTRODUCTION

TDC has several applications in different engineering fields. TDC is useful in measurement of the velocity of the moving particles in many physics experiments, unknown fiber length, the thickness of the chemical coating on a substrate can also be measured using TDC[4]. In the field of particle and high energy physics, TDC is mostly used for requirement of precise time interval measurement. In electronics it gives advantage in utilization of measuring the time interval between two pulses.

TDC is most important application in time of flight (TOF) application. TOF is a method used to measure distance between sensor and object, based on the time difference between the emission of signal and its return to the sensor, after being reflected by an object [2]. Application of medical, space, nuclear science also needed measurement between two events. In digital phase locked loop, TDC serves as phase detector.

For meeting time requirements of different applications ASIC- based chips are can be designed but design of such chips is costly, complicated and time consuming.

Field Programmable Gate Arrays (FPGAs) provide configurable logic blocks (CLBs) that can behave like any logic circuits. To implement variety of circuits, FPGAs provide very flexible way [7]. Therefore, Timing devices based on FPGAs are becoming very popular. It has several advantages like lower cost, and faster development cycle. It has some disadvantages like delay variation due to Process, voltage & control, unpredictable place & route and no direct control over delays. Circuit delays of FPGA devices are highly dependent on wiring and routing inside an integrated circuit, which is why manual placement and routing of signals is essential for accurate measurements. The resolution of measurement is also dependent on the technology used, and with more recent deep sub-micron technologies, higher resolution can be acquired.

2. PRINCIPAL OF OPERATION

A TDC converts a time interval between different pulses into digital numbers. A TDC has two inputs, a start which arrives first and a stop which comes later. Difference between positive edges of start pulse to positive edge of stop pulse is called as input time interval (T_{in}).

The most basic TDC is as shown in figure 1. Counter will enable when start signal is arrived and disable when stop signal is arrived. Counter will count number of clock cycles taken to measure input time interval. By multiplication of counted numbers by counter with reference clock frequency unknown input time interval can be determined [9]. This architecture also called as direct gating. In this TDC, the start and stop signals are not synchronous with reference clock signal, while the counter counts the number of cycle which can introduce an error in the time information. Its waveforms are as given figure 2.

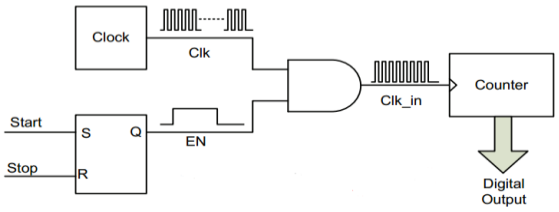

Fig -1: Counter based TDC (Direct gating)

There are some parameters that needs to taken into account in TDC.

1. Minimum interval - The minimum time between consecutive pulses.
2. Minimum dead-time - The minimum time between the stop pulse and the next start pulse.

3. Resolution - It is defined as the minimum unit of the time measurement.

The resolution of this device is limited by the speed of the reference clock and it cannot be higher than a single clock period. For getting higher resolution, high clock frequency is needed which leads to major power dissipation. Constraints like on chip clock frequency of the particular device is the key factor in limit the application of this kind of architecture.

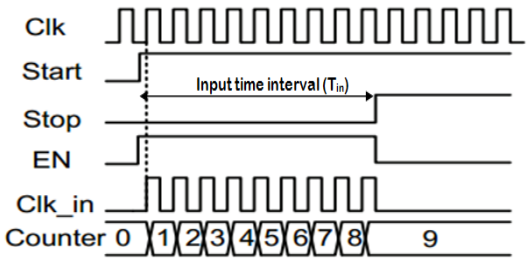

Fig -2: Waveform of counter based TDC

3. TYPES OF DELAY LINE

To overcome issue of high clock frequency and high power dissipation, different delay line architecture which is discussed in different literature has been studied and presented here.

1.1 TDC Based on a single Delay line

In this architecture, buffers are used as a delay cells. The TDC based single delay line is suitable for technology scaling because of its fully digital organization [9]. Six buffers as delay cells are embedded into a charge-pump Delay Locked loop (DLL) as shown in figure 3. Six delayed clocks with different delay can be generated by this method. A hit signal is mainly works as a sampling clock. The states of the six clocks will be samples into hit register when edge of the hit signal is positive. The timing diagram is illustrated in Figure 4.

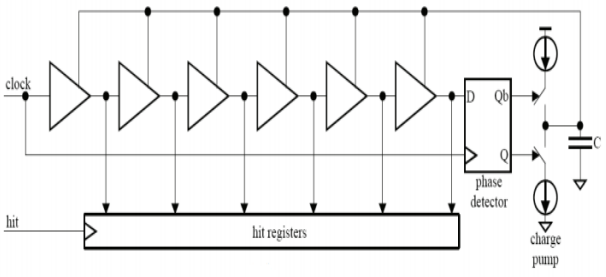

Fig -3: Single delay line architecture

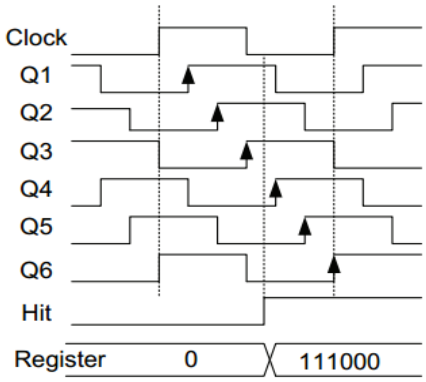

Fig -4: Waveform of Single delay line

The resolution of the TDC using a single DLL is given by

$$\text{Resolution} = T_{clk}/N \quad (1)$$

Here,

T_{clk} = Period of the clock

N = Number of delay cells in the DLL

Resolution of TDC based on single delay line is mainly dependent on clock period as well as number of buffers embedded into delay line. In FPGA clock period is limited by technology used. So by increasing number of delay elements can be useful. But Minimum number of delay cells and its delay time is also technology dependent. Moreover, there is also a problem of mismatching a delay cells in this method which does not allow integrating large number of delay cells. So, achieving higher resolution can be difficult.

To improve the time resolution of this architecture, one can try to further divide the delay of the delay cells by using an array of delay lines or other techniques.

1.2 TDC Based on array of Delay line

For eliminating the issue of single delay line array of delay line can be used in which several Delay Locked Loops (DLLs) are employed in the array. Resolution is depends on time difference between delay cells in delay line. The reference clock is propagated by the array of DLLs. In this method, power dissipation and area will be high because use of several DLLs in array. For overcome this issue tapped delay line and vernier delay lines are widely used approaches [9].

The resolution of the TDC based on the DLL array is as given below

$$\text{Resolution} = T_m - T_n \quad (2)$$

Here,

T_m, T_n = delay time of the delay cell in both DLLs

m, n = the number of the delay cells with the delay time of tm and tn.

1.3 TDC Based on Tapped Delay line

As shown in above figure 5, tapped delay line is consisting of one latch chain and one buffer chain. Start signal is given to buffer chain and stop signal is given to the latch chain. Delay of latch chain and buffer chain is different. In this architecture resolution is depends on difference of the delays between latch and buffer. This architecture is more area efficient than single as well as vernier delay line.[7]

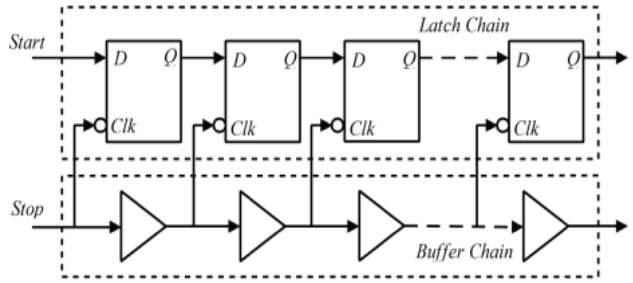

Fig -5: Tapped delay line architecture

Achieving higher resolutions will require more effort in terms of optimization of delay element, placement and routing of delay cells in this architecture because the elements used are of different types.

1.4 TDC Based on vernier Delay line

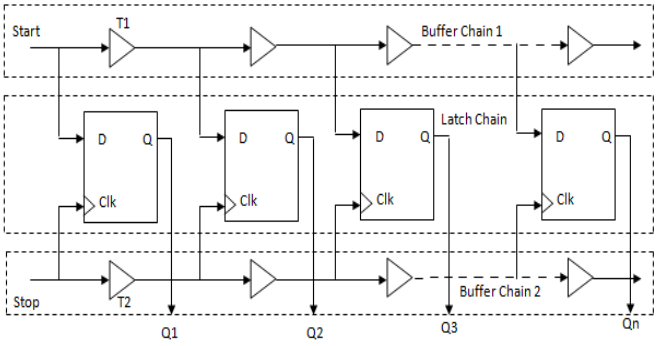

Fig -6: Vernier delay line architecture

The Vernier delay line is shown in Figure 6. The principle of the measurements originates from the Vernier ruler[9]. Two delay lines are required. As shown in above figure, vernier delay line is consist of one latch chain and two buffer chain. Latch chain is mainly used for holding the result. Start signal and stop signal both are given to the different buffer chains. By using the vernier method, the small time difference can be measured.

To realize the TDC using vernier delay line, two DLLs should be employed. Thus, the synchronization of the multiphase clock is very important in this circuit.

Resolution of vernier delay line is equal to delay difference between two delay times (T1 and T2) of the delay cells in two delay line.

This architecture is more area efficient than single delay line and less area efficient than tapped delay line. Compared to the tapped delay line TDC this method requires more area in FPGA, but achieving finer resolutions is easier as the delay elements used are of the same type [7].

1.5 Gated ring oscillator based TDC

Gated ring oscillator based delay line contains gated ring oscillator, many counters and arbitrary adder as shown in figure 7. This TDC operates only when the "Enable" signal is high level and stops when this signal is at low level. The outputs of the gated ring oscillator can be used as the clocks which drive the counter to counting numbers [9]. Counter will get reset when the enable signal is at low level.

Binary adder will obtain the total number of all counters. And the measured time interval will be proportional to sum of counted numbers by binary counter.

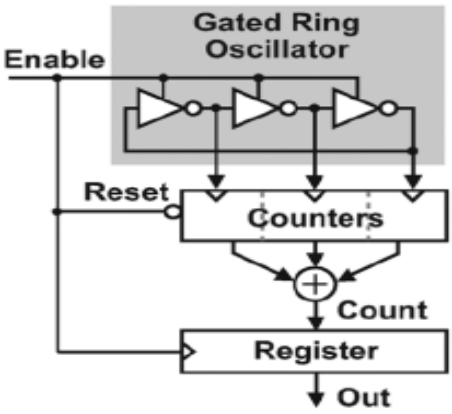

Fig -7: GRO based TDC

1.6 TDC based on pulse shrinking delay line

In pulse shrinking delay line, non-homogeneity is used to to create delay line. The architecture and the operational principle are as shown in Figure 8. In this architecture, a Reset signal is used to ensure the T_{out} is at Low level at the beginning. The input time interval is shrieked with each cycle in the delay line with a fixed width. The output of the delay line is then feedback to the input to AND gate for circular operation. A high-resolution counter is driven by Tout and generates digital outputs which are proportional to the measured time interval [9].

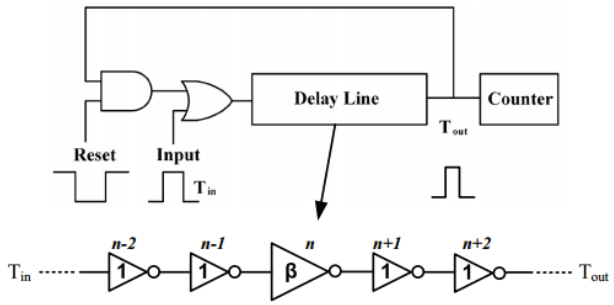

Fig -8: Pulse shrinking delay line

In this kind of delay line, inverters are used as delay cells and two types of inverters are necessary. First type can be the standard inverter with the gain of one unit. The second type is the inverter with the gain of β unit. Because of the difference of the input capacitance and equivalent ON resistance, for fixed time interval pulse will be shrinking. This shrinking delay interval depends on the dimension of the transistors, threshold voltage, power supply, temperature and other parameters.

Pulse shrinking delay line can be implemented in FPGA as well as standard CMOS technology whose cost is much higher than FPGA.

1.7 TDC based on Vernier ring oscillator delay line

The important element of this design is two precise retrigger-able ring oscillators of very small difference in time periods (Δτ). These oscillators are used to determine the time difference between two pulses START and STOP, as shown in Figure 9. The *Start* and *Stop* pulses will enable the slow and fast oscillators respectively. The slow oscillator (time period T1) is triggered by START and the fast oscillator (time period T2) is triggered by STOP. In this technique, T2 < T1 and STOP arrives after START, at some point the rising edge of the fast oscillator will coincide with rising edge of the slow oscillator. This coincident will be detected by a phase detector. In this technique, slow oscillator and fast oscillator will serve as a clock coarse counter and fine counter respectively and the number of clock pulses (n1 and n2) will be counted. These counters will stop counting when the phase detector detects the phase coincidence of the oscillators [8, 21].

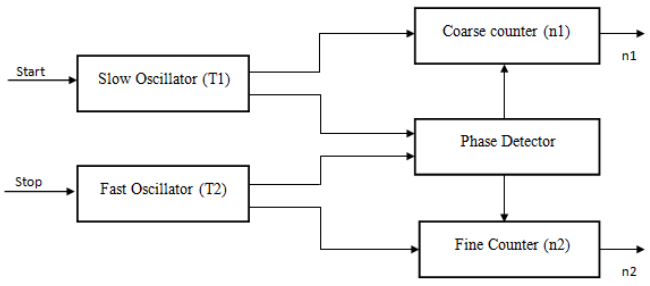

Fig -9: Vernier Oscillator delay line

Input time interval can be determined by equation:

$$T_{in} = T_1 (n_1) - T_2 (n_2) \quad (3)$$

Here,

T_1, T_2 = Time periods of slow clock and Fast clock respectively

n_1, n_2 = Counted numbers of coarse counter and fine counter respectively

This equation also depends on the circuit used for phase detection. For different phase detector circuit equation can be varied.

Benefit of using the oscillators is that it reduces the matching requirements on the delay buffers used in vernier delay line. This feature is very useful to reduce the temporal uncertainties of Vernier delay line based TDCs which is mainly caused by delay variation of buffers [21].

Disadvantage of this architecture is that it takes so many cycles to complete a single time interval (longer dead time). Conversion time is also high in this type of delay line than other delay lines which can detect time interval every cycle.

Waveforms of vernier delay line are shown below:

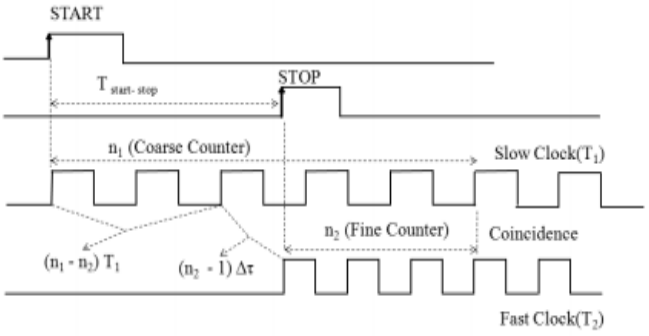

Fig -10: Waveform of Vernier ring Oscillator delay line

1.8 4xOversampling method

In this method, single delay line with four buffers which can give exactly 90 degree phase shift has been used [2]. Delay locked loop has been used to achieve exact 90 degree phase shift for this technique. Delay Locked Loop provides constant phase shift to output clocks. In figure 11, DLL has a Phase Detector which measures the phase error and to convert this information into voltage charge pump is required. Clock signal is given to the delay element. In this technique, four phase shifted clocks (0, 90,180, 270 deg) are generated [2]. This four shifted clocks works as a clocks which triggers four different counters. Resulting count has four times higher resolution than reference clock frequency [2].

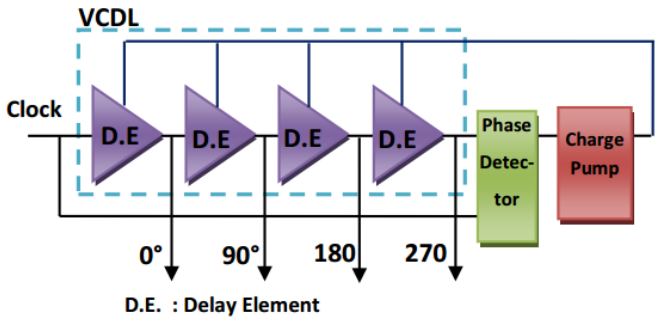

Fig -11: Delay line based on 4xOversampling method

1.9 Tapped delay line with use of multiplexer

The main advantage of vernier delay line over tapped delay line is that vernier delay line has same delay elements for giving delay in both delay lines rather, tapped delay line approach has different delay elements for both delay line which requires careful delay matching between latch and buffer chains. But tapped delay line is more area efficient as it uses fewer elements than vernier delay line [7]. In this technique, same element (multiplexer) has been used as latch and buffers as shown in figure 12. By using only a same element as latch and buffer, it could possible to narrow down the delay difference. Therefore use of multiplexers instead of both latch and buffer is much useful [7]. Carry chain multiplexers with dedicated routes can be used in FPGA for creating this kind of design.

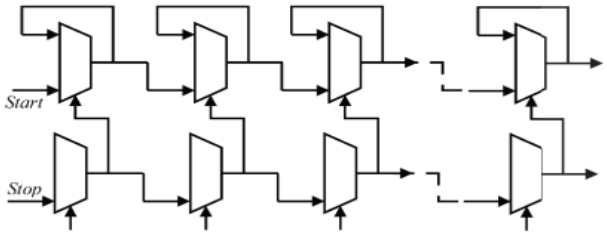

Fig -12: Tapped delay line by multiplexer

The main advantage is that a multiplexer can be easily configured to behave as a buffer as well as a latch, just by changing the way the output is connected. This allows the two parts of the chain to be very precisely matched. It can be also called as hybrid approach. The latch and buffer chains are based on the Tapped Delay Line approach, but the individual delay elements are realized using the same underlying hardware, thus giving delay matching similar to the VDL method [7].

Table -1: Comparison of architecture in terms of resolution

Sr. No.	Architecture	Minimum Resolution
1	Counter based TDC	~1 ns
2	Single delay line	~100 ps
3	Array of delay line	~50 ps
4	Tapped delay line	~10 ps
5	Vernier delay line	~10 ps
6	Ring oscillator based delay line	~100 fs
7	Pulse shrinking delay line	~1 ps
8	Vernier Ring oscillator delay line	~10 ps

4. ADVANTAGES AND DISADVANTAGES OF ARCHITECTURE

Table -2: Advantages and disadvantages of architecture

Sr. No.	Type	Advantages	Disadvantages
1	Counter based TDC	Very simple architecture, Easy to design, less area requirement	Very high frequency is needed to achieve smaller unit of resolution
2	Single delay line	Less frequency for high resolution, Only one DLL required	High number of delay cells required for high resolution
3	Array of delay line	Less number of delay cells are required as compared to single delay line	High area, High power dissipation due to multiple DLL
4	Tapped delay line	Clock is not required, High resolution can be achieved	Mismatching of delay due to different element used as delay cells
5	Vernier delay line	Mismatching of delay is low due to same delay	Component variant delay due to many

		elements used as delay cells, High Resolution can be achieved, Clock is not required	buffers in one delay line
6	Vernier Ring oscillator based delay line	Component invariant delay due to use of oscillator	Longer dead time
7	Ring oscillator based delay line	High resolution	High area

5. CONCLUSIONS

In this paper we have discussed basic of Time to digital converter. We also tried to focus on different types of delay line based TDCs. Many delay line algorithms are available for improving the resolution of TDC. Depending upon the required resolution, we can select the appropriate delay line measurement technique to design time to digital converter. Based on design complexity, minimum required resolution and technology used, we can conclude that vernier ring oscillator based delay line is more suitable. It can also be easy to implement on FPGA because of its fully digital circuitry.

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