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Performance Evaluation of Various CMOS Full Adder Designs: A Review

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Abstract - *In VLSI systems like microprocessors and application-specific DSP architectures, the basic arithmetic operation which is extensively used is 'Addition'. The overall performance of most of the systems is determined by the adders. Power consumption, speed and area are important but conflicting design aspects. Many researchers have worked on full adder designs using various technologies. Present paper deals with exhaustive review of literature based on full adder designs.*

Key Words*: *Full adder, Gate diffusion input, MAC, PDP, Propagation delay.

1.INTRODUCTION

Addition is one of the fundamental arithmetic operations, which is used extensively in many VLSI systems. Adders determine the overall performance of the circuits. There is a need to find out high performance full added circuits, which can be used to design more complex circuits like multipliers, MAC, filters etc. This article presents a review of the work done in different full adder circuits designed using different number of transistors and technologies by various researchers.

2.RELATED WORK

Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat proposed a low power hybrid 1-bit full adder[1]. The simulation was carried out using Cadence Virtuoso tools with 180/90nm technology. The average power, delay, PDP of proposed full adder were compared with other standard design approaches like complementary pass transistor logic, transmission gate adder, transmission function adder and other designs. The improved PDP was offered by the proposed 1-bit adder.

Yi WEI, Ji-zhong SHEN[2] proposed a novel 1-bit full adder cell using 8T. In order to reduce the power consumption and minimize the transistor count, one inverter and three multiplexers are used. The PDP, power dissipation and propagation delay of proposed 8T adder were compared with other adder designs using HSPICE simulations. They concluded that the proposed 8T adder has lower PDP and lower power consumption.

Mariano Aguirre-Hernandez and Monico Linares-Aranda[3] designed two full adders which consumes low power, high speed and reduced PDP with an alternative logic structures and pass transistor logic styles. They compared proposed full adders with other full adders. Proposed full adders exhibited an average PDP advantage of 80% with only 40% of relative area. All the full adder circuits were designed with a 0.18µm technology and tested using a comprehensive testbench.

D.V.Morozov and M.M.Pilipko[4] implemented a single bit CMOS adder with enhanced performance. This adder design consists of separate circuits which operates in parallel for obtaining the Sum and Carry signals. The circuit for the 'Sum' signal is a sequential connection of two XOR gates. The design is simulated using Cadence software with 0.18µm CMOS technology at the supply voltage of 1.8V. Because of the in-parallel operation of Sum and Carry, a decrease in the delay times and decrease in the number of transistors were achieved.

Yingtao jiang, Abdulkarim Al-Sheraidah, Yuke wang, Edwin Sha and Jin-Gyun Chung presented a novel low power multiplexer based 1-bit full adder constructed using 6 identical multiplexers and a total of 12 transistors[5]. Simulations were carried out using HSPICE to evaluate MBA-12T and five other adders including SERF, 10T adders and 28T adder. MBA- 12T adder consumes 23% less power than the 28T adder. MBA-12T adder was 64% speedier than the fastest of all other designs.

Deepak Garg, Mayank Kumar Rai,[6] proposed the implementation of full adder 3T XOR and 2-to-1 multiplexer modules were used and with total 8Transistors. Proposed full adder was compared against 10T full adder, 12T full adder, 16T full adder, 28T full adder. Here results are simulated through TANNER-EDA with 2.3 supply voltage based on 0.18um CMOS technology. Authors said that, compared to other full adders 8T adder successfully embeds the buffering circuit. 3T XOR based full adder gives high

speed, low voltage, and that lead to less energy consumption. As the transistor count is less it consumes less chip area, less cost of manufacturing, that was done via designing and simulating the layout.

The work carried out by **Deepali Sandhu, Sudhir Singh, Satwinder Singh**[7] presented the comparison of low voltage, high speed full adder circuits. Here hybrid design full adder approach combined in a single unit, and adder is designed using XOR-XNOR. Authors also discussed the conventional full adder combined with MOSCAP is called hybrid design. This technique helps to reduce propagation delay, power consumption, and area of the chip design. Simulation results in terms of delay, power, power delay product (PDP) are compared against conventional CMOS, TG, and hybrid adder circuits.

Shipra Mishra, Shelendra Singh Tomar, Shyam Akashe, in "Design low power 10T full adder using process and circuit techniques" [8] analyzed 10T full adder for minimizing the leakage current, leakage power and boost up the speed. This analysis carried out in different process and circuit techniques. To minimize the leakage power, minimum transistors were used, and made variation in transistor dimension for reducing leakage current. These simulations carried out through Cadence environment virtuoso tool with a 0.45µm technology and for different supply voltages. This also expresses that, design lines need to select suitable to required design features. On implementing on deep sub micron method CMOS leakage current reduced at the process level. Most of the power consumption decreased at the circuit level by constructing designs using less number of MOSFETs.

The authors, **Saradindu Panda, A. Banerjee, B. Maji, Dr. A. K. Mukhopadhyay**,[9] proposed the evolution of full adder to achieve high performed full adder in all important parameters. Starting from conventional 28T CMOS full adder, 20T transmission gate full adder, 14T full adder, 10T static energy recovery full adder, 10T realized using GDI (gate diffusion input), 9TA, and 9T B full adder, at last 8T full adder. All the adders have advantages and disadvantages with their respect. GDI based adder performed better but fabrication of MOSFET are cost effective, fabrication process is twin well CMOS SOI (silicon on chip). TG (transmission gate) based adders showed low average delay, but 14T full adder had low power delay product. Authors concluded that, 8T full adder is the best option for optimization of power and delay.

Saravanan R, Kalaiyarasi M, S. Jim Hawkinson, D Sathya, [10] presented that in order to achieve high speed, low power dissipation, and power delay product various techniques can be used, such as hybrid CMOS logic style to decrease PDP, Gate diffusion input (GDI) logic styles, and alternative internal logic styles. Authors also presented full voltage swing along with high speed, low power dissipation. There was an evolution in full adder parameters by conducting different experiments from different designs. Initial design was the hybrid logic style, later constructed by utilizing GDI based full adder, and GDI technique also eradicated from construction of full adder with XOR/XNOR. This approach provided the high speed, very low power, and voltage swing. This work was compared with the other full adder in 1-bit, 2-bit, 4-bit, 8-bit and 16-bit structures and this technique was better. All designs were simulated in 180nm technology on Mentor Graphics tool and results are analyzed in test bench forms.

Karthik Reddy. G [11] said that in integrated circuits power consumption and leakage power is the major concern. By lowering the power consumption of full adder, power consumption of ALU would be reduced which in turn reduces the power consumption of processors. Here the author proposed that designing low power and less transistor count full adder on cadence tool and virtuoso platform with 180nm n-well CMOS technology with supply voltage of 1.8V and frequency of 100MHz. Newly designed 6T full adder saved 93.1% of power compared to 28T adder, SERF by 80.2%. It also highly performed than pass transistor and GDI techniques.

Table -1: Survey of Different Full Adder Designs

Sl. No	Title of the Paper	Publisher & Year	Authors	Language or Tool used	Conclusion
1	Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit	IEEE 2015	Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat	Cadence with 180/90nm technology	Improved PDP was offered by proposed 1-bit full adder
2	Design of a low power 8-transistor 1-bit full adder cell	Journal of Zhejiang University -SCIENCE C 2011	Yi WEI,Ji-zhong SHEN	HSPICE	Proposed 8T adder has lower power consumption
3	CMOS Full-Adders for Energy-Efficient	IEEE 2011	Mariano Aguirre-Hernandez, Monico	HSPICE & Nanosim	Proposed full adder exhibited PDP advantage of 80% with

	Arithmetic Applications		Linares-Aranda	simulaion	only 40% of relative area
4	A Circuit Implementa-tion of a Single-bit CMOS Adder	Russian Microelect ronics 2013	D.V.Morozov, M.M.Pilipko	Cadence with 0.180µm technology	A decrease in delay times & number of transistors were achieved
5	A Novel Multiplexer – Based Low-Power Full Adder	IEEE 2004	Yingtao jiang, Abdulkarim Al-Sheraidah, Yuke wang, Edwin Sha, Jin-Gyun Chung	HSPICE	MBA-12T adder consumes 23% less power than the 28T adder and 64% speedier than the fastest of all other designs
6	CMOS Based 1-Bit Full Adder Cell for Low-Power Delay Product	IJECCT 2012	Deepak Garg, Mayank Kumar Rai	Tanner EDA with 0.18µm technology	Proposed circuit has the lowest PDP with a significant improvement in silicon area & delay
7	Analysis of CMOS Full Adder Circuits for Low Voltage VLSI Design	IJCSCE 2013	Deepali Sandhu, Sudhir Singh, Satwinder Singh	--	Designed adder circuits exhibits less delay, power consumption, PDP against conventional CMOS, TG & hybrid adder cells
8	Design Low Power 10T Full adder Using Process and Circuit Techniques	IEEE 2012	Shipra Mishra, Shelenra Singh Tomar, Syam Akashe	Cadence with 0.45µm technology	Proposed 10T full adder consumes low power
9	Power and Delay Comparison in between Different types of Full Adder Circuits	IJAREEIE 2012	Saradindu Panda, A.Banerjee B.Maji, Dr.A.K. Mukhopadhyay	--	Average power is low for GDI full adder. Average delay is low for TG based full adder. PDP is low for 14T full adder. 8T full adder is best option for optimization of power & delay
10	Evaluation of Power Delay Product for Low Power Full Adder Circuits based on GDI Logic Cell using Mentor Graphics	IJETAE 2014	Saravanan R, Kalaiyarasi M, S. Jim Hawkinson, D Sathya	Mentor Graphics with 180nm technology	Proposed designs demonstrate less power, delay & PDP compared to standard designs
11	Low power-area designs of 1bit full adder in cadence virtuoso Platform	IJVLSI 2013	Karthik Reddy G	Cadence with 180nm technology	Proposed 6T full adder saved 93.1% power compared to 28T adder and saved 80.2% power compared to SERF design

3. CONCLUSIONS

Adders are the very important structures in all most every VLSI designs. So the performance of adder decides the performance of VLSI designs. From the comparison among the adders, the performance parameters such as power, delay, power delay product for various full adder designs are different. The choice of full adder circuit can be made depending on the requirement using suitable technology.

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