

VHDL Implementation of High Speed and Low Power BIST Based Vedic Multiplier

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Abstract - In modern electronics world applications of integrated circuits are increasing day-to-day. All hardware segments which are produced are focusing on High speed, Low power and User agreeable application. Among these video and audio based processing applications are increasing. Multipliers are the essential consistent operational unit in any of the procedure. So we have outlined a high-speed multiplier utilizing our Indian customary multiplier called Vedic multiplier. Another vital equipment in testing modules is capacity to test the module independent from anyone else. The Built-in-self-test (BIST) feature encourages the user to verify the functionality and authenticate the module is defective or working fine. This paper presents a BIST based implementation of high-speed Vedic multiplier. The proposed design is realized by using Xilinx Tool using VHDL programming language. A low power Test Pattern Generator (TPG) used in design realization.

Key Words: built-in-self-test, Pseudo Random Number Generator, Very Large Scale Integrated circuits, Very High Speed Integrated Circuit, Vedic Multiplier, Xilinx, VHDL.

1. INTRODUCTION

Nowadays, the performance of the hardware design can be evaluated using its operational speed and power consumed by the hardware. Field Programmable Gate Array (FPGA) is desired and promising high speed and low power consumption hardware. In FPGA the operation is based on the switching of the internal recourse architecture. For a development of the design, this FPGA can be used and verify the operation of the circuit architecture. If there are any modifications to be done, then we can change the circuit design and again we can verify. Low power system offers benefits like long battery life, high performance, etc.

For modern digital applications, high-speed processor with low power consumption design is required. The most common and important module used in the digital signal processors is a multiplier. The multiplier is used to process the complex data. The self-testing feature is another feature that is required for testing or diagnosis of the different multiplier architecture. This feature helps the configurable integrated circuits to test by itself. In the self-test operation, the hardware is tested by applying different inputs for the functionality of the module. A simple block diagram of BIST is shown in Fig:1. Here a Logic BIST Controller is designed for controlling of the user data and

the TPG data and depending upon the control function selected by the user the mux is switched and the data is given to the Circuit Under Test (CUT). The output of the CUT is given to a response analyzer and the output of Logic BIST Controller is also given to the analysis the circuit which is developed.

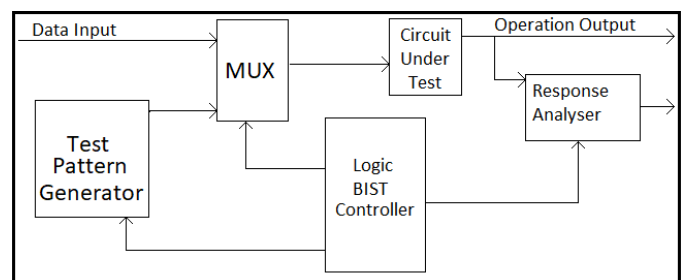


Fig -1: Simple Block Diagram of BIST Design

Numerous design adjustments are proposed by researchers and scientists are working with respect to low power BIST based rationale circuits for some applications. In this paper Low power test pattern generator designed by using Low-power Linear Feedback Shift Register. By utilizing this outline approach we have diminished the exchanging action in view of single input change design produced by a counter and a gray code converter. This design has the characteristics of high speed, low power consumption. A Low power Linear input move enlist based low power test design generator configuration is proposed. This paper mainly focuses on the BIST and how to reduce the power consumption. In this transition is reduced by generating the gray code with 1-bit distance.

A review on Vedic Mathematics for a digital signal processing operation is present. This paper deals with the review of literature based Vedic Mathematics. A FPGA based 4-bit Vedic multiplier using LFSR is present. This document describes the implementation of the 4-bit Vedic multiplier enhances with the propagation delay. TPG is the major component of the BIST hardware design. Many BIST based applications are proposed and simulated by researches to propose power and speed optimization designs based on FPGA implementation. FPGA implementation of BIST enables UART for real time interface application. This design enables self-test of a common hardware interface.

Today's requirement is low power circuit implementation of BIST Based logic circuits on FPGA to achieve high-speed operational circuits. The Test pattern is designed using a modified architecture by reducing the number of sequential circuits.

2. TEST PATTERN GENERATOR AND VEDIC MULTIPLIER DESIGN

2.1 Test Pattern Generator

The present work gives the BIST based approach for the implementation of a Vedic multiplier using configurable hardware. A low power 4-bit Vedic multiplier is used to test logic design in the proposed work. The multiplier design is implemented using the gate level architecture representation for realizing the low-power hardware. The RTL schematic of the Vedic multiplier is shown in Fig 2. A gate level combination is used to generate a half-adder and full adder. These designs are used in combination to generate the multiplier using the adder terms.

For BIST implantation, a test design generator with arbitrary test vectors are required. For TPG design, a Low-power modified design of linear-feedback-shift-register(LFSR) is used. A 3-bit register is used to generate 4-bit random test vectors. It is a comparatively low power design realization as compared to other existing designs. Most of the TPG has a register-to-bit ratio of 3:4.

The present design, TPG generates a repetitive sequence of Six random numbers of 4-bit in sequences shown in Fig 3. The logic block diagram of the test vectors generated is shown in Fig 4.

Three flip-flops are used with linear feed-back. The yield of the last flip-flop is XOR-ed with the controlled contribution of the enable pin. The output of the block is given as input to the first flip flop. The output of the first flip flop is XOR-ed with the second flip-flop to generate the first output bit. Thus if Enable input is low then the output of the TPG will drive to logic "0000". An active high signal will enable the hardware to generate a random 4-bit signal. This circuit generates a 4-bit random values using three registers, so relative low power consumption is used by this circuit. RTL schematic of Test Pattern Generator is shown in Fig 5.

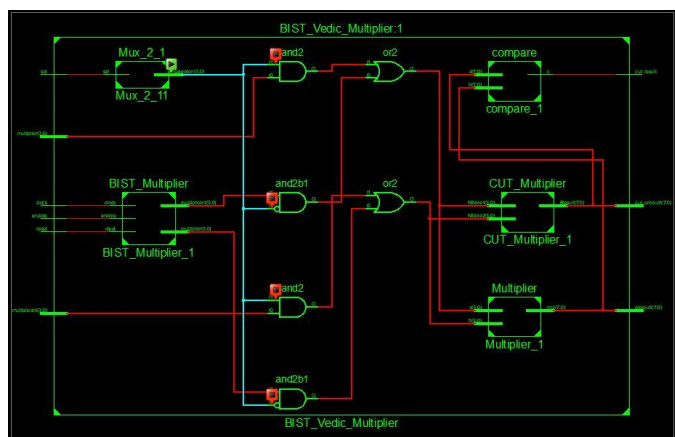


Fig -2: RTL Schematic of Proposed Vedic Multiplier

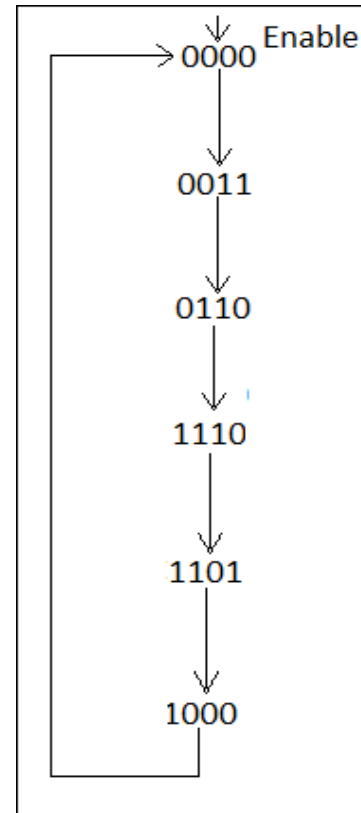


Fig -3: Flow Diagram of Test Vectors Generated by TPG

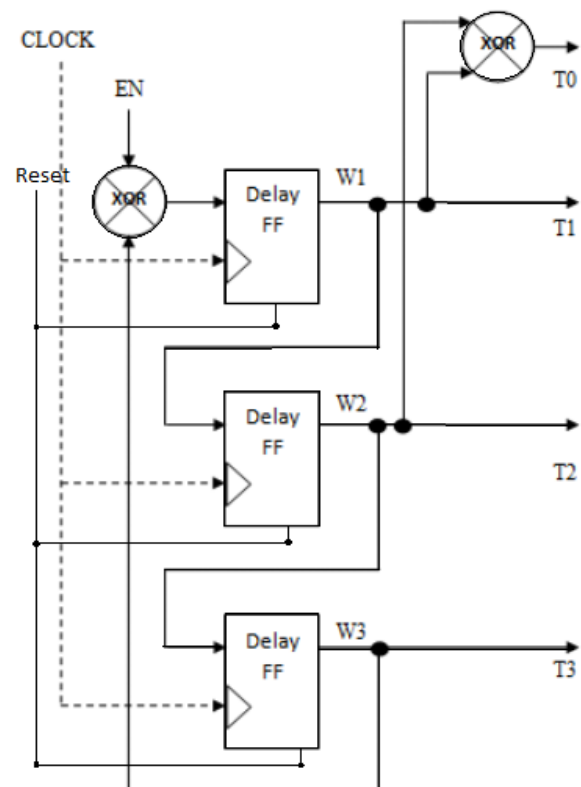


Fig -4: Logic Diagram of Test Vector Generator Used in Proposed project

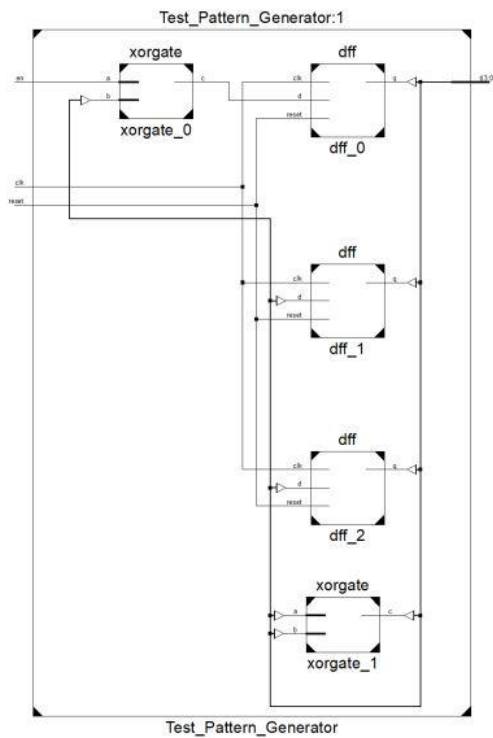


Fig -5: RTL Schematic of 4-bit Test Pattern Generator

2.2 Vedic Multiplier

In this paper, the Vedic multiplier is designed by using the 2-bit gate level Vedic multiplier. The 2-bit gate level Vedic multiplier proposed in this project is shown in Fig. 6. By combining the four 2-bit Vedic multipliers, we have designed 4-bit Vedic multiplier. Normal 4-bit parallel adder's are used to add the partial products of 4 2-bit Vedic multiplier. The proposed 4-bit Vedic multiplier is shown in the Fig. 7.

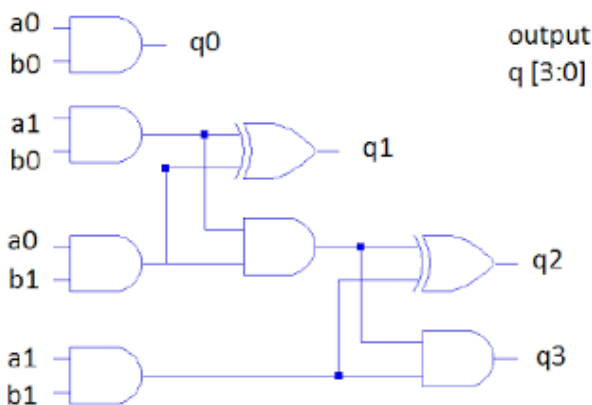


Fig -6: Gate level Logic of 2-bit Vedic Multiplier

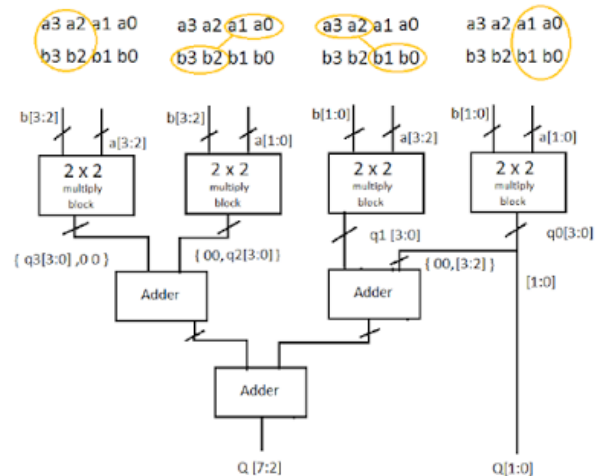


Fig -7: Proposed architecture of 4-bit Vedic Multiplier

3. PROPOSE BLOCK DIAGRAM

In this paper, we have given flexibility to the use to select the data line weather from the user or from the TPG. Depending on the selection line the module will take the respective input and will be given to the both the modules of CUT multiplier and Vedic Multiplier which we have proposed then the output of the two modules are given to compare/verify block to check the output are similar or not and then depending upon the output of the two multiplier the output will be driven to logic high or logic Low.

If the output of the module is Logic High then CUT will be pass else there is defect in the CUT. The proposed block diagram of this project is shown in the Fig 8.

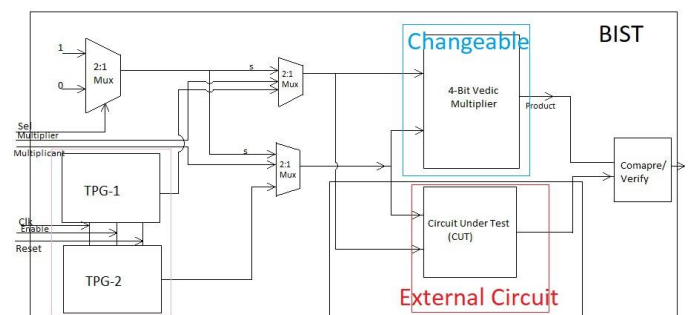


Fig -8: Proposed block diagram of the High speed and Low power BIST Based Vedic Multiplier

3. SIMULATION AND SYNTHESIS RESULT

The BIST based Vedic Multiplier design, proposed work is implemented using VHDL Hardware Descriptive Language on Xilinx ISE Tool. The RTL block diagram of the proposed design is shown in the Fig. 9. The complete simulation is performed on Xilinx ISim Tool using VHDL. The waveform simulation result of BIST-Vedic Multiplier and Vedic multiplier design are shown in Fig 10 and Fig 11 respectively.

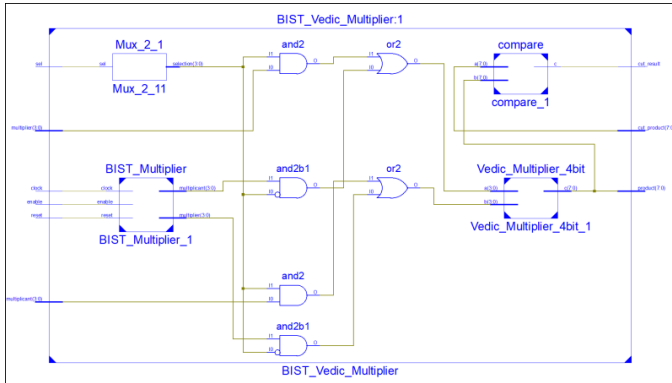


Fig -9: RTL Block Diagram of Proposed Design

The power consumption is performed on different FPGAs with different internal and auxiliary voltages. Xilinx FPGA devices from Kintex-7, Vertex-6, and Spartan-6 family devices are used for analyzing dynamic power consumption. The dynamic power consumption is presented in Table 1. The power-frequency analysis of the proposed work is performed using Xilinx XPower Tool.

The time constraints(Delay) is performed on different FPGAs with different internal and auxiliary voltages. Xilinx FPGA devices from Kintex-7, Vertex-6, and Spartan-6 family devices are used. The time constraints are presented in Table 2.

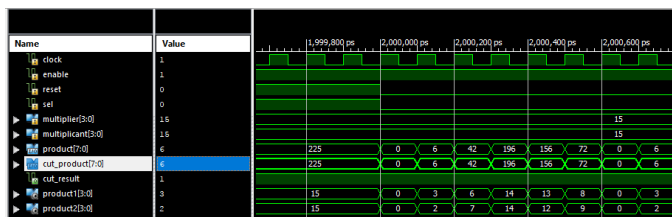


Fig -10: Waveform Simulation for Proposed BIST Based Vedic Multiplier

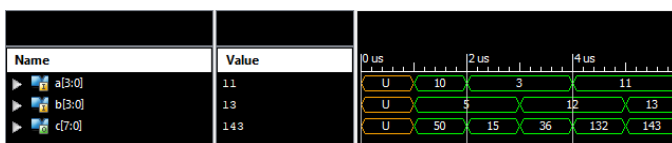


Fig -8: Waveform Simulation for Proposed Vedic Multiplier

Table-1: Dynamic Power Consumption of Proposed Design

Device	Voltage		Dynamic Power(w)	Total Power(w)
	VCCint	VCCaux		
XC6SLX150-2FGG900	1.2	2.5	0.1	0.113
XC6VCX75T-FF484	1.0	2.5	0.6	1.293
XC7K70T-2LFBG676	1.0	1.8	0.04	0.045

Table-2: Time Constraints in Proposed Design

Device	Maximum Frequency(MHz)	Combinational Path Delay(ns)	Total Path Delay(ns)
XC6SLX150-2FGG900	567.215	14.897	15.65
XC6VCX75T-FF484	1300.136	5.417	5.622
XC7K70T-2LFBG676	1507.954	4.906	5.064

5. CONCLUSIONS

In this present work the logic design which is used in the built-in-self-test application is a 4-bit Vedic multiplier and the test pattern generator is also designed for generating random 4-bit vector. Here the test pattern generator has modified to low register-to-bit ratio, i.e the number of bits sequence generated is more than the number of registers. Thus, the proposed model is very convenient for the users to select the data externally or to generate the data internally to cover all the bits from 0000 to 1111. This work simulation and synthesis clearly indicates that low power is required and high speed performance to develop this application. In future we can use a high speed multiplier rather than Vedic multiplier and also increase the bit sequence by multiple series combination of similar architecture of logic circuit for a long bit sequence generation of random number.

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BIOGRAPHIES



I am Manohar Mohanta M.Tech(VLSI System Design) student in Malla Reddy College of Engineering and Technology. My main concentration is on DSP Domain to reduce the time delay and power consumption of any module. I am passionate to learn and implement the algorithms in VLSI Domain.