International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 09 | Sep -2017 www.irjet.net p-ISSN: 2395-0072

VLSI Architecture for Cyclostationary Feature Detection Based Spectrum Sensing for Cognitive-Radio Wireless Networks and Its ASIC Implementation

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Abstract-*Cyclostationary feature detection for spectrum sensing in cognitive radio network has significant prospect in future wireless-communication systems. This work deals with the very-large scale-integration (VLSI) architectural transformation of such detection al-gorithm for field-programmable gate-array (FPGA) prototyping and application-specific integrated-circuit (ASIC) design. System level design of this detection algorithm and the architectures of all its internal blocks has been proposed in this paper. Subsequently, performance analysis of the suggested detector in additive-white Gaussian-noise (AWGN) envi-ronment has been carried out where it could deliver 0.95 probability of detection at -6 dB. Similarly, performance comparison of the implemented and simulated detector showed that there is a absolute error of only 0.07. Eventually, the proposed system-level architecture is synthesized and post-layout simulated using 90 nm complementary metal-oxide semiconductor (CMOS) technology node. It occupies 23.13 mm^2 of core area with 3663K gate-equivalents and consumes total power of 6.5 W at 100 MHz clock frequency.*

Keywords*-VLSI, Digital ASIC Design, FPGA, cognitive radio, de-tection probability, spectrum sensing and orthogonal-frequency division-multiplexing (OFDM).*

1.INTRODUCTION

Wireless communication has expanded its horizon in almost every aspect of human lives and its consequence is rapid surge in the demand of spectral resource. Transceivers for such system con ventionally operates in pre-allocated spectrum band. However, the contemporary spectrum-allocation policy indicates the shortage of unallocated spectrum band; albeit, measurements shows that the allocated bands are under utilized. Cognitive radio is an innovative technology to circumvent the scarcity of spectrum bands and utilize them to the fullest . It has the intelligence to understand the surrounding wireless-communication environment and allow the users of cognitive radio network (secondary users) to access the unutilized portions of the spectrum without disturbing the operations of the authorized user of that band (primary user). For example: various wireless applications utilize the 2.4 GHz free industrial scientific and medical (ISM) band. However, this band is overcrowded because majority of applications like Bluetooth, WiFi, ZigBee etc. utilizes it and, therefore, it is difficult to provide high quality of service in such band. As mentioned earlier, developers are not allowed to operate in other allocated bands and are reserved by the government. Due to such rigid allocation of the spectrum, some frequency bands are over utilized (like ISM bands) and some are severely under utilized (like analog TV bands).

In the cognitive radio network, transceiver associated with each of the secondary users must possess a capability to sense the radio spectrum and detect the presence of primary user . If the channel is free then secondary user can access the channel otherwise it has to keep sensing the spectrum until it finds free channel which is not under the use of any primary user. Thereby, several spectrum sensing algorithms have been reported viz. energy detection, matched filter and cyclostationary based methods . Energy detection is popular spectrum sensing technique which is carried out based on the energy sensed . The advantageous side of this technique is its simplicity and ease of hardware implementation.

However, it delivers poor performance under low signal-to-noise ratios (SNRs) and is not suitable for detecting the spread spectrum signals. On the other hand, match filter based detection requires exact knowledge of target user, consumes more power and has highly complex architecture Finally, the cyclostationary based spectrum sensing provides adequate performance even at lower SNRs and possess good signal classification capability . Thereby, this technique is suitable for the wireless communication system where secondary users need to sense the spectrum under very low values of SNRs and the quality of sensing is of primary concern.

From the implementation perspective, cognitive radio device based on cyclostationary detection possess challenge at all level of abstractions like antenna, analog-RF and digital-baseband designs. Con-temporary wireless devices demands miniaturization in the size where all the functional blocks are embedded on a single system on chip (SoC) . ASIC design of cyclostationary detection algorithm is absolute necessary in the future cognitive-radio network for wireless communication applications. However to the best of our knowledge, there are no reported works where the ASIC design aspects of such detection algorithm has been carried

out. Therefore, this work aims to bridge this gap in the research paradigm of cognitive radio from VLSI implementation aspect. Brief descriptions of paper contributions are as follows:

System level design of the cyclostationary based spectrum detection algorithm for OFDM signals has been presented.

Detailed VLSI architectures of autocorrelation module, pipelined fast Fourier transform (FFT) unit, multiply-&-accumulate (MAC) block, frequency selector and test statistics computing unit are proposed. Subsequently, the integration of these sub-blocks to realize cyclostationary detector has been discussed.

Performance analysis of detection algorithm where probability of detection versus SNRs has been plotted in AWGN channel environment. Consecutively, the proposed architecture is hard-ware implemented in FPGA platform and its functionality as well as performance are verified with respect to conventional ones.

Eventually, the verified architecture of cyclostationary detector is ASIC synthesized, placed, routed and post-layout simulated in 90 nm CMOS technology node.
Organization of this paper is as follows. Section II presents mathe-matical prerequisite of cyclostationary spectrum sensing for OFDM signals. System level description of the detector for spectrum sens-ing and its detail VLSI architectures are illustrated in section III.

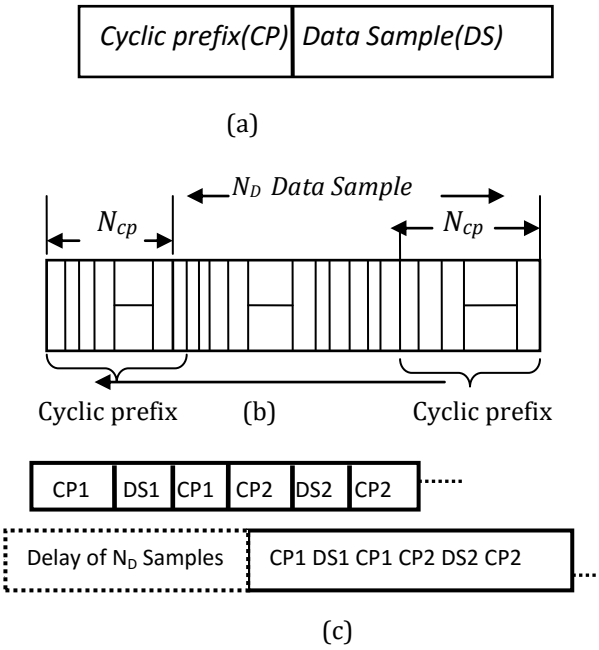

Figure 1. Schematic representations of (a) typical OFDM symbol (b) OFDM symbols with segregated samples, and (c) illustration for the periodicity in cyclic prefix of OFDM symbols.

Subsequently, section IV includes information regarding performance analysis, FPGA implementation and ASIC design synthesis as well as post-layout simulation for the proposed architecture. Finally, this paper concludes in section V.

II. PRINCIPLE OF CYCLOSTATIONARY SPECTRUM SENSING

A signal $x(n)$ is said to be cyclostationary if its time varying expectation of auto correlation

$$E[x(n)\, X\, x^*(n-r)] \quad (1)$$

is periodic and there exists Fourier series expansion for such periodic signal. This is termed as cyclic property of the autocorrelation signal that has been exploited in this work and the frequency domain tests are carried out for the detection purpose.As mentioned earlier, we have considered OFDM based communication system and, there by, it is essential to understand the auto correlation of OFDM symbol. Fig. 1(a) shows a typical structure of such OFDM symbol. It incorporates collection of orthogonal subcarriers modulated using quadrature amplitude modulation (QAM) or phase shift keying (PSK) modulation appended with cyclic prefix. Such cyclic prefix is a portion of the modulated signal (last N_{cp} samples) which is appended in the beginning to complete the OFDM symbol, as shown in Fig. 1(b). Thereby, such cyclic prefix of OFDM symbol results periodicity in the expectation of autocorrelation signal. Subsequently, if the lag factor τ equals N_D(as indicated in Fig. 1(c)) then the autocorrelation at this lag should be periodic. Such autocorrelation is periodic for some delay τ and therefore, the Fourier series

$$\hat{R}(\tau,\alpha) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)\times x^*(n-\tau)\times \exp\left(\frac{-j2\pi\alpha n}{N}\right) \quad (2)$$

where α is the frequency of autocorrelation signal which is also referred as cyclic frequency and N is the total number of input samples. In order to compute this equation for $\hat{R}(\tau,\alpha)$, it is possible to use discrete Fourier transform (DFT) operation and, moreover, it can be efficiently calculated using N-point FFT algorithm. As we know that the equation for DFT is represented as

$$F(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)\times x^*(n-\tau)\times \exp\left(\frac{-j2\pi kn}{N}\right) \quad (3)$$

$$\forall\ k = \{0,1,2,\cdots,N-1\}.$$

The frequency component corresponding to the cyclic frequency α, which plays significant role for detection process, can be computed as $F(\alpha) = X_\alpha + j\cdot Y_\alpha$. (4)
Therefore, if the autocorrelation is periodic having frequency α then $F(\alpha)$ value at the out of FFT process will have a nonzero value. Eventually to test the presence of primary user, it is necessary to compute the test statistics as [5]

$$\hat{r} = [\Re\{F(\alpha)\} \quad \Im\{F(\alpha)\}] \tag{5}$$

where real and imaginary parts of the autocorrelation signal are arranged as a vector $\hat{r}$. Thereafter, the test statistic can be obtained using the following expression:

$$\hat{T}_C = N \times \hat{r} \times \varphi^{-1} \times \hat{r}^T \tag{6}$$

where ψ is the covariance matrix which is expressed as

$$\varphi = \begin{bmatrix} \hat{E}[X^2(k)] & \hat{E}[X(k)Y(k)] \\ \hat{E}[X(k)Y(k)] & \hat{E}[Y^2(k)] \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}. \tag{7}$$

Each of the elements in φ matrix are mathematically represented as follows:

$$A = \hat{E}[X^2(k)] = \frac{1}{N}\sum_{k=0}^{N-1} X^2(k), \tag{8}$$

$$B = C = \hat{E}[X(k)Y(k)] = \frac{1}{N}\sum_{k=0}^{N-1} X(k) \times Y(k), \quad and \tag{9}$$

$$D = \hat{E}[Y^2(k)] = \frac{1}{N}\sum_{k=0}^{N-1} Y^2(k). \tag{10}$$

Eventually, the test statistic is determine as [5]

$$\hat{T}_C = \left[\frac{X^2(\alpha) \times D + Y^2(\alpha) \times A - 2 \times X(\alpha) \times Y(\alpha) \times C}{A \times C - B^2}\right]. \tag{11}$$

This test statistic $\hat{T}_C$ applies Neyman-Pearson hypothesis-testing method to test the presence of the primary signal. Such hypotheses are given as

$$H_0 : \ \hat{T} = \epsilon,$$

$$H_1 : \ \hat{T} = T + \epsilon$$

where $\hat{T}$ is the estimated value of the detection test statistic and ϵ is the contribution of noise to the test statistic. Similarly, T is the ideal value of the test statistic. In case of hypothesis H_0, there is no signal and it includes only noise contributions in the test-statistic calculation process. On the other side, there are both signal as well as noise contributions to the test statistic calculation under the hypothesis H_1. For the null hypothesis, the test statistic is χ^2 distributed and it is feasible to compute the threshold by its inverse probability distribution function as

$$\eta_C = F^{-1}_{\chi^2_2}(1 - P_{FA}) \tag{12}$$

where P_{FA} is the probability of false alarm [5]. Thereby, one can make a decision by comparing the value of computed test statistic with the threshold value and then make a decision for the presence of primary user [3].

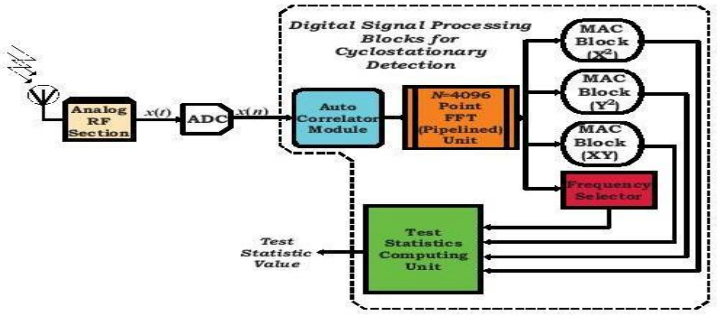

Figure 2. Block diagram of system level design for cyclostationary detection.

III. PROPOSED ARCHITECTURE FOR CYCLOSATIONARY DETECTION

A. Communication and Quantization Specifications

In order to construct an OFDM symbol, this work considers 64 subcarriers and the length of cyclic prefix is one fourth the total number of subcarriers in each symbol that translates to 16 subcarriers. Thus, the length of OFDM symbol includes 80 complex numbers where each of them corresponds to a subcarrier that is quadrature phase-shift keying (QPSK) modulated. Subsequently for reliable detection, it is necessary to assume 50 such OFDM symbols and this results into total number of 4000 samples. Thereby, this imposes on the requirement of at least N = 4096 point FFT for computing the test statistics. In this paper, each of complex number has been quantized with 64 bits where the most-significant 32 bits are reserved for the real portion and the rest 32 bits represents the imaginary part of this complex number. Additionally, each 32 bit number (for real or imaginary part of the complex number) has been further segregated as Q15.16 fixed point. It implies that the most significant bit (MSB) is dedicated for the sign of number, subsequent 14 bits is allocated for the magnitude of the whole number prior to decimal point and the rest 16 bits quantize fractional precision of the number. Our work considers two's complement number representation and arithmetic computation throughout the system-level design for all the operations. Finally, this work assumes the probability of false alarm (P_{FA}) to be 0.1 for the threshold computation.

B. System Level Description

Block diagram representation of the complete system for cyclostationary detection is shown in Fig. 2. It comprises of antenna that provides radio frequency (RF) signals to analog RF section which band-pass filters, for a bandwidth of 4 MHz in this work, and low noise amplifies as well as down converts such RF signal into baseband signal $x(t)$ for further processing. Subsequently, this signal is sampled by analog to digital converter (ADC) to deliver series of samples $x(n)$. Fig. 2 shows that ADC outputs quantized samples and are fed as input to the auto correlator module where the lag factor τ

for autocorrelation operation is 64 samples delay in this work and this value can be reconfigured if required. Thereafter in consecutive clock cycles, the output from the autocorrelator module is fed to the FFT module and when sufficient number of samples

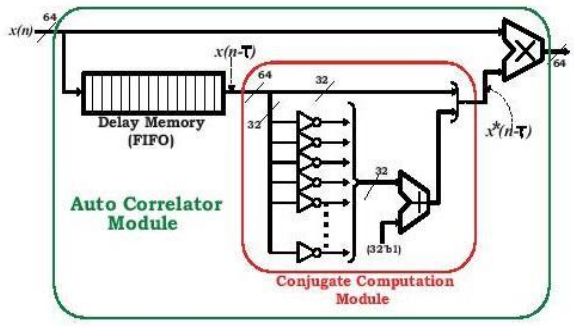

Figure 3. Suggested architecture for the module that computes auto correlation of complex input samples from ADC.

Arrive at the input of subsequent FFT unit then this module starts performing the DFT operation. Thereby, the output is delivered in every consecutive clock-cycle from this unit and are fed to three multiply and accumulate (MAC) modules which starts computation until next 4096 clock cycles. Simultaneously, the frequency selector module is activated which snoops on the output of the FFT module and latches its output corresponding to the cyclic frequency α. The outputs from MAC modules are fed to the test statistic computing unit which calculates the magnitude of test statistic. Thereafter, the output from this unit is compared with the predefined threshold, which is reconfigurable and stored in a register, to make final decision for the presence of primary user. In this work, each of these blocks in Fig. 2 are activated only for the period for which they are operating data, otherwise the modules which are not in use are disabled with the aid of clock gating technique. Additionally, the internal stages of every block are pipelined to make this architecture high-speed and low power.

C. Auto-Correlator Module & Pipelined-FFT Unit Architectures

The suggested digital architecture of auto correlator module is shown in Fig. 3. As discussed earlier in system model, this moduleaccepts 64 bit complex input $x(n)$ which is first stored in a delay memory and eventually multiplies current input sample with the conjugate of delayed version of such input. The delay memory mentioned here is indeed realized using first-in first-out (FIFO) which outputs the value of $x(n-\tau)$, as shown in 3. Consecutively, conjugate operation has been performed by calculating the two's complement of the least significant 32 bit of the 64 bit delayed input $x(n-\tau)$ and this will negate its imaginary part. Thereafter, such two's complemented 32 bit are concatenated with 32 bit of the real part to generate the conjugate value $x^*(n-\tau)$. Eventually, Fig. 3 shows that the current input is multiplied with the obtained conjugate value to determine the autocorrelation of input $x(n)$.

This work incorporates N = 4096 point (4K point) decimation-infrequency radix-4 FFT unit for the cyclostationary detection process and its suggested architecture has been shown in Fig. 4. In order to process 4096 point FFT, this architecture has been segregated into six identical radix-4 FFT stages. Additionally, the suggested FFT architecture has been pipelined in such a way that each pipeline-stage includes one stage of radix-4 FFT module, as shown in the Fig. 4. As the 64 bit auto correlated inputs are fed to this architecture, only the first stage of the FFT is initially active and it sequentially stores these data into the memory modules until it receives sufficient number of samples to start computing first output. Immediately after it receives the required number of inputs, the sequencer module is activated and

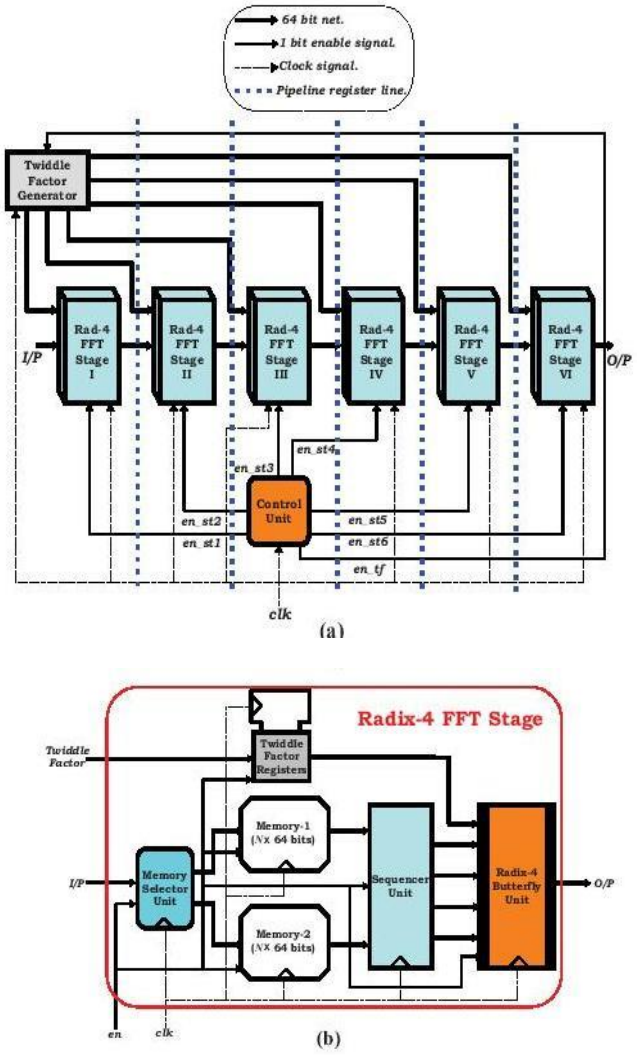

Figure 4. (a) Proposed architecture of N = 4096-point radix-4 FFT used in the suggested cyclostationary-detector design. (b) Internal architecture of radix-4 FFT stage.

then feeds the input to radix-4 FFT butterfly, as shown in Fig. 4. Subsequently, the next FFT stage is activated and it generates single output in each clock cycle. Within a radix-4 FFT stage, as soon as the first memory is full then the memory selector module enables another memory and starts storing the input samples in it. On the other hand, if there are no input samples to a previous stage then this memory is disabled and thereby powering up the FFT stages only when they are functional. It is to be noted that the output of FFT is in bit reversed order. Thereby, it is not necessary to rearrange the FFT output, as the sequence of the data is of less concern for further processing of consecutive blocks in the architecture.

D. Suggested architectures of MAC, Frequency Selector and Test- Statistic Calculator Modules

Fig. 5(a) shows the architecture of MAC module which accepts two 32-bit real-number inputs in Q15.16 fixed point format. When this module is activated in every clock cycle, it multiplies two 32 bit inputs and adds this product with the previous value that is fetch from the accumulator and then stores back the result in accumulator. Additionally the *reset* signal has been incorporated to clear the accumulator contents. Similarly, if the enable signal input is held low then the multiply operation is not performed, nevertheless, the value of accumulator is latched on the output pins of MAC module. On the other hand, Fig. 5(b) shows the architecture of the frequency selector module used in this work. This module has been designed to snoop the output of FFT unit until the frequency component for α (cyclic frequency) appears. Immediately after the frequency component of α appears at the input, it latches the 64-bit complex value on its output pins. It can be implemented using simple counter circuit which counts up to the desired value and then latches the input value to the output where there is a counter overflow.

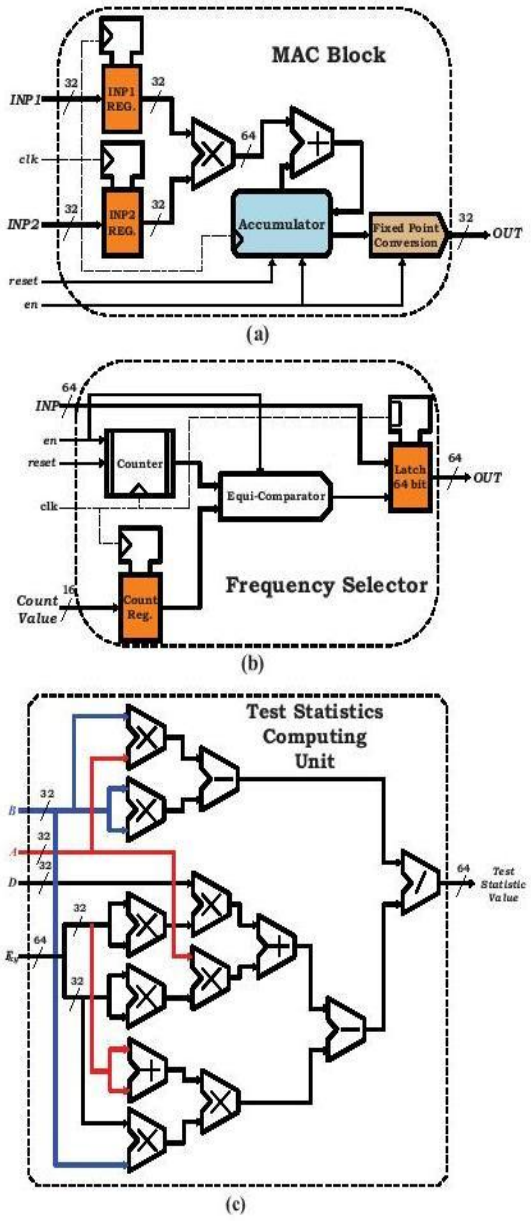

Figure 5. Suggested VLSI architectures of (a) MAC block (b) frequency selector and (c) test statistics computing unit of the cyclostationary detector.

statistic value from (11) has been presented in Fig. 5(c) and it is referred as test-statistics computing unit in this paper. It is fed with four 64 bit inputs from three MAC modules and a frequency selector module, as shown in 2. The outputs from MAC Blocks (X^2), (Y^2) and (XY) are represented as *A*, *D* and *B* respectively. Similarly, frequency selector output is denoted as F_{xy}, as shown in Fig. 5(c). This suggested architecture comprises of eight multipliers, two adders, two subtractors and a divider for computing the test

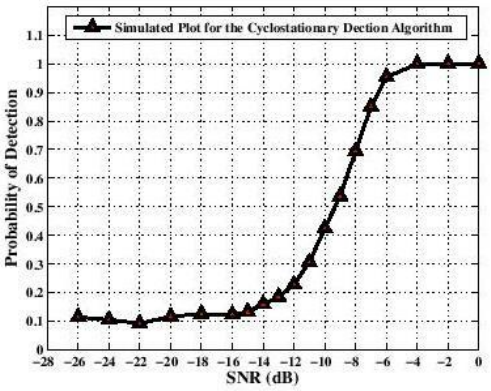

Figure 6. Simulated plot for probability of detection versus SNR for the suggested cyclostationary detection in AWGN channel environment.

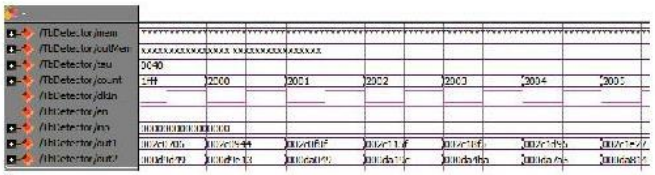

Figure 7. Post place-&-route simulated input-output waveform of the FPGA-prototyped cyclostationary detector.

statistic value $\widehat{T_C}$ from (11).

IV. PERFORMANCE ANALYSIS, FUNCTIONAL VERIFICATION AND VLSI DESIGN

In order to analyze the performance of the cyclcostationary detection algorithm, this work carried out simulation with 50 OFDM symbols which is equivalent to 4000 samples. These samples are modulated and are attenuated by passing through AWGN channel environment [8]. Thereafter, the algorithm for cyclostationary detection has been invoked to process the samples and generate the final test-statistic output. Thereafter, the comparison of this result with the predefined threshold has been carried out to make the decision whether the primary user is present or absent. During this course of simulation, detection process for 4000 samples ran for atleast 1000 times for each SNR in order to calculate reliable probability of detection. As a result, the obtained plot of probability of detection versus SNR is shown in Fig. 6. It shows that the probability of detection tends to improve at higher SNR and vice versa towards lower SNR. Specifically, the suggested detector algorithm has a probability of detection of 0.95 and 0.1 at -6 dB and -22 dB, respectively, as shown in Fig. 6.

Consecutively, this work has hardware prototyped the proposed architecture of detector on the FPGA. This design has been coded using Verilog hardware-descriptive-language (HDL), synthesized and the configuration file (in .bit format) is dumped on Virtex-V (XC5VFX200T) FPGA boards. The testbench that includes the samples of $x(n)$ are used to post place-&-route simulation of the synthesized code and its outputs are verified with the simulated results of the algorithm. Thereby, the input-output waveform obtained from the FPGA prototype is shown in Fig. 7. Additionally, the input samples (in fixed point format) are also processed by the hardware prototype of the detector and the plot of probability of detection at

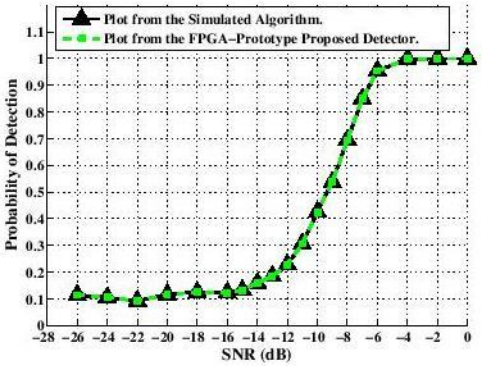

Figure 8. Comparative plots for probability of detection versus SNR for the suggested cyclostationary detection in simulation and implementation modes.

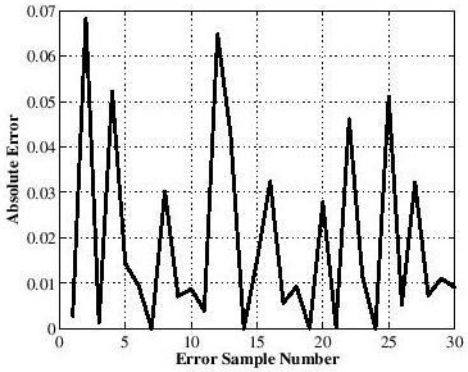

Figure 9. Comparative error plot for the suggested cyclostationary detection in simulation and implementation modes.

different SNRs is plotted, as shown in Fig. 8. It can be observed that the implementation plot is same as the simulated plot. Thus, even after the fixed point implementation of the design, we have obtained accurate magnitude of T_C values. In this paper, we have compared the number of T_C values calculated from the simulation of the detection algorithm with those values calculated from FPGA prototype and then calculated the absolute error. Such error plot has been shown Fig. 9 and it can be clearly observed that the maximum error between the simulated and implemented results is 0.07, which is within the permissible limits. The proposed architecture of cyclostationary detector has been synthesized, using standard cell libraries of UMC 90 nm-CMOS technology node, under various design constrains. The static timing analysis (STA) of the gate-level netlist that is generated from the synthesis has reported that the pipelined design can be operated with the maximum clock

frequency of 110 MHz and it consumes 3663K gate equivalents (GEs). Subsequently, the verified netlist is imported for the physical design process (backend design), using the SoC encounter tool from Cadence, along with the integrated I/O pads. Such netlist including the proposed design and I/O pads are placed, routed (power and signal routed), clock tree synthesized and, finally, STA is carried out to check the setup as well as hold violations. The chip layout of this detector architecture is shown in Fig. 10. Thereafter, the RC extraction of the this chip layout is carried out

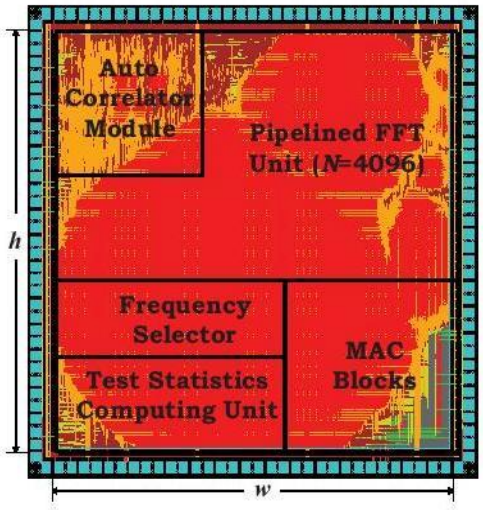

Figure 10. Generated chip layout of the proposed cyclostationary detector using 90 nm CMOS process with the core dimension ($h \times w$ = 5.12 mm × 4.50 mm).

Table I
ASIC POST-LAYOUT SIMULATED RESULTS OF THE PROPOSED CYCLOSTATIONARY DETECTOR.

Design Parameters	Values Obtained
Technology (nm)	90
Supply Voltage (V)	0.9
Core Area (mm^2)	23.13
Dynamic Power (mW) @ 100 MHz	6380.62
Leakage Power (mW) @ 100 MHz	77.87
Total Power (mW) @ 100 MHz	6458.49
Maximum Clock Frequency (MHz)	110
Gate Equivalents (GEs)	3663K

and such values are used along with the test bench to carry out postlayout simulation. Eventually, the total power consumed during the course of post-layout simulation is noted, as listed in Table I.

V. CONCLUSION

The paper presented architectural aspect of cyclostationary-feature based detection for spectrum sensing of OFDM based cognitiveradio wireless network. VLSI architectures of all the blocks those are involved in the detection process has been suggested and then integrated for FPGA implementation. Subsequently, the performance analysis indicated that the suggested decoder architecture delivered adequately even at lower SNRs: it detected the spectrum occupancy of primary user with the probability of 0.95 even at -6 dB of SNR. On the other hand, the suggested architecture was ASIC synthesized and post-layout simulated using 90 nm CMOS process. Thereby, chip layout of this design could perform with the maximum clock frequency of 110 MHz and occupied 23.13 mm2 of core area. To the best of our knowledge, this paper reported the ASIC design of such prospective concept of cyclostationary detection for the first time. Therefore, this work can pave new path in the field of cognitive radio for the future wireless-communication systems.

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