

PERFORMANCE ANALYSIS OF A LOW-POWER HIGH-SPEED HYBRID 1-BIT FULL ADDER CIRCUIT USING CMOS TECHNOLOGIES USING CADANCE

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ABSTRACT: The general objective of our work is to investigate the power and delay performances of low-voltage full adder cells in different CMOS logic styles for the predominating tree structured arithmetic circuits. A new hybrid style full adder circuit is also presented. The sum and carry generation circuits of the proposed full adder are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem. As full adders are frequently employed in a tree structured configuration for high-performance arithmetic circuits, a cascaded simulation structure is introduced to evaluate the full adders in a realistic application environment. A systematic and elegant procedure to scale the transistor for minimal power-delay product is proposed. The circuits being studied are optimized for energy efficiency at 180nm, 90nm and 45nm CMOS process technology. With the proposed simulation environment, it is shown that some survival cells in standalone operation at low voltage may fail when cascaded in a larger circuit, either due to the lack of drivability or unsatisfactory speed of operation. The proposed hybrid full adder exhibits not only the full swing logic and balanced outputs but also strong output drivability. The increase in the transistor count of its complementary CMOS output stage is compensated by its area efficient layout. Therefore, it remains one of the best contenders for designing large tree structured arithmetic circuits with reduced energy consumption while keeping the increase in area to a minimum. In this report the 1-bit proposed full adder circuit is designed and also it is also extended to 4-bits and the results of power and delay were also tabulated.

KeyWords: FA=Full Adder, HA=Half Adder

1. INTRODUCTION

There are four basic arithmetic operations. Addition is one of them. Addition of two or more numbers is broadly utilized in numerous applications of VLSI, for example in application-specific DSP architectures and microprocessors. The numbers that are added in VLSI applications are usually in the form of binary digits that is

in the form of 0's and 1's. Addition is the core of many other operations like subtraction, multiplication, division and address calculation. In VLSI field, an architecture called "Adder" is used to add two or more binary digits. Adder can be either a FA or a HA. This project concentrates on FA. Thus the main objective of this project is enhancing the performance of the available one-bit FA cell.

The requirement for low-power VLSI systems is constantly increasing because of the endless applications emerging in mobile communication and compact devices. Today's compact devices are usually battery operated for example, mobile phones, PDA's, which demands VLSI with less power consumption. So designers and developers are facing more problems regarding high performance, rapid speed, low-power consumption and narrow silicon space. Thus constructing a high performance low-power adder cells are having enormous importance. Therefore in this project, a well-organized approach for understanding the adder construction and working is given. It is focused on splitting the entire FA into several smaller modules. Every single module is constructed, optimized, and tested individually. Multiple FA cells are formed by joining these smaller modules.

FA's, being the most basic building block of all the processors, thus remains a key concentration area for the scientists over the years. Distinctive logic styles with their own pros and cons were examined to execute 1-bit FA cells.

The outlines, detailed up until this point, might be comprehensively classified into two classifications:

Static style: Power leakage is measured during the Continuous flow of Voltage.

Dynamic style: Power leakage is measured during the switching ON and OFF of a Circuit.

Static FA's are usually more stable, less complicated with low power demand even though the on-

chip area requirement is more in comparison to its dynamic counterpart.

FA's can be constructed using different logics, namely: Standard static complementary metal-oxide-semiconductor logic (CMOS), dynamic CMOS logic, complementary pass-transistor logic (CPL), and transmission gate full adder (TGA).

Whereas some adders can be constructed by implementing more than one logic style. Such architectures are called hybrid-logic designs. These hybrid logic designs makes use of advantageous features of above mentioned logic styles to enhance the general execution of the FA. Even though this hybrid logic style offers promising execution, a large portion of these designs encounter a poor driving capacity which results in the definite reduction in their execution in cascaded mode of functioning if the reasonably designed buffers are excluded.

Hybrid Full Adders are used in the battery-operated compact gadgets such as Mobile phones, PDA's, and notebooks which require VLSI, and ULSI designs with a better power delay aspects. It is used in the Processor chip like Snap dragon, Intel Pentium for CPU part, which consists of ALU. This block is used to carry out the operations like addition, subtraction, multiplication etc.

1.1 Literature Survey

In computer arithmetic the FA's can be categorized into two fundamental classes. The first class includes Ripple Carry Adders (RCA) and Array Multipliers. These architectures are constructed by arranging the full adders in chain where the output of first adder is the input to the next adder. Thus in these designs the critical path travels from carry-in of the first FA to the carry-out of the last FA. Here the generation of the carry-out signal should be quick otherwise; the late carry-out signal not only increases the delay but also create more disturbance and glitches in the succeeding stages subsequently ending up consuming more power.

The second class includes Wallace Dadda tree multipliers and multiplier-less digital filters were described in **P. J. Song et al.**[1], **A. P. Chandrakasan et al.**[2] and **C. H. Chang et al.**[3], which forms a tree like architecture. FA's in these architectures forms a tree of few layers to pack the partial products to a carry saved number before a last carry propagation adder changes over it to a typical binary number. These multiplier designs are proved to be quicker than its chain structured architectures. However, these tree structured architectures are more complicated because of their irregular structure and lengthy interconnections. Thus, this unpredictable structure makes the layout bit complicate and takes wide silicon area.

Lengthy interconnections will possibly bring down the execution in ultra deep submicron process. Thus a methodology has been presented in **C.H Chang et al.**[3], this paper is used to considerably improve the efficiency in using silicon area by making the FA's to avoid the cross-stage interconnections as much as possible, without disturbing the connectivity in individual stages. In these designs three outputs from the upper adder stage acts as the inputs to the lower adder stage in order to provide flexibility for redistributing the cells. Due to this feature, the outputs namely sum and carry-out of the FA's are obtained synchronously thus reducing the glitches in the lower stages.

N. H. E. Weste et al.[4] described that CMOS logic. The standard complementary (CMOS) style-based adder usually consists of 28 transistors. This design shows more robustness against transistor sizing voltage scaling but the design needs high input capacitance and buffers thus it prove to be its major disadvantage.

J. M. Rabacay et al.[5] describes the complementary design to the CMOS FA is the mirror adder, which consumes almost same power and consists of same number of transistors as of CMOS style but the delay in the path through which carry propagates within the adder is generally less in comparison to that of the standard CMOS FA.

D. Radhakrishnan[6] and **C.H Chang et al.**[3] were described the CPL Full Adder. CPL consists of 32 transistors with a better voltage swing. Even though it has a better voltage swing it's not a suitable choice for applications which requires low power. The major limitations of CPL are regular "ON" and "OFF" of intermediate nodes, overloading of its inputs, requirement of more number of transistors and static inverters.

R. Zimmermann et al.[7] and **A. M. Shams Et al.**[8] describes the major limitation of CPL is the voltage degradation that has been effectively over come in TGA, which requires only about 20 transistors for designing the FA. But the other limitations of CPL like, slow-speed and more power consumption are always been the major issues to be concentrated. Thus, the researchers came with a more effective approach which includes the advantageous features of various logic styles in order to improve the overall performance of the design called as the "Hybrid logic approach".

Vesterbacka et al.[9] presented an approach for implementing a FA using more than one logic style which employs 14-Transistors.

Zhang et al.[10] has proposed hybrid pass logic with static CMOS output drive FA (HPSC). This HPSC circuit uses a pass transistor logic employing only six transistors where the XNOR and XOR functions are synchronously obtained and it is made used in CMOS module so as to get full swing outputs of the FA but demands more number of transistors and also decreases the speed. In spite of the reality that the hybrid logic styles provides good performance, but most of these hybrid logic adders encounter poor driving capability issue and thus their performance gets corrupted drastically when functioning in a cascaded mode without a well designed buffers.

This paper concentrates on the tree structured architectures for examining the FA's being optimized and simulated in the presented tree structure simulation environment. Another objective is to prolong the life span of battery operated compact electronics in order to limit the energy usage per arithmetic operation. Here low power consumption does not mean low energy. To complete any arithmetic operation, a circuit can utilize very low power by clocking at exceptionally low frequency but it needs more time to complete the entire operation. One of the objectives of this project is to study the energy efficiency of the FA's designed using various logic styles with a decreasing input voltage in an 180nm technology. The main aim of this project is to enhance various specifications such as delay, power and transistor count of the FA in comparison to the already existing logic style's.

1.2 PROBLEM DEFINITION

The problem being faced is designing of a Hybrid FA using Cadence virtuoso 180-nm, 90-nm and 45-nm technology is to reduce delay, area and power of a circuit. In the literature survey it is evident that the CCMOS logic utilizes 28-Transistors, similarly in the CPL and TGA Logic uses 32T and 20T. These structures are not suitable for a suitable choice for low-power applications because of various limitations as discussed in the literature survey. The main drawbacks of these structures are voltage degradation in the output voltage levels and slow response, high power utilization and high area occupied. Therefore with the concern on power, area and speed, design and develop a hybrid full adder structure and validation of these structure in different technologies that is 180nm, 90nm and 45nm using cadence tool.

2.PROPOSED METHODOLOGY

The suggested FA circuits were prescribed by 3 blocks is represented in Fig-1. Module-1 and module-2 were XNOR modules, that will produce a sum signal (SUM) and module-3 creates the Cout(output carry signal). Each module is composed separately with the end goal that the whole adder circuit is upgraded in terms of power, area and delay

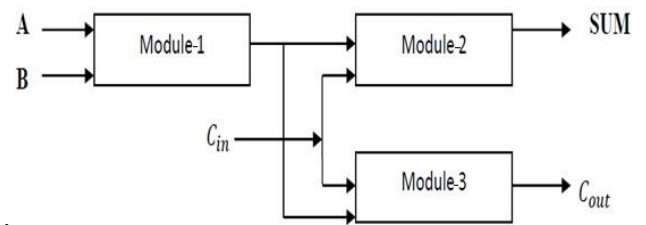


Fig-1: Schematic structure of proposed full adder

2.1 Altered XNOR-Module

In the suggested FA circuit, XNOR-module is in charge of the majority of the power utilization of the whole adder circuit. Subsequently, this module is intended to limit the power to the most desirable extend with by passing the voltage degeneration probability.

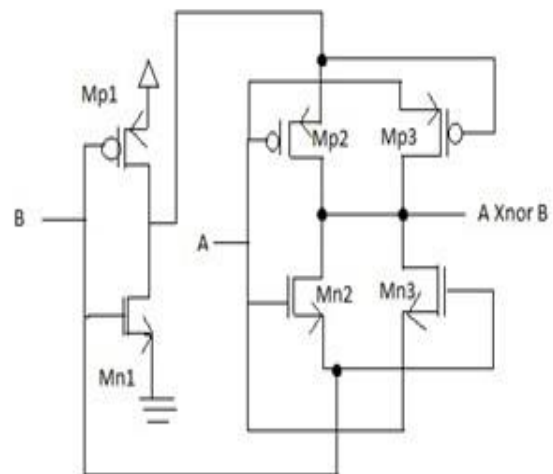


Fig-2: XNOR module.

The Modified XNOR circuit as demonstrated in a Fig-2 has a power utilization is decreasing remarkably by careful utilization of a weak inverter framed by Mp1 and Mn1 transistors. Moving faster into the levels of a output signals is ensured by level restoring of Mp3 and Mn3 transistors. Different topology of XOR/XNOR is already being described. The XOR/XNOR utilizes 4T's at the price of a low logic swing. Contrarily, the XOR/XNOR described in utilizes a 6T's to obtain preferred logic swing equated to a 4T XOR/XNOR circuit. Here the XNOR module houses 6T, but having distinctive transistor organization than that of 6T XOR/XNOR. The XNOR circuit introduced in this work is having a low power and high speed when compared with the 6T XOR/XNOR circuit.

2.2 Carry Generation Module

The transistors Mp7, Mp8, Mn7, and Mn8 are depicted in Fig-3 represents a output carry signal. Through a TG's (Mn7 and Mp7), the input carry signal (C_{in}) is being propagated. This will causes a reduction in a overall carry propagation path. The intentional utilization of strong TG's ensured further decrease in propagation delay of a carry signal.

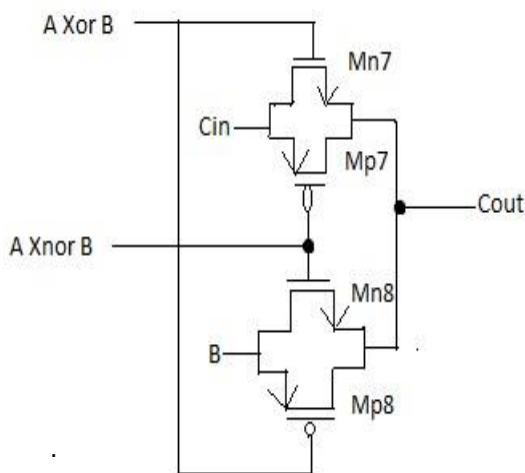


Fig-3: Carry generation module.

The CMOS and TGA logic developed a new concept of Hybrid Adder in different CMOS technologies using Cadence and compare the different technology results and analyze the Adder performance of the area, power and delay

2.1.1 Operation of the proposed FA.

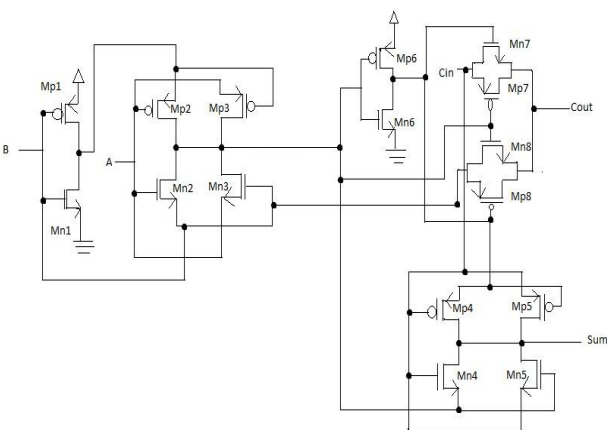


Fig-4: The circuit representation of proposed FA.

The Fig-4 demonstrates the detail outline of the proposed FA. The "sum" is being a output of a FA is formed

by the 2-XNOR modules. The transistors Mp1 and Mn1 of the inverter will generate B, it is successfully utilized to plan the controlled inverter utilizing a transistor pair Mp2 and Mn2. However, it is having some voltage degeneration issue, which is being removed by utilizing a 2 pass transistors Mp3 and Mn3. pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6) comprehend to a second stage XNOR module to form a total Sum operation. Looking at a truth table of a FA, the action for C_{out} is being generated and abstracted as follows:

$$\text{If, } A = B, \text{ then } C_{out} = B; \text{ else } C_{out} = C_{in}.$$

The unity between inputs A and B is analyzed by $A \odot B$ operation. In the event that they are same, at that point C_{out} is equal to B, it is achieved by utilizing the TG acknowledged by transistors Mp8 and Mn8. Contrarily, the input carry signal C_{in} is emulated as C_{out} which is achieved by other TG comprising of transistors Mp7 and Mn7.

3. PRINCIPLE OF IMPLEMENTING A PROPOSED FULL ADDER

First design and develop 1-bit proposed full adder using Cadence virtuoso and check the result in ADEL waveform window. 1 bit hybrid Full adder is designed by Hybridizing (that is combining) XNOR Module and Carry generation Module using Cadence virtuoso and check the result in ADEL waveform window. Validation and the results were also analyzed for 1 bit hybrid FA of 180nm, 90nm and 45nm technology using the Cadence virtuoso tool. The 1 bit hybrid FA circuit is extended to 4-bit FA circuit. By using the four 1 bit FA's which is connected in series. After applying the inputs Validation and the results were also analyzed for 4 bit hybrid FA of 180nm, 90nm and 45nm technology using Cadence virtuoso tool.

3.1 SPECIFICATIONS ANALYSIS

1) Power Analysis: Power measurement is being one of a key factor for designing a current VLSI circuits. Overall power loss includes static and dynamic losses.

$$P_{total} = P_{Static} + P_{Dynamic} \dots (1)$$

Conflict to early days, as a dynamic power losses conquered any additional form of power losses, with a latest move to UDSM level designing; currently static power losses too have become a major worry. There are two types of Power losses they are

- **Static Power loss:** Power leakage is calculated during the continuous flow of Voltage.
- **Dynamic Power loss:** Power leakage is calculated during the turning on and off of a circuit.

2) Delay or Lag Analysis: As a raise in count of inversion levels in series will lead to a enhancement in lag of a circuit. Interconnect capacitance, junction capacitance, Inter wire capacitance, intra wire capacitance; each of these capacitances will matters for the improved delays.

$$tpd = (C/I) \Delta V(2)$$

Logical effort(C/I) details for all these factors quantitatively. Dynamic circuits were built with the purpose to utilize the internal capacitances to grip some important information which in case of static circuits is merely because of delays. These circuits sustained to be very beneficial when fast operation speeds are essential.

3.2 SIMULATION ANALYSIS

Each circuit is simulated using BSIM 3V3 180nm, 90nm and 45nm technology on Tanner EDA tool. Every circuits are being simulated on explicitly similar input patterns which valid for impartial testing environment. Each simulation is being operated on a bound of voltages 1.8v,1.2v and 1v for 180nm, 90nm and 45nm technologies respectively. Schematics of 1 bit FA and 4 bit FA for 180nm, 90nm and 45nm technology were designed and simulated for the results.

3.3 CIRCUIT IMPLEMENTATION OF 1-BIT PROPOSED FA

The Circuit realization of 1-bit proposed FA of 180nm technology is as shown in the Schematic Fig-5.

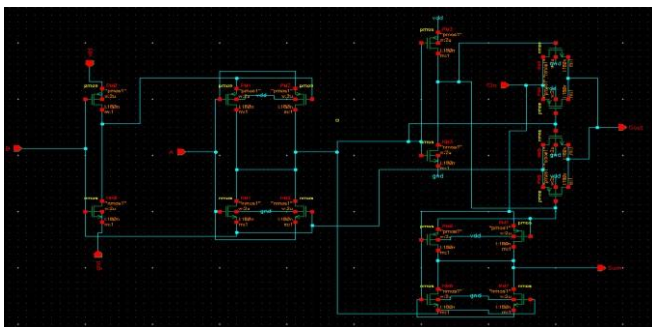


Fig- 5: Schematic representation of 1-bit proposed full adder of 180nm technology

It includes 16 transistors of 180nm as the minimum possible length in 180nm technology. The schematic consist of A, B, Cin, vdd and gnd as inputs and Cout and Sum as outputs. In this circuit module1 and module2 is implemented with XNOR module to get Sum as the output, but module3 is implemented by carry generation module to get Cout as the output. The nMOS and pMOS will be set to L=180nm and W=2µm respectively as a default value.

3.4 CIRCUIT IMPLEMENTATION OF 1-BIT PROPOSED FA OF 90nm TECHNOLOGY

The Circuit implementation of 1-bit proposed FA of 90nm technology is as shown in the Schematic Fig-6, which consist of 16 transistors of 90nm as the minimum possible length in 90nm technology. The schematic consist of A, B, Cin, vdd and gnd as inputs and Cout and Sum as outputs. In this circuit module1 and module2 is implemented with XNOR module to get Sum as the output, but module3 is implemented by carry generation module to get Cout as the output. The nMOS and pMOS will be set to L=100nm and W=120nm respectively as a default value.

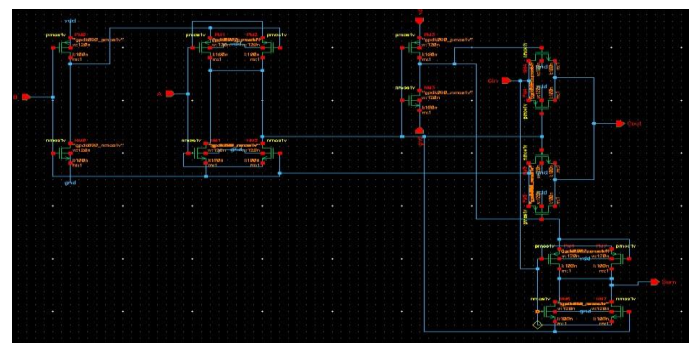


Fig-6: Schematic representation of 1-bit proposed full adder of 90nm technology

3.5 CIRCUIT IMPLEMENTATION OF 1-BIT PROPOSED FA OF 45nm TECHNOLOGY

The Circuit implementation of 1-bit proposed FA of 45nm technology is as shown in the Schematic Fig-7, which consist of 16 transistors of 90nm as the minimum possible length in 45nm technology. The schematic consist of A, B, Cin, vdd and gnd as inputs and Cout and Sum as outputs. In this circuit module1 and module2 is implemented with XNOR module to get Sum as the output, but module3 is implemented by carry generation module to get Cout as the output. The nMOS and pMOS will be set to L=45nm and W=120nm respectively as a default value.

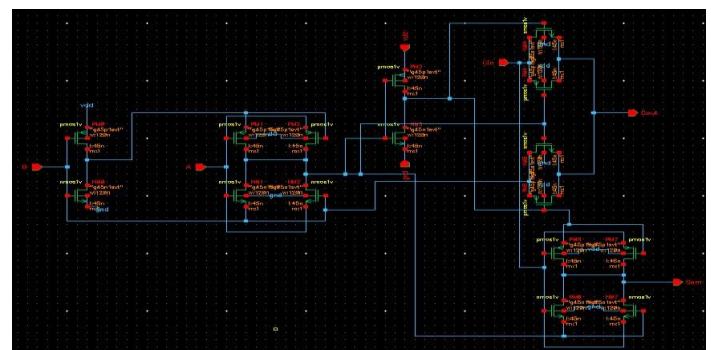


Fig-7: Schematic representation of 1-bit proposed full adder of 45nm technology

3.6 CIRCUIT IMPLEMENTATION OF 4-BIT PROPOSED FULL ADDER

Till now we have discussed about the 1-bit proposed FA circuit. By using 1-bit proposed FA circuit we can extend our design by connecting the full adder circuit in series. The 4-bit proposed FA circuit is interpreted as shown in the Fig-8 and is being implemented in 180nm, 90nm and 45nm technologies. To implement 4-bit proposed full adder circuit, four 1-bit FA symbols are connected in series with $A_0-3(A_0, A_1, A_2, A_3)$, $B_0-3(B_0, B_1, B_2, B_3)$, C_{in} , v_{dd} and gnd as input pins, and $C_0-3(C_0, C_1, C_2, C_3)$ and $S_0-3(S_0, S_1, S_2, S_3)$ as output pins. The carry generated in the first 1-bit adder is fed as C_{in} and the process repeats till the last adder.

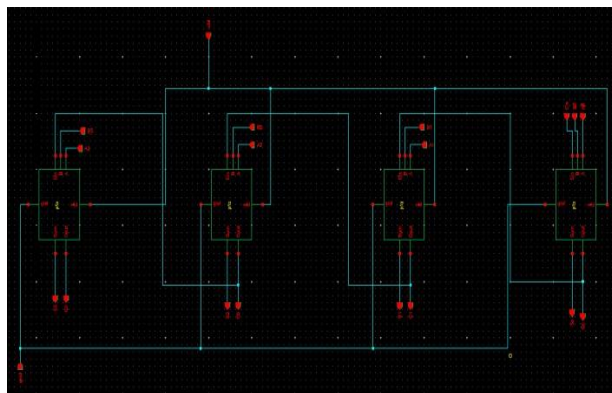


Fig -8: Schematic representation of 4-bit proposed full adder of 180nm technology.

4 RESULTS

The Test Schematic representation and output waveform of 1-bit proposed FA and 4-bit proposed FA is obtained and is shown for different technologies like 180nm, 90nm and 45nm as shown in the figures below

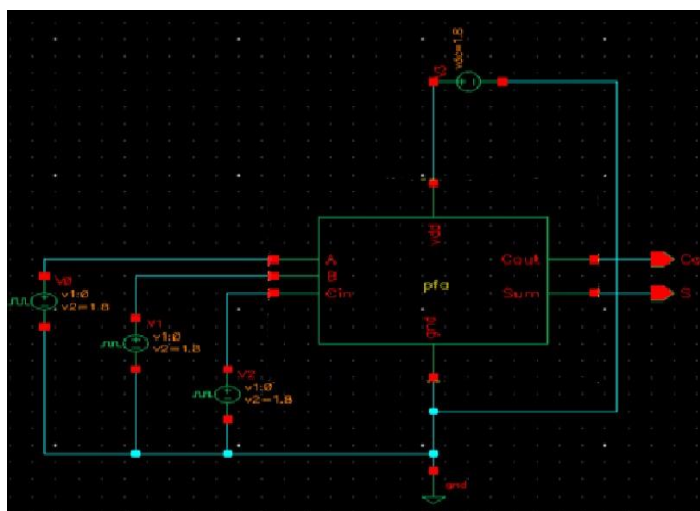


Fig-9: Test Schematic representation of 1-bit proposed FA circuit of 180nm technology

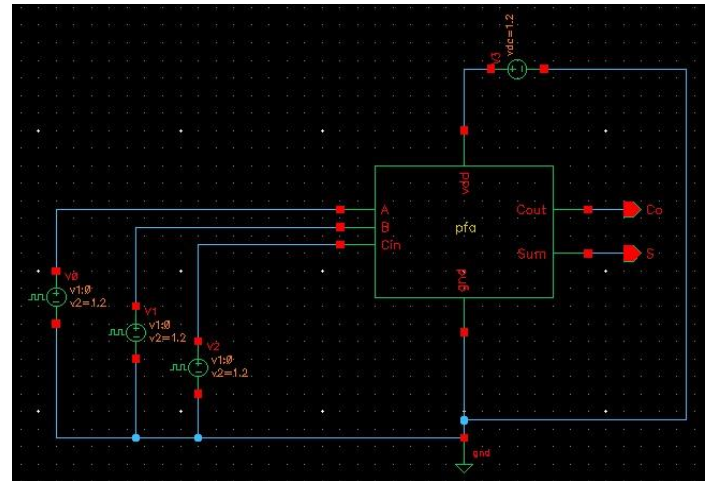


Fig -10: Test Schematic representation of 1-bit proposed FA circuit of 90nm technology

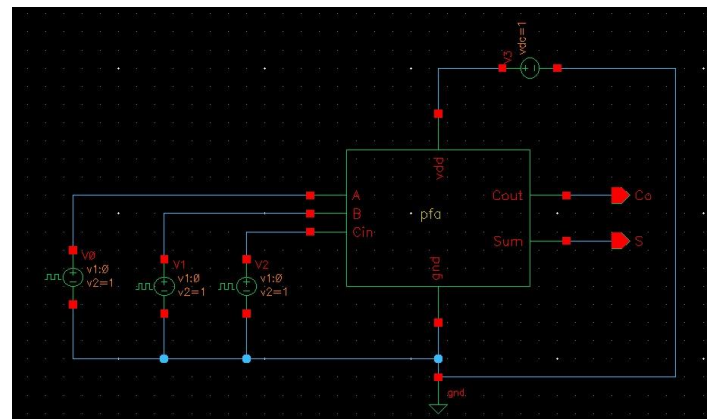


Fig -11: Test Schematic representation of 1-bit proposed FA circuit of 45nm technology

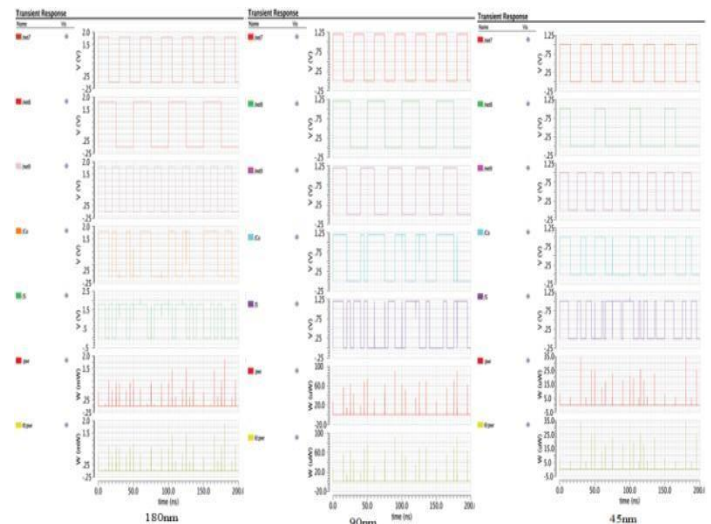


Fig-12: Transient response of 1-bit proposed FA.

Table -1: Results comparison of power between various technologies for 1-bit proposed full adder.

Sl.no.	Parameters	180nm	90nm	45nm
1	Static Power (μw)	43.15	2.342	0.3115
2	Dynamic Power (nw)	0.6447	892.1	0.09397
3	Power dissipation (μw)	43.1506	3.2341	0.31159

Table -2: Results comparison between various technologies for 1-bit proposed full adder.

Sl.no.	Parameters	180nm	90nm	45nm
1	Operating voltage	1.8v	1.2v	1v
2	Power(μw)	15.115	0.18315	0.10937
3	Current(μA)	8.3975	0.14965	0.10937
4	Transmission Delay(pS)	86.39	81.62	25.99
5	DC Power (μw)	37.39	7.767	5.275
6	Power dissipation (μW)	12.190	0.8490	0.0709
8	Storage capacity	1-bit	1-bit	1-bit
9	Hybrid full adder implementation	16T	16T	16T
10	Operating Temperature	27 °C	27 °C	27 °C

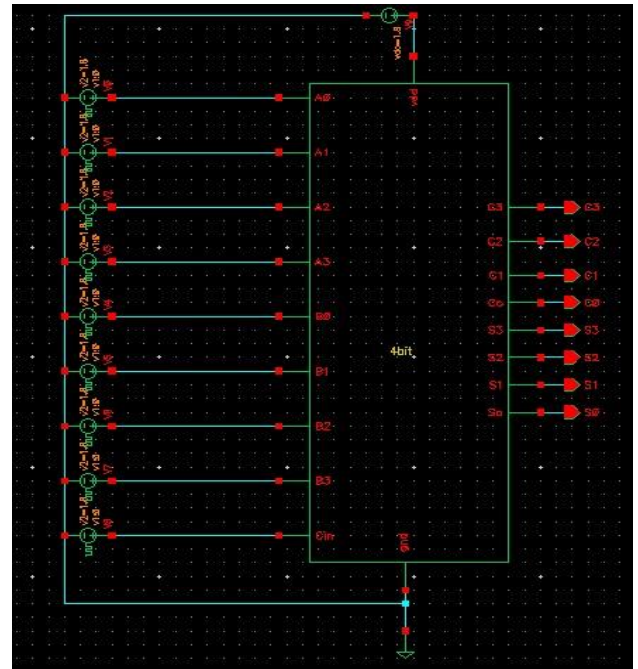


Fig -13: Test Schematic representation of 4-bit proposed FA of 180nm technology

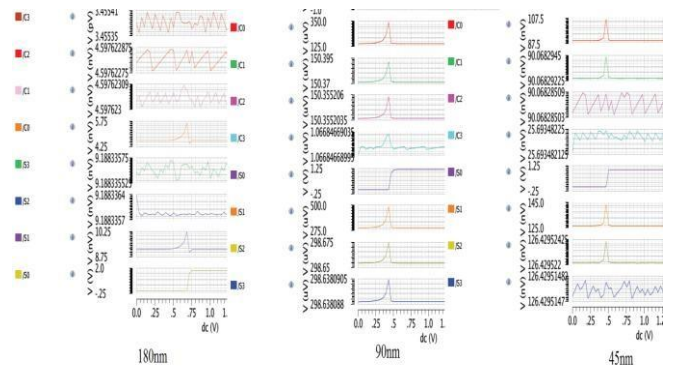


Fig-14:Transient response of 4-bit proposed FA

Table -3: Results comparison of power between various technologies for 4-bit proposed full adder.

Sl. no	Parameters	180nm	90nm	45nm
1	Static Power (μW)	12.19	0.6259	0.07091
2	Dynamic Power (nW)	0.1553	223.1	0.02425
3	Power Dissipation (μW)	12.190	0.8490	0.0709

Table -4: Results comparison between various technologies for 4-bit proposed full adder.

Sl.no	Parameters	180nm	90nm	45nm
1	Operating voltage	1.8v	1.2v	1v
2	Power(μ w)	27.56623	2.817567 2	0.07831 6827
3	Transmission Delay(pS)	112	103.3	92.93
4	Power dissipation (μ w)	43.1506	3.2341	0.31159

4. CONCLUSIONS

In this work, a low power hybrid 1 bit and 4 bit FA has been presented. The simulation is done by utilizing standard Cadence Virtuoso tools with 180nm, 90nm and 45nm technologies and results of another standard design approaches are compared. In the previous work they are using a TGA Logic for both carry and sum block. But the proposed 1-bit FA combining the two different structures that is TGA for carry block and CCMOS for Sum block. Therefore the proposed structure of 1-bit FA uses only 16T's instead of 20T's compared with the previous work.

The proposed 1-bit FA is compared with the different technologies with different parameters(Propagation delay and power dissipation). The comparison statements are briefly discussed in result section.

The Transmission Delay of 1-bit FA in 180nm is 86.39ps, 90nm is 81.62ps and 45nm is 25.99ps. Similarly Power dissipation of 1-bit FA in 180nm is 12.1901 μ w, for 90nm is 0.8490 and 45nm is 0.0709 μ w.

The 1-bit proposed FA circuit is extended to 4-bit and the results compared with the same technologies. The operating voltages required are decreases when technology shrinks. Similarly the power consumption reduces with the technology shrinks. Thus we can say that area can be reduced with the decrease in transistors widths and length.

The Transmission Delay of 4-bit FA in 180nm is 112ps, 90nm is 103.3ps and 45nm is 92.93ps. Power dissipation of 4-bit FA in 180nm is 43.1506 μ w, 90nm is 3.2341 μ w and 45nm is 0.31159 μ w.

Finally this method improved scheme is proposed. This method compared with different technologies saves more hardware resources. For the further reduction of hardware we can perform the ASIC design flow by doing this we can greatly reduce the number of logics hence we can reduce the hardware utilization and also we can reduce the area gate and power.

4.1 FUTURE WORK

As a future scope, enhancing the execution of 1 bit FA's can be executed by changing the value of W/L proportions. Utilizing the design of 1 bit proposed FA blocks, we can implement a 2 bit, 4 bit, 8 bit, 16 bit, 32 bit, 64 bit Subtractor/Adder circuits. These adders can also be design and differentiate using different possible nm technologies like 180nm, 90nm, 65nm, 32nm, 22nm, and so on.

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