

CFOA based Mos-C Single Resistance Controlled Sinusoidal Oscillator

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Abstract - In this paper, a Single resistance controlled Sinusoidal Oscillators is presented using a single current feedback operational amplifier (CFOA). The main feature of this circuit configuration is that frequency of oscillation (FO) and condition of oscillation (CO) can be controlled by single resistance. It uses single CFOA and minimum passive components that are three voltage controlled resistors and one capacitor only to realize oscillator response. The circuit topology is verified by simulating the circuit on PSPICE using TSMC 0.35 μ m CMOS Technology process parameters with supply voltages of +/- 1.25V and controlling voltage $V_{b1}=0.35V$, $V_{b2}=-0.55V$. The simulated and theoretical results were found to be in good agreement with each other.

Key Words: Single resistance controlled oscillator (SRCO), CFOA, CMOS, voltage controlled resistor (VCR).

1. INTRODUCTION

Versatile Analog integrated circuits are the essential building block of continuous time signal processing circuits and they find extensive applications in communication, instrumentation systems and control engineering. Sinusoidal oscillators play very important role in signal processing, instrumentation and measurement, control systems and communication engineering applications.

From the literature survey on oscillators, it can also be inferred that there has been emphasis on realizing single-element or single-resistance-controlled oscillators (SRCOs) because of their usefulness and ease of operation. Furthermore, the reduction in the design complexity and the convenience of realization has led to the evolution of a number of SRCOs involving different types of active building blocks [1]-[16]. The SRCO realizations are called canonic which employ a minimum number of passive components i.e. only three resistors and two capacitors in [4]-[7] and [10]-[14]. The research on implementations of single-element-controlled oscillators or SRCO with the following significantly advantageous features has received prominent attention of researchers; (a) employment of two grounded capacitors (GC) as preferred for integrated Circuit implementation, along with the minimum numbers of (only three) resistors, (b) non-interacting control of conditions of oscillation (CO) and frequency of oscillations (FO), (c) a simple CO (i.e. not more than one condition of oscillation), (d) use of readily available off-the-shelf active building block

(ABB) for implementing these SRCOs and (e) in some cases, the availability of explicit output.

Various type of single resistance controlled sinusoidal oscillator (SRCO) circuits have been reported in literature using different building blocks such as operational amplifier[2], operational trans-conductance amplifier [3], current conveyors [4] and current feedback operational amplifier (CFOA) [5-16]. During the last few decades, current mode signal processing circuits are receiving considerable attention over SRCO [7-8] due to its advantageous features such as wide bandwidth, high slew rate, greater linearity, simpler circuitry, low power dissipation, faster response time and larger dynamic range [17-18]. Due to the advancement in current mode circuits new building blocks have been reported such as CMOS based Current feedback Operational Amplifier (CFOA). CMOS based CFOA is one of the current mode building blocks that provide all the advantages offered by current mode processing circuits. CMOS based CFOA provides features such as high slew rate, wide bandwidth, simple implementation, high CMRR, high input impedance and low power dissipation in compare to BJT based CFOA. In addition to this, it is minimizing parasitic capacitances as its input terminals and output terminals therefore it is suitable for high frequency and medium frequency operations. High output impedance at the z terminal of CMOS based CFOA facilitates easy driving an external load without additional current buffers. As far as the application of CMOS based CFOA is concerned various current mode and voltage mode filters and oscillators. Shen-luan Liu *et al.* [19] presented new sinusoidal oscillators with single element control using a BJT based current-feedback amplifier (CFA). The oscillation frequency of the sinusoidal oscillators can be controlled by a resistor or capacitor. The oscillation frequency of one of the sinusoidal oscillators is insensitive to the input and output voltage tracking errors of the CFA. Senani R. and Singh V.K. [20] presented a family of SRCO using a single BJT based current feedback operational amplifier (CFOA). Frequency of oscillation and condition of oscillation is controlled by single resistance.

In this paper single resistance controlled sinusoidal oscillator (SRCO) is designed that realizes oscillation responses and does not involve any component matching constraints. It is free from internal parasitics of CFOA, because internal parasitics (resistance and capacitor) is connected with CFOA's Z-pin. The SRCO is designed with single CMOS based CFOA and passive elements (resistance)

is realized with voltage controlled resistance (VCR). The theoretical results are verified by simulating the circuit on PSPICE software using TSMC 0.35µm CMOS model parameters. By placing appropriate values of the resistor and capacitor the pole frequency is kept at 137.42 MHz for oscillation responses. The simulation result shows that the circuit works KHz, MHz and is suitable for high and medium frequency operations.

1.1 CURRENT FEEDBACK OPERATIONAL AMPLIFIER (CFOA)

The symbolic representation of Current feedback operational Amplifier (CFOA) and its equivalent circuit is given in Fig. 1 and Fig. 2 respectively.

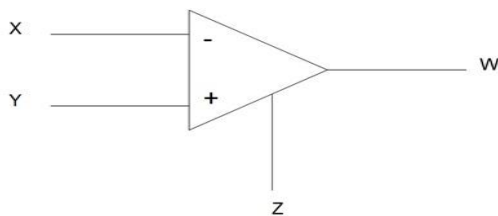


Figure -1: Symbolic Representation of CFOA [17]

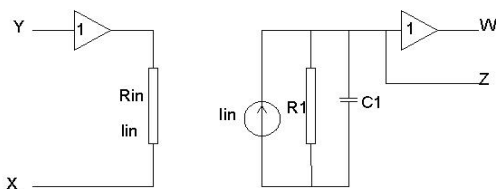


Figure -2: Equivalent Circuit of CFOA [17]

It's ideal and non-ideal port relationship can be characterized as follows:

A. Ideal part relationship-

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \\ i_w \end{bmatrix} \quad (1)$$

The ideal matrix equation is given as:

$$V_x = V_y, I_z = I_x, I_y = 0, V_w = V_z$$

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & \beta & 0 & 0 \\ 0 & 0 & \gamma & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \\ i_w \end{bmatrix} \quad (2)$$

The Non ideal matrix equation is given as:

$$V_y = \alpha V_x, I_z = \beta I_x, V_w = \gamma V_z, I_y = 0$$

Where $\alpha = (1 - \epsilon_1)$ ($\epsilon_1 \leq 1$) denotes the current tracking error of a CFA, $\beta = (1 - \epsilon_2)$ ($\epsilon_2 \leq 1$) is the input voltage tracking error, and $\gamma = (1 - \epsilon_3)$ ($\epsilon_3 \leq 1$) is the output voltage tracking error.

CFOA is a four terminal device. Here, X and Y is the inverting and non-inverting input terminal respectively and Z and W are the output terminals. X terminal offers very low input impedance while Y terminal has very high input impedance. The two output terminal Z and W have very high and very low output impedances respectively. The input impedance of CFOAs is high for the positive (Y) input and low for the negative (X) input. The non-inverting input of CFOA is connected to the input of a unity gain, which usually takes the form of emitter follower circuit. Since the non-inverting input is the input of a buffer, it's a high impedance input. Now, because this buffer's output connects to the inverting input impedance. A current flow through the inverting input (X) that generates a voltage which is equal to current times the trans-impedance. This converts high input impedance to low output impedance which must be present at the load to get maximum current in order to drive load of the CFOA.

1.2 CIRCUIT CONFIGURATION

The circuit configuration is shown in Fig. 4. The circuit is a single resistance controlled sinusoidal oscillator. In SCRO condition of oscillation and frequency of oscillation is controlled by single resistance. It uses minimum number of active and passive components i.e. one CFOA, three voltage controlled resistor (VCR) and one capacitor. It requires internal parasitics resistance and capacitance (connected to CFOA's Z-pin) to realize oscillator response to produce frequencies KHz to MHz.

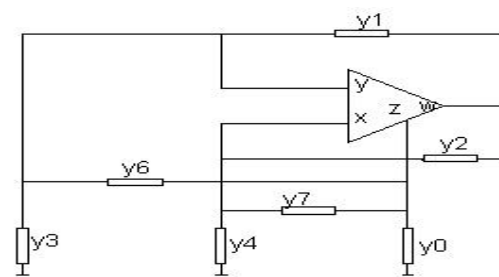


Figure -3: General Configuration for synthesis of SCROs [20]

It is known that for canonic realization (employing only two capacitors) of a SCRO, a minimum of five elements are necessary, a generalized five-node structure, which can be used to enumerate the set of canonic SCROs, can be formulated. After eliminating the elements rendered redundant (shown by dotted lines) by the constraints imposed by the characterizing equation of the CFA, this is reduced to the form shown in Fig 3. Synthesis of the

oscillation then follows the same methodology. To conserve space, we omit the details and present here only the final result and observations, restricting ourselves only to the realization of variable frequency SCROs (although a number of new single-frequency oscillators also emerge from the process). The general characteristic equation of this structure is found to be

$$y_0(y_1 + y_3 + y_6) + y_3(y_2 + y_6 + 2y_7) - y_4(y_1 + y_6) = 0 \quad (3)$$

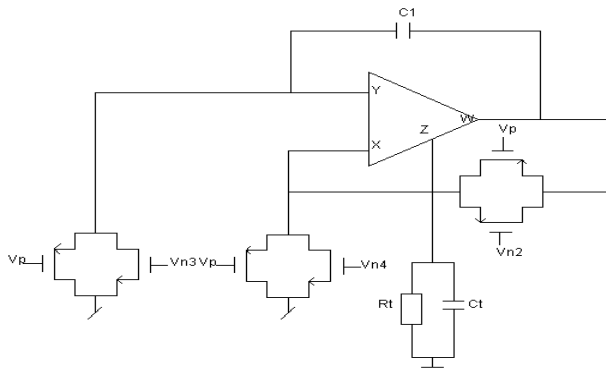


Figure -4: Oscillator circuit configuration [20]

The circuit configuration is based on the above SCRO admittance configuration in which Z-port connected with internal parasitics (resistance and capacitance). With this configuration no of passive elements is reduced and in this circuit

$$y_3 = \frac{1}{R_3}, y_2 = \frac{1}{R_2}, y_4 = \frac{1}{R_4}, y_1 = sC_1, y_0 = \frac{1 + sR_4C_1}{R_4} \quad (4)$$

With taking these values in the above equation, the characteristics equation is

$$s^2 + \frac{s}{C_1 R_3 C_2} \left(C_2 + \frac{C_1 R_3}{R_2} - \frac{R_3 C_1}{R_4} \right) + \frac{1}{C_1 R_3 C_2} \left(\frac{1}{R_4} + \frac{1}{R_2} \right) = 0 \quad (5)$$

With the help of these equation on comparison Frequency of oscillation (FO)-

$$\omega_0 = \sqrt{\frac{1}{R_3 C_2 C_1} + \frac{1}{R_2}}$$

Condition of oscillation (CO)-

$$\frac{R_3}{R_4} = \frac{C_2}{C_1} + \frac{R_3}{R_2}$$

In this SRCO, frequency of oscillation (FO) is controlled by R3 and condition of oscillation is adjustable by resistance R4. To add IC implementation feature to the oscillator, R is realized using two MOSFET transistors operating in the

ohmic region, see Fig. 5, which are electronically tuned through voltage Vn2, Vn3, Vn4 of Fig. 4. A simple analysis shows that, with matched transistors, the nonlinearity of each transistor will be cancelled by its counterpart. As a result a linear programmable resistor is obtained and given by:

$$R = \frac{1}{K_o(V_{n1} - V_p - V_{tn} + V_{tp})} = \frac{V_1 - V_2}{I} \quad (6)$$

Where Ko and Vt are transistor's Trans conductance and threshold voltage respectively.

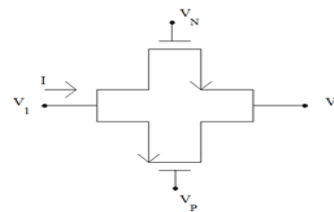


Figure -5: Basic structure of Voltage controlled Resistor (VCR) [21]

Equation shows that R is linear resistor and can be controlled through biasing voltages Vn and Vp. In our case Vp is fixed at -0.65 V while Vn is adjusted through the value of resistance that is why the condition of oscillation is achieved.

1.4 FREQUENCY STABILITY FACTOR (Sf)

The frequency stability of an oscillator is a term used to characterize how small the frequency fluctuations of the oscillator signal are. We usually refer to frequency stability when comparing one oscillator with another. Using the definition of the frequency stability factor (Sf) as

$$Sf = \left. \frac{d\phi}{du} \right|_{u=1} \quad (8)$$

Where u= w/w0 is the normalized frequency and Φ (u) represents the phase function of the open loop transfer function, with C1=C2=C, R2=R3=R and R1=R/n, Sf, for the circuit is found that

$$Sf = 2\sqrt{n} \quad (9)$$

Which is larger as in the current conveyer (cc) based oscillator in compare to the op-amp. Particularly when the passive components are realized with precision at voltage controlled resistor (VCR) then the frequency stability factor (Sf) will be too low, tend to the unity.

2. SIMULATION RESULTS

The presented circuit configuration is simulated and verified by PSPICE software using TSMC 0.35µm CMOS process parameters with supply voltages of +/-1.25V and controlling voltage Vb1=0.35V, Vb2= -0.55V. The obtained oscillator responses are given in Fig 6.

The circuit is designed for fo = 137.42 MHz. The values for passive components are calculated from condition as follows:

$$C_t = 0.001\mu F, C_1 = 0.001\mu F, R_t = 50K, V_p = -0.65V, V_{thn} = 1V, R_3 = 1K$$

$$V_{thp} = -1V, V_{n3} = 0.758V, V_{n2} = 0.724V,$$

$$V_{n4} = 0.702V, R_2 = 1.8K, R_4 = 1.25K$$

$$K_0 = 36.185 \frac{\mu A}{V^2} \text{ (Simulated)}$$

Power supply is chosen ±1.25V (DC).

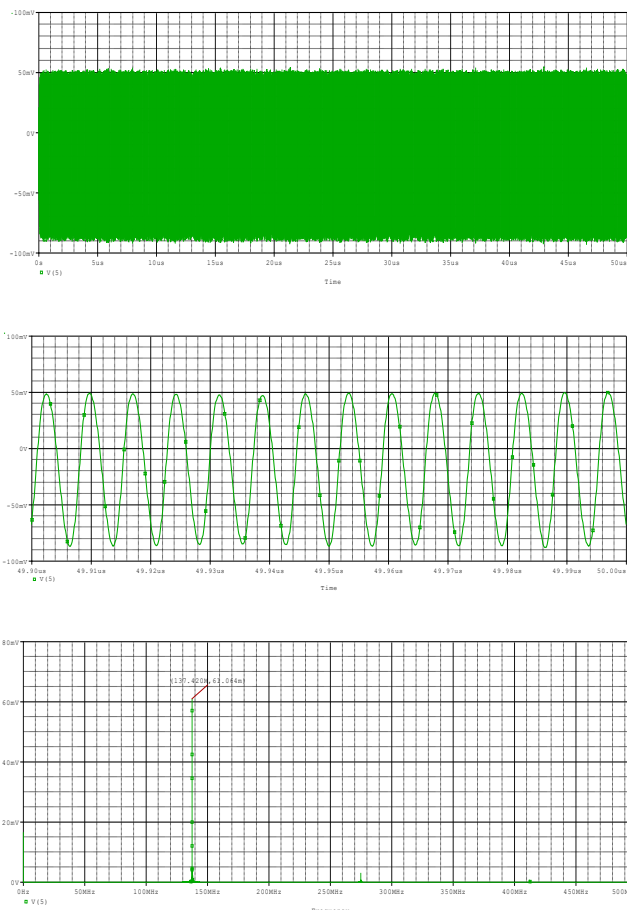


Figure -6: Simulation result of presented circuit

The CMOS realization of CFOA is shown in Fig. 7 [22]. To check the workability of CMOS based CFOA, we have carried out SPICE simulation of SRCO instead of BJT based CFOA.

The aspect ratio of NMOS and PMOS is shown in Table 2 and parameters of CMOS based CFOA in Table 3.

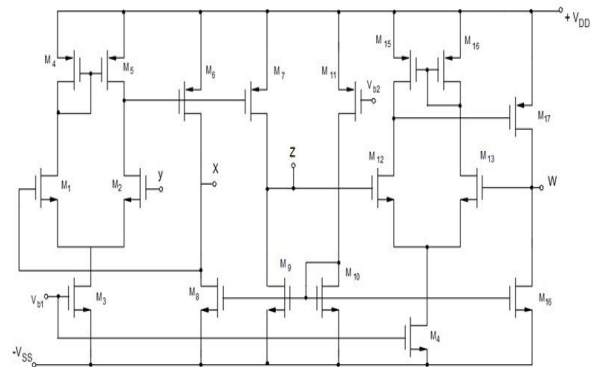


Figure -7: CMOS realization of CFOA. All the controlling voltage and supply voltages are selected as 0.35V and -0.55V and +/-1.25V, respectively [22]

Table -2: Transistor aspect ratio of the CFOA [22]

Transistor	W [µm]	L [µm]
M1-M3	15	1
M8-M10	15	1
M12-M14	15	1
M18	15	1
M4-M7	20	1
M11	20	1
M15-M17	20	1

3. CONCLUSION

In this paper single resistance controlled sinusoidal oscillator presented that realizes oscillation of sinusoidal frequency. Oscillator frequency is varying with the help of Vn3. So this oscillator is variable frequency oscillator. The presented circuit uses minimum active and passive component i.e. one CFOA, three voltage controlled resistors (VCR) and one capacitor. It is free from internal parasitics of CFOA. It offers low power dissipation, low output impedance and high input impedance. Use of voltage controlled resistor (VCR), which is useful for IC implementation. Frequency stability factor is better than previous circuit. The presented circuit topology is verified by simulating the circuit on PSPICE using TSMC 0.35µm CMOS process parameters with +/- 1.25V supply voltages and controlling voltage Vb1=0.35V, Vb2= -0.55V. The presented circuit works very well at high frequencies and medium frequency above MHz and KHz range therefore; it is suitable for high frequency and medium frequency applications. The theoretical and simulated results are found to be in good agreement with each other.

ACKNOWLEDGEMENT

The authors would like to thank Prof. V.K. Singh for the statistical support and the guidance. The authors would also like to thank Institute of Engineering & Technology, Lucknow for providing the Tools and Technology for the work to be completed.

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BIOGRAPHIES :



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