Design & Simulation of Half Adder Circuit Using AVL technique based on CMOS Technology

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Abstract - *Power optimization is a technique used in low voltage applications. Arithmetic circuits play a crucial role in designing of any VLSI system. In this paper, Arithmetic circuits are designed using Adaptive Voltage Level (AVL) techniques. This technique consumed less power as compare to conventional design. Total power dissipation is reduced by applying the AVLS (adaptive voltage level at supply) technology in which the supply potential is increased and AVLG (adaptive voltage level at ground) in which the ground potential is raise. This paper shows how we can control power using AVL techniques. The AVL technique based on Arithmetic circuit is compared to conventional design which is based on total power consumption, propagation delay, layout area, speed and is more preferred.. The result indicates that the significant reduction in power consumption of this proposed cell with the AVL technique. This design is better in designing the system that consumed less power. All the circuits are simulated on tool Micro Wind 3.1 and DSCH in 65 nanometer CMOS technology.. This technique reduces the total power dissipation by applying the adaptive voltage level at ground (AVLG) technology in which the ground potential is raised and adaptive voltage level of supply (AVLS) in which supply potential is increased. The main aim of the design is to investigate the power dissipation, power delay product, layout area, routing wires for Arithmetic circuit for the proposed design style. The simulation results shows that in all the technique AVL technique is more preferred because it takes less power consumption, delay ,fast response as compared to other techniques.*

Key Words: *Arithmetic circuits, AVL techniques, Low Power, High Speed, VLSI*

1. INTRODUCTION

The simplest combinational circuit which performs the arithmetic addition of two binary digits is known as half adder.. It is the necessary building block for designing any VLSI system. Figure 1.1 shows the logic diagram of half adder. Table 1.1 represents truth table of half adder. It adds two inputs and produces the two outputs in the form of sum and carry. The sum is 1 when either of the input is one. The sum is 0 when both the inputs are 0 or

Carry is one when both the inputs are 1. From the truth table the logical expression of sum output can be written as a sum of product expression by summing the inputs for which the sum is 1. S = A'B + AB' this expression can be simplified as XOR form

$$S = A \oplus B$$

Carry output can be written as product of sum expression for which the carry is 1. Cout = AB

1.1 Related Work

There are many papers that have been published for reducing the power consumption of the arithmetic circuits such as half adder, Full adder, Comparator and half subtractor. All are based on different methodologies for various Logic style. In such papers they have designed the circuit by using various logic design style Complementary Pass Transistor design style, Transmission Gate design style, Hybrid CMOS design style, Bridge design style and many more design style. All these designs are modified by using the technique adaptive voltage level .It has two types. The first is AVLG technique in which the ground potential is raised and second is AVLS technique in which supply potential is increased. By using AVL technique various parameter like power consumption, layout area, propagation delay, and power delay product are reduced. .The main drawback using AVL technique is the number of routed wires is increased.

1.2 Proposed Half Adder Design Style

In the proposed design of Half Adder the circuit is design via XOR/XNOR & Transmission Gate design style as hybrid design and introduces this conventional design

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with AVL techniques. Variation in technology scaling introduces the variation in parameters values. If the technology is reducing more & more than the desired system would be more suitable for low power, low propagation delay and high performance. For these performance AVL techniques such as AVLG (adaptive voltage level at ground) technique in which the ground potential is raised and AVLS (adaptive voltage level at supply) technique in which supply potential is increased. For this design total number of 09 transistors is required for the operation of Half Adder. As compared to the other design style the proposed AVL technique has the following advantages such as low power dissipation, low propagation delay, less No. of transistors, less Layout area, high performance and less PDP . So that this design style makes the Half Adder more efficient .The most affected design is via AVLS technique.

1. CMOS IMPLEMENTATION OF HALF ADDER CIRCUIT

The circuit is designed using CMOS as combination of Pull-up and Pull-down networks. The function of the Pull-up network is to provide a connection between the output and VDD when the output of the logic gate is meant to be

1. The function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0.

16 numbers of transistors are needed for the implementation of half adder using CMOS. Figure shows the circuit diagram of Half Adder using CMOS design style. This design has numerous disadvantages such as more power consumption, propagation delay, routing wires and layout area. So this design is not widely used due to complex structure. Layout cell, Simulation result, MOS characteristic and Variation of Power Vs Supply voltage is shown in Fig
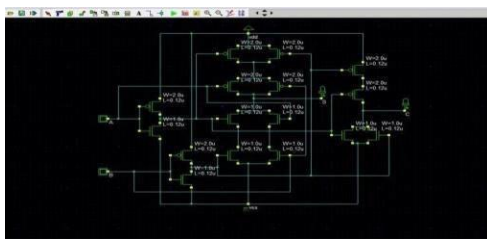

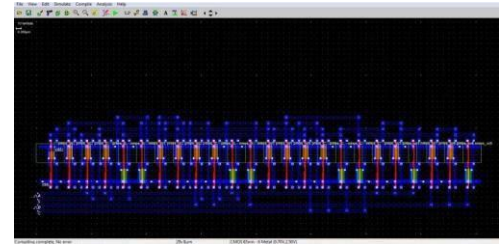Fig2.1: Circuit Diagram of Half Adder using CMOS Design
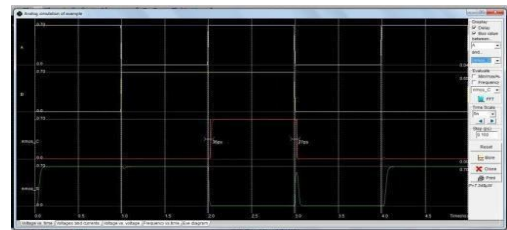

Fig2.2: Layout cell of Half Adder using CMOS Design

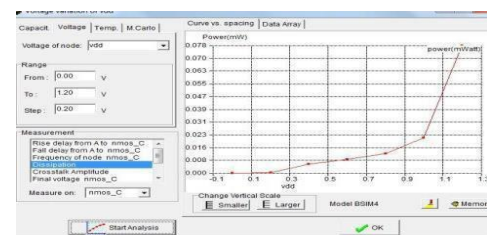Fig2.3: Simulation Waveform of Half Adder using CMOS design

Fig2.4: Variation of Power Vs Supply voltage of Half Adder using CMOS

Conventional Design of Half Adder

In conventional design of Half Adder the circuit in designed using Transmission Gate & XOR/XNOR based. Design style that requires less no. of transistors. Figure shows the circuit diagram of conventional design of Half Adder. This design requires only 6 transistors to implement the Half Adder. It requires 3 PMOS and 3 NMOS transistor to implement the Half Adder which is very less as compared to CMOS half Adder Design. The cell layout design of conventional half adder is simulated by Microwind 3.1 software at 65 nm technology at Vdd = 1.0 V at Temp. 27° C .this design consumes less power, propagation delay, layout area, routing wires, PDP as compared to CMOS Half Adder. Layout cell, Simulation result, MOS characteristic and Variation of Power Vs Supply voltage is shown in Fig
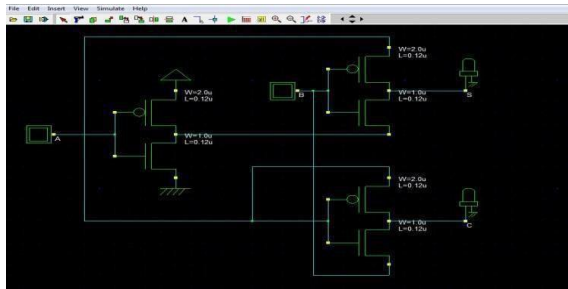
3.3.1 AVLG Technique

Fig3.1: Circuit Diagram of Conventional Half Adder
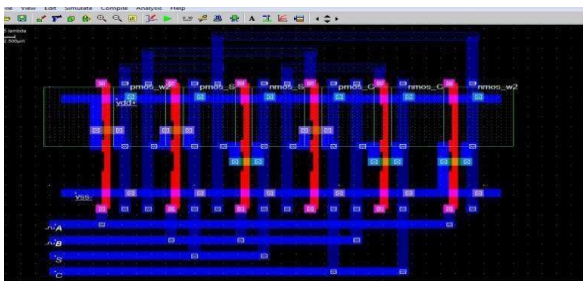

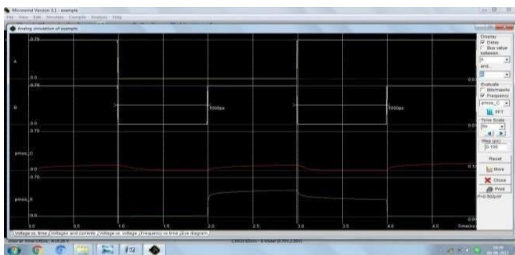Fig3.2: Layout Cell of Conventional Half Adder

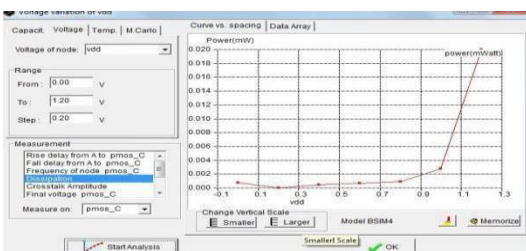Fig3.3: Simulation Waveform of Conventional Half Adder

Fig3.4: Variation of Power Vs Supply voltage of Conventional Half Adder

3.3 Design of Half Adder using AVL Technique

Adaptive voltage level technique is used to reduce the power consumption, propagation delay, layout area, PDP as compared to CMOS and conventional Half Adder design. In AVLS technique an additional control circuit is used at the upper end of the circuit to bring down the supply voltage. In AVLG technique control circuit is used

at the lower end of the circuit to lift the ground potential of conventional half adder circuit.

In AVLG technique, a combination of 1 N-MOS & 2 P-MOS circuits are connected in parallel. An input clock pulse is applied to the N-MOS of circuit of AVLG and all the P-MOS are connected to ground. This AVLG circuit is connected at the ground terminal of conventional one by removing ground. It would lift the ground potential of the circuit to reduce the power consumption of the conventional half adder design. Depending upon the input signal the output also varied and the usage of clock pulse is to prevent any defect in half adder during power consumption. The cell layout design of conventional half adder using AVLG technique is simulated by Microwind 3.1 software at 65 nm technology at Vdd = 1.0 V at Temp. 27° C .this design consumes less power, propagation delay , layout area , PDP as compared to CMOS and conventional Half Adder. Layout cell, Simulation result, MOS characteristic and Variation of Power Vs Supply voltage is shown in Fig.
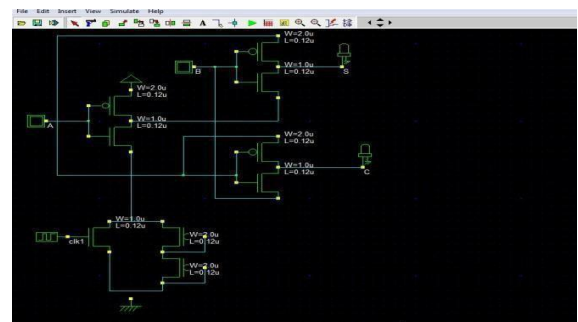

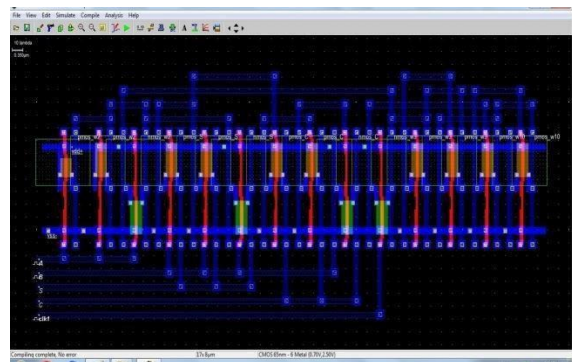Fig4.1: Circuit Diagram of Half Adder using AVLG Technique

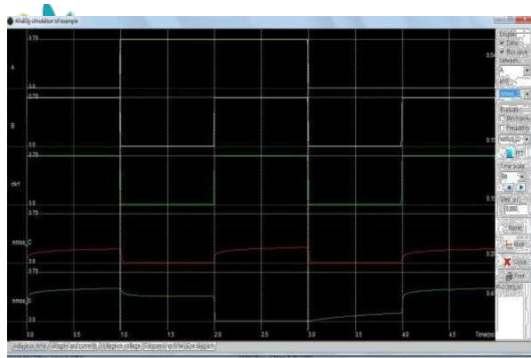Fig4.2: Layout cell of Half Adder using AVLG Technique

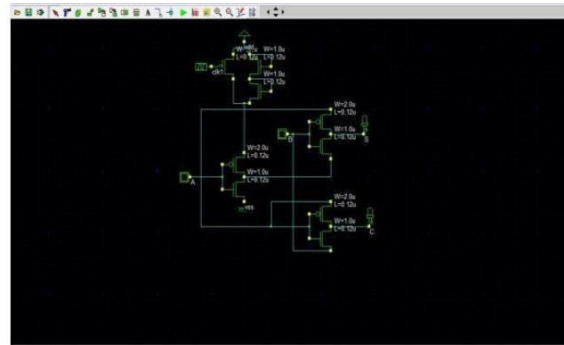Fig4.3: Simulation Waveform of Half Adder using AVLG Technique

Fig4.4: Variation of Power Vs Supply voltage of Half Adder using AVLG Technique
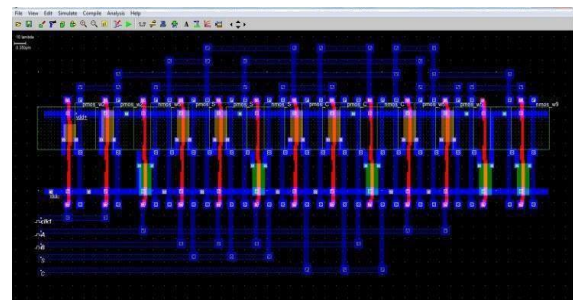
AVLS Technique

In AVLS technique, a combination of 2- N-MOS & 1-P-MOS are connected in parallel. So that a input clock pulse is applied at the P-MOS of circuit of AVLS circuit and the rest of the NMOS transistor is connected to the drain terminal. This approach is more valuable for reducing the power consumption also for the leakage current. . This AVLS control circuit is placed at voltage supply source terminal of the conventional half adder design in which supply is given through this control circuit. This control circuit at the upper end would bring down the supply voltage given to the whole circuit in order to reduce the power consumption of the conventional half adder design. When the input is varied corresponding output will be produced. It would reduce the leakage power by reducing the gate to source voltage and gate to drain voltage. This design would be responsible for very low power consumption.. The cell layout design of conventional half adder using AVLS technique is simulated by Microwind 3.1 software at 65 nm technology at Vdd = 1.0 V at Temp. 27° C .This design consumes less power, propagation delay, layout area, PDP as compared to Half Adder using CMOS, conventional and AVLG Technique. Layout cell, Simulation result, MOS characteristic and Variation of Power Vs Supply voltage is shown in Fig

Fig5.1: Circuit Diagram of Half Adder using AVLS Technique

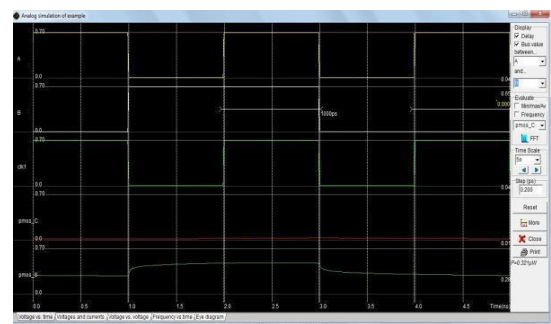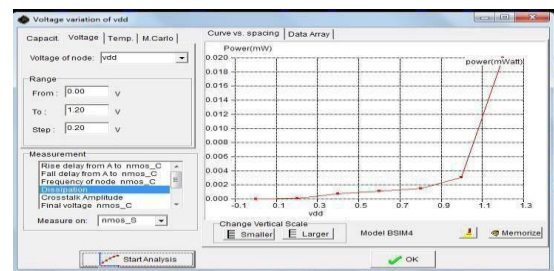Fig5.2: Layout cell of Half Adder using AVLS Technique

Fig5.3: Simulation Waveform of Half Adder using AVLS Technique

Fig5.4: Variation of Power Vs Supply voltage of Half Adder using AVLS Technique

RESULT

S. No.	Parameters	C-CMOS	Conventional	AVLG	AVLS
1.	Power Consumption (µw)	7.348	0.502	0.383	0.321
2.	Routed Wires	50	14	35	30
3.	Compiled Cells	16 / 16	6 / 6	9 / 9	9 / 9
4.	Layout Area (μm^2)	232	96	136	128
5.	Propagation Delay (ns)	0.70	0.67	0.65	0.54
6.	PDP (fj)	5.1436	0.33634	0.2485	0.17334
7.	No. of N-MOS and P- MOS transistors	8 , 8	3 , 3	5,4	4 ,5

CONCLUSIONS

From the above result we can see that the simulation result of this half adder using Adaptive Voltage Level technique shows that the power consumption is much reduced as compared to other techniques .Propagation delay, layout area, PDP also reduced as compared to other technique. It also requires less routed wires as compared to CMOS design. Various parameters have been calculated by using Micro wind 3.1 at 65 nm technology. Design of Half Adder using AVLS technique is more efficient in speed, layout area, power consumption, routed wires and propagation delay as compared to other technique. All the circuits operate at supply voltage of 1.2 V and temp. of 27°C.By using AVL technique size of circuit is also reduced. The application of AVL technique is used to reduce the power dissipation of digital circuits. By using AVL technique power can be saved up to 60 %.

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