International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 08 | Aug -2017 www.irjet.net p-ISSN: 2395-0072

A REVIEW OF LOW POWER NOVEL GATE DESIGN

Abirami.G[1] , Banumathi.T[2]

[1,2] *Assistant Professor, Prince Shri Venkateashwara Padmavathy Engineering College,Chennai.*

ABSTRACT: Reversible logic gate design is the novel gate for low power. Reversible logic is one of the promising technologies for low power in VLSI design. It is the technique to recover the output from the input itself. Number of input in the gate is equal to the number of outputs. The function of the logic gates purely depends on quantum cost function. Garbage output of the gates is ignored. Varieties of logic gates are available in the VLSI design. In this paper briefly discuss the different reversible logic gate functions. And also explains compare different adders with different gates.

Keywords: Quantum cost, Garbage output, Low power

1. INTRODUCTION

ADP parameter is one of the main concerns in VLSI design. Because it decides the circuit is best or not. Power consumption is one of the major issues in any type of VLSI circuit. Because every interconnection the power will dissipate and finally major loss the power in the output side. Because most of the digital logic circuits are easy and complex in nature. The novel reversible logic design allows the subsystem logic circuit with low power dissipation approximately zero power dissipation. The breakdown of power in the circuits relates with ever-increasing the attractiveness of portable electronic devices. All battery using components like Laptop, pagers, portable video players and cellular phones are the major source of power,

2. RELATED WORKS

kumar K et al. has been proposed the adders using reversible logic for efficient Implementation. Here the paper briefly explains the different types of adders were implemented with different reversible logic gates. The efficient adders are CSA, CSLA, RCA, CBA etc., are mostly used adders in the digital circuits. Design had done by both logic circuits named as reversible and irreversible logic gates. The performance of the adders is synthesized by using the Modelsim simulation environment.

Guan, Z. et al. were proposed the novel ALU design with the concept of depends on the reversible computing. Reversible logic gates are replaced the conventional gates. It functions perform the operation same as conventional ALU design. Proposed the method of design of efficient adder circuits based on the HNG and Prese gates. HNG and PFAG gates are used to design the lower hardware complexity and low power adder circuit.

3. REVERSIBLE LOGIC GATES

Reversible logic gate design is the most successful design for computer with the generation of heat. It generates less amount of heat inside the computer. Energy efficiency in the circuit can be achieved by reversible logic computing architecture. Normally energy efficiency is to change the speed of circuits and reduce the delay such as micro and nano electronic. To enhance the portability of devices can be achieved by reversible logic circuit. The component size of the circuit to decrease the size of the device and the outcomes is portable.

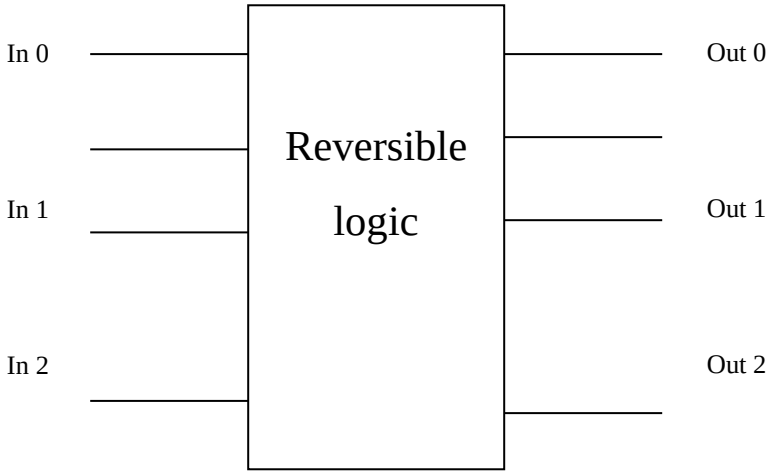

Fig. 1. Basic Reversible Logic Circuit

Feynman Gate

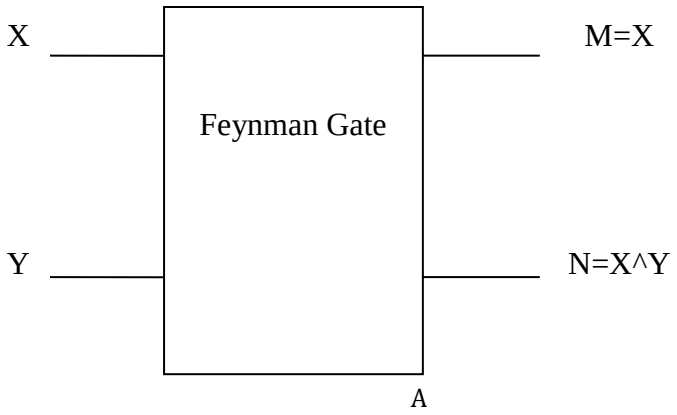

Fig. 2. Block of Feynman Gate

It consists of two inputs and two outputs. It is also called as Controlled NOT gate. The above block clearly shows the operation of the output. Quantum cost of the Feynman gate is one.

Fredkin Gate

Fredkin gate is a three input gate; it contains three inputs and three equal outputs. The name of the fredkin gate is controlled permutation gate. The basic gate function is shown in figure. 3.

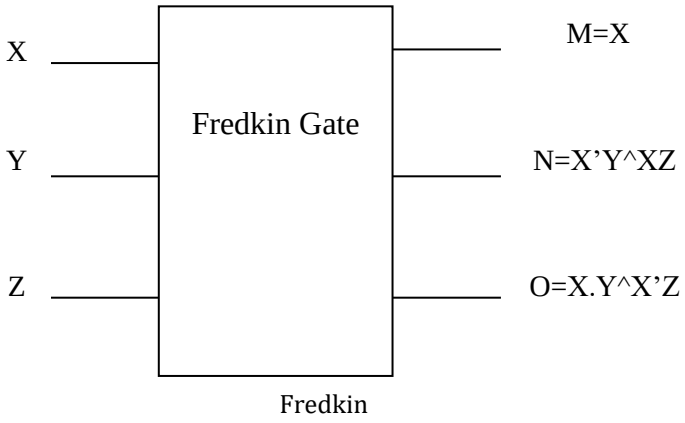

Fig. 3. Fredkin Gate

Peres Gate (PG)

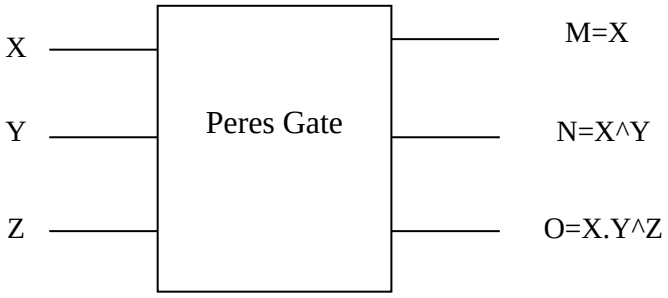

Fig. 4. Peres Gate

Peres gate is a three inputs and three output gates. Quantum cost of the peres gate is four. It is also constructed by using 1 Toffoli and 1 Feynman gate. It is also called as new Toffoli gate.

4. FULL ADDER USING PERES GATE

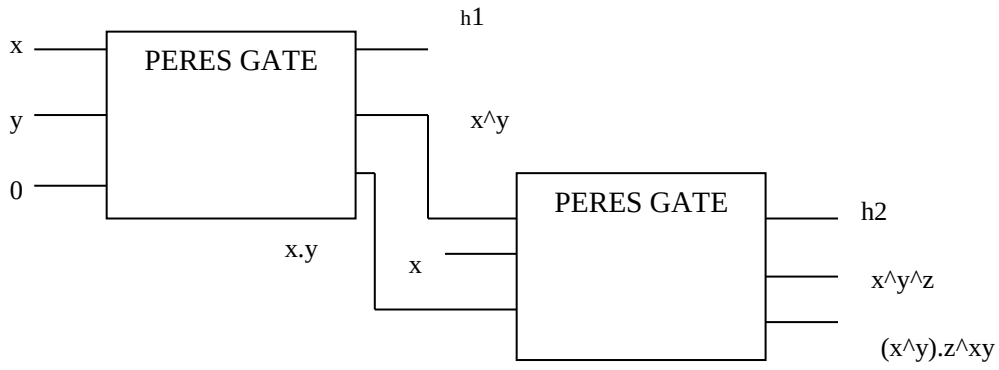

Fig. 5. Full Adder using Peres Gate

The above circuit is the full adder circuit which is constructed by using two peres gate. The two peres gates are cascaded to each other. The output of the first stage is forwarded to the input of the second peres gate. It reduces the power consumption compared to the normal full adder circuit.

5. RESULTS AND DISCUSSION

The adder circuit can be synthesized and evaluated using Xilinx simulation environment, and also compared with the traditional full adder circuit.

Table. 1. Comparison of Adder circuits

Parameters	Adder using Peres Gate	Adder using HNG
Quantum Cost	126	98
Garbage Output	30	32
Delay (ns)	7.74	7.78

6. CONCLUSION

In this paper, reversible logic gates using different adder circuits were designed and compared with some parameters to known the best adders. Delay and quantum cost should be reduced for proposed adder circuit.

REFERENCES

1. P.Vanusha, K.Amurtha Vally, "Low Power Computing Logic Gates design using Reversible logic", Vol. 3(10), pp. 123-129, Oct. 2014.
2. D. Maslov and G. W. Dueck, "Garbage in reversible design of multiple output functions," in Proc. 6th Int. Symp. Represent. Methodology Future Comput. Technol., pp. 162–170, Mar. 2003.
3. J. Lim, K. Kwon, and S. I. Chae, "Reversible energy recovery logic circuit without non-adiabatic energy loss," Electron. Lett., vol. 34(4), pp. 344–346, Feb. 1998.
4. Bangyuan, Chen Xunweiwu and Massoud Pedram, "Power Estimation in Binary CMOS Circuits Based on Multiple-Valued Logic", OPA (Overseas Publishers Association) N.V., 2000.