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Comparative Analysis of 11T and 16T and 28T Full Adder Based 4*4 Wallace Tree Multiplier Using Cadence 180nm Technology

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Abstract - *Multiplier is an important key component used for arithmetic operations in digital signal processor. Power utilization in multiplier is more when compared with adders and subtractors. So decreasing the power utilization of multiplier makes a digital signal processor more efficient. A Wallace tree multiplier is an efficient high speed multiplier that multiples two integers. Here 4*4 wallace tree multiplier is proposed with eight full adders and four half adders. Each full adder used in this design has only eleven(11T) transistors and half adder used in this design has only 10 Transistors which is less in number when compared with the conventional full adders. Due to this the power utilization of full adder block is reduced, such that power utilization of 4*4 wallace tree multiplier will be decreased. The proposed design this simulated using 180nm technology in cadence virtuoso tool and has achieved up to 50% power saving in comparison to the Wallace Tree Multiplier that has been designed using Conventional Full adder.*

***Key Words*: – Multiplier, Power Dissipation, Wallace Tree Multiplier, Full Adder, Cadence Virtuoso Tool.**

1. INTRODUCTION

One of the most important issues in VLSI Desig in power utilization. With the continuously increasing chips complexity and number of transistors in a chip, circuits power utilization is growing as well. Higher power utilization, raises chips temperature and directly effect battery life in portable designs as it causes more current to be withdrawn from the power supply. High temperature afflicts circuit operation and reliability so requires more complicated cooling and packing techniques. Full adder is the fundamental unit in circuits used for performing arithmetic operations such as multipliers, large adders therefore reducing power utilization in full adders, will reduce the overall power utilization of the whole system. Most of the VLSI applications.

Multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Multiplications are very expensive and slows the overall operation. Consider two binary numbers X and Y that are M and N bits wide, respectively. To introduce the multiplication operation, it is useful to express X and Y in the binary representation, the below fig.1 structure of Multiplier.

```
                A3 A2 A1 A0
              * B3 B2 B1 B0
        ---------------------
             S30 S20 S10 S00
          S31 S21 S11 S01
       S32 S22 S12 S02
    S33 S23 S13 S03
  ---------------------------------------------
  P7 P6 P5 P4  P3  P2  P1 P0
```

Figure 1: Structure of Multiplier

2. EXISTING WORK

2.1. Wallace Tree Multiplier

A Wallace tree is an efficient hardware implementation approach to design a digital circuit that multiplies two integers, and this multiplier is first introduced by an Australian Computer Scientist Chris Wallace in 1964. Wallace tree is known for their optimal computation time, when adding multiple operands to two outputs using carry-save adders. Other researchers also proved that Wallace tree and Dadda multipliers are the two well-known fast multipliers compared to array multiplier However, the Wallace tree guarantees the lowest overall delay. The Wallace tree has three steps to perform during the multiplication process: first, multiplying each bit of one of the arguments, by each bit of the other. Depending on the position of the multiplied bits, the wires carry different weights. Next, reduction of the number of partial products to two by layers of full and half adders will be performed and

lastly, group the wires into numbers, and add them with a carry look ahead adder.

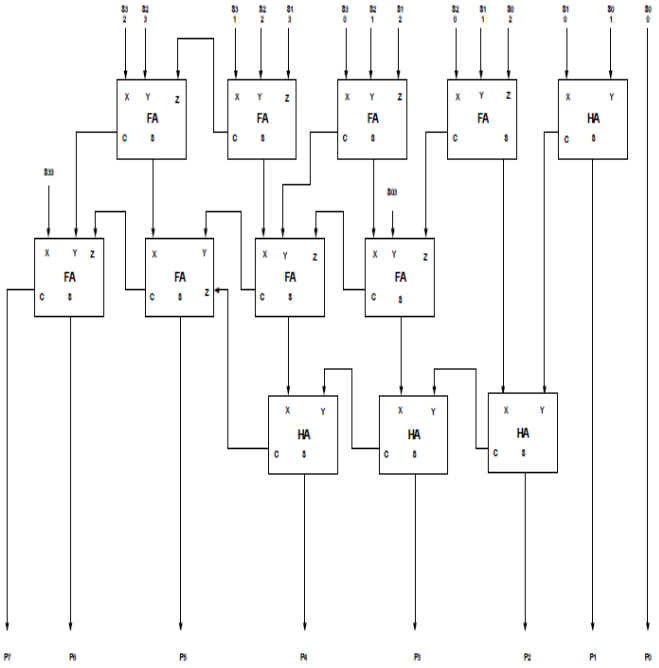

Figure 2: Block Diagram of Wallace Tree Multiplier

Applications of Wallace Tree Multiplier

- Multiplication is the basic arithmetic operation important in several microprocessors and digital signal processing applications.
- Digital Signal processing Systems require multipliers to implement DSP algorithms such as convolution and filtering where the multiplier lies directly within the critical path.
- Multipliers are the most frequently used devices in Image processing. Fast Fourier Transformation (FFT) is one of the important transforms often used in image processing. The computational process of FFT involves a large number of addition and multiplication operations.

2.2. Cadence EDA Tool Used For Design

Cadence EDA Tool:

- **Operating System:** Red Hat Linux 5.1.19.6
- **Design Tool:** Cadence IC6.1.6

Cadence Features: Cadence Virtuoso Schematic Editor: It provides numerous capabilities to facilitate fast and easy design entry, including design assistants that speed common tasks by as much as 5x.

Cadence Virtuoso Analog Design Environment:

Designed to help users create manufacturing-robust designs, it is the advanced design and simulation environment for the Virtuoso platform. It gives designers access to a new parasitic estimation and comparison flow and optimization algorithms that help to center designs better for yield improvement and advanced matching and sensitivity analyses. By supporting extensive exploration of multiple designs against their objective specifications, Virtuoso Analog Design Environment sets the standard in fast and accurate design verification.

2.3. 28T Full Adder Using 4*4 Wallace Tree Multiplier

Initially a 4*4 Wallace Tree multiplier is designed using a Conventional Full Adder. The Conventional Complementary Metal Oxide Semiconductor full adder consists of both pull up and pull down networks. It consists of 28 transistors. The schematic diagram of 28 transistor full adder is shown in Figure 3 and a 4*4 Wallace Tree Multiplier with this 28 transistor adder design is shown in Figure 4. The design is simulated using 180nm technology in cadence virtuoso Tool and resulted with high power consumption due to increased transistor count.

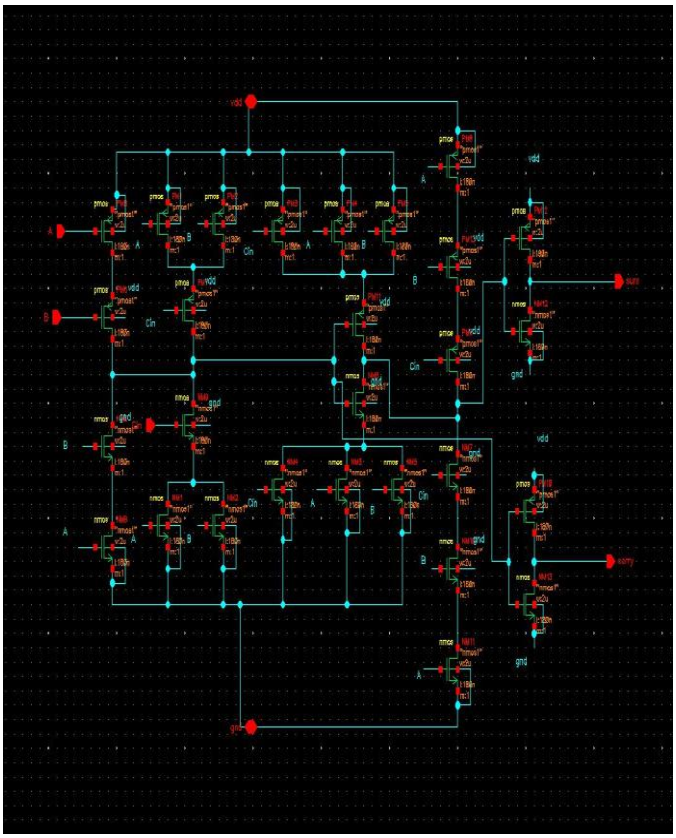

Figure 3: Schematic diagram of 28T Full Adder

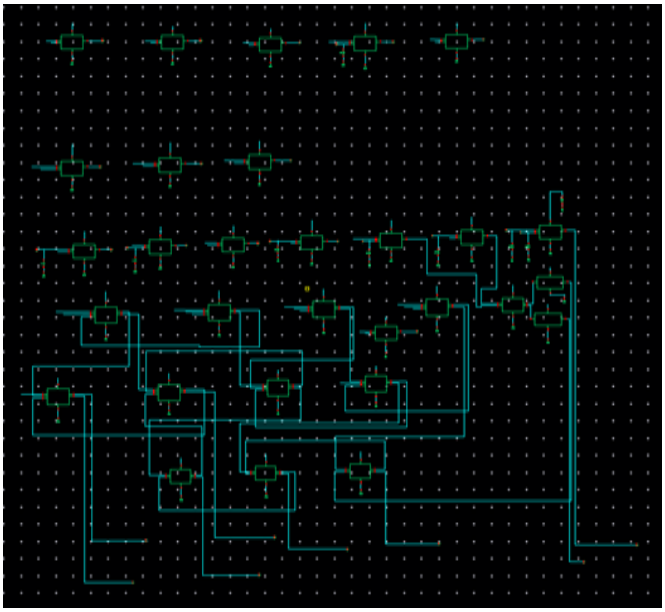

Figure 4: Schematic diagram 28T Full Adder based 4*4 Wallace Tree Multiplier

2.4. 16T Full Adder Using 4*4 Wallace Tree Multiplier

Later, a 16T full adder is proposed. This design is a combination of XOR-XNOR circuit and transmission gates. It do not provide enough driving power due to non full swing sum output and full swing carry output. Though it occupies less area, it consumes more power due to threshold voltage losses. But the power dissipation of 16T adder is much less than that of the conventional adder. The schematic diagram of 16T full adder is shown in Figure 5 and 4*4 Wallace Tree Multiplier with 16T full adder is shown in Figure 6. The design is simulated using 180nm technology in cadence virtuoso Tool.

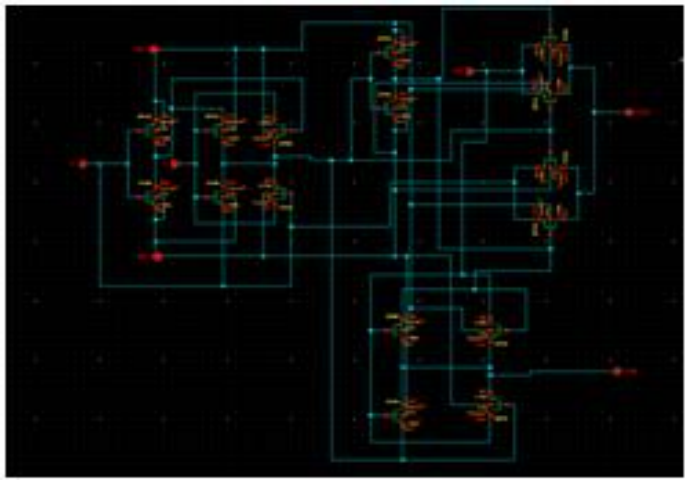

Figure 5: Schematic diagram of 16T Full Adder

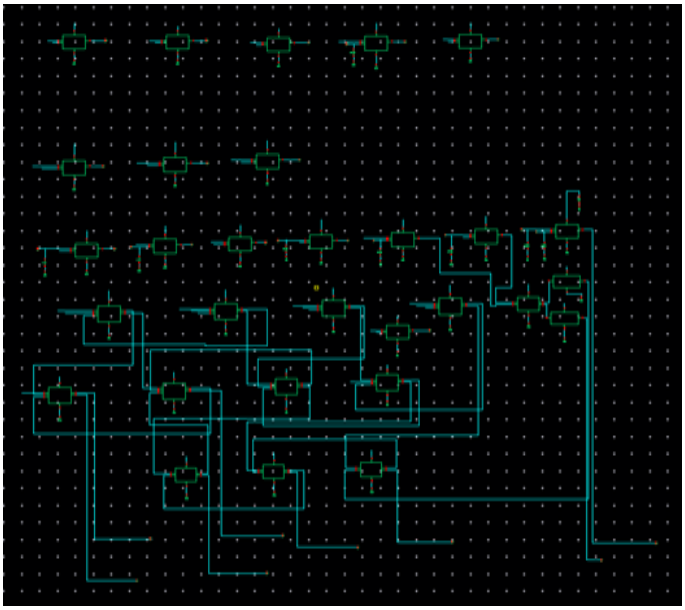

Figure 6: Schematic diagram 16T Full Adder based 4*4 Wallace Tree Multiplier

3. PROPOSED WORK

This proposed work presents the design of low power 4*4 Wallace Tree multiplier based on 11T full adders. Based on the comparison of the existing adders, the 11T full adder is chosen for the design due to its low power consumption. The 11T full adder consists only one 4T XOR gate. This full adder has overcome the voltage degradation occurring due to threshold drop. This problem has overcome by increasing the aspect ratio(W/L) by making the length as constant and increasing the width. Here the 11T Full Adder is designed using 180nm technology in cadence Tool. The schematic diagram of 11T full adder is shown in Figure 7. Finally it is proved that reducing the transistor count decreases the power consumption of a circuit.

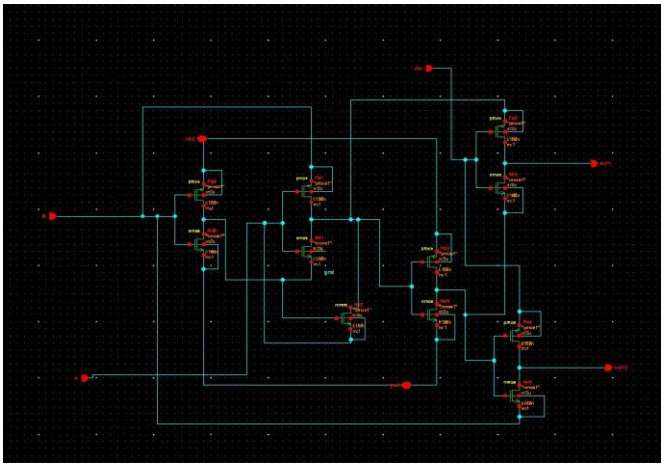

Figure 7: Schematic diagram of 11T Full Adder

Though different multipliers exist, here a Wallace Tree Multiplier is chosen for design due to its high performance and speed. Now a 4*4 Wallace Tree Multiplier is designed with the above simulated 11T full adder using 180nm technology in cadence virtuoso Tool. The Wallace Tree Multiplier designed here consists of 11 transistor full adder. Here it is shown that reducing the transistor count, reduces the power consumption of a CMOS circuit. The schematic diagram of 4*4 Wallace Tree Multiplier based on 11T full adder is shown in Figure 8.

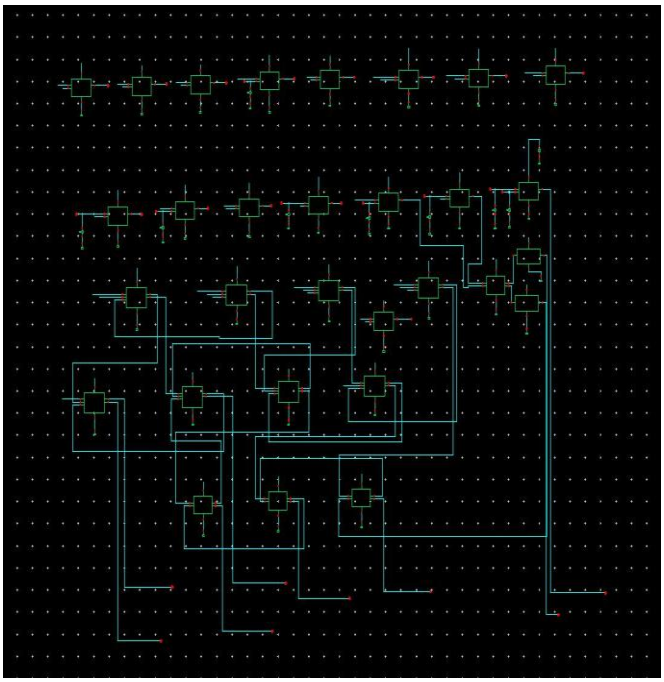

Figure 8: Schematic diagram 11T Full Adder based 4*4 wallace Tree Multiplier

4. RESULTS

A Wallace Tree Multiplier based on 11T full adder has been proposed. From the result, the proposed design consumes less power when compared to the conventional full adder based Wallace Tree Multiplier. It saves up to 50% of power compared to Wallace Tree Multiplier based on conventional full adder. Using the Wallace Tree Multiplier based on 11T full adder in a Digital Signal Processor makes the system more efficient. These designs were simulated using 180nm technology in Cadence virtuoso Tool and the output waveforms.

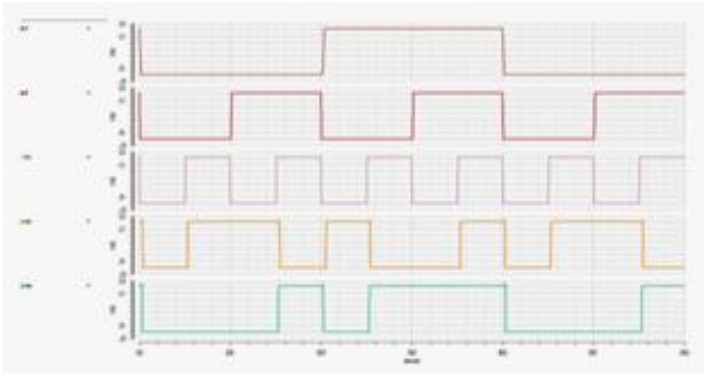

Figure 9: Simulated Waveforms of 11T Full Adder

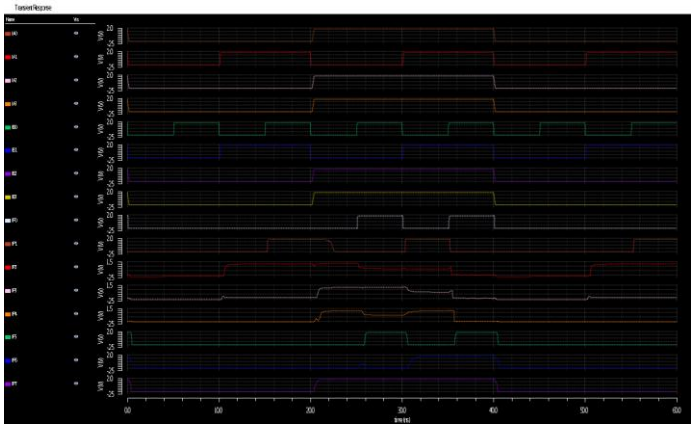

Figure 10**:** Simulated Waveform 11T Full Adder based4*4 Wallace Tree Multiplier

5. COMPARSION

Table1 shows the comparative analysis between the conventional full adder, 16T full adder and 11T full adder. This analysis shows that 11T full adder has less transistor count and power consumption. Table 2 shows the comparative analysis between the Wallace tree multiplier based on conventional full adder, 16T full adder and 11T full adder. From the analysis it shows Wallace tree multiplier with 11T full adder is best suited for the low power applications as it is effective in all cases such as transistor count and power consumption.

Table 1: Comparison Table for Full Adders

	28T Full Adder	16T Full Adder	11T Full Adder
Transistor count	28	16	11
Power consumption	35.12µw	17.53µw	8.42µw

Table 2: Comparison Table for Wallace Tree Multiplier

	Wallace Multiplier based on 28T Full Adder	Wallace Multiplier based on 16T Full Adder	Wallace Multiplier based on 11T Full Adder
Transistor count	264	168	128
Power Consumption	278.7 µw	134.7µw	78.492µw

6. CONCLUSION

In this paper, a 4*4 Wallace Tree Multiplier based on 11T full adder was designed using 180nm technology in cadence virtuoso Tool. From the results and comparison, it has been proved that the Wallace Tree Multiplier based on 11T full adder has less power consumption. It consumes only 50% of the power when compared to other conventional full adder based Wallace Tree Multipliers. The Wallace Tree Multiplier based on 11T full adder is worth enough to make a Digital Signal Processor performance efficient.

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