International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 07 | July -2017 www.irjet.net p-ISSN: 2395-0072

An Extensive Literature Review on Reversible Arithmetic and Logical Unit

Sanjay Kumar[1], Dr. Harjinder Singh[2]

[1]M.Tech. Scholar, Department of Electronics and Communication Engineering, Punjabi University Patiala
[2]Assistant Professor, Department of Electronics and Communication Engineering, Punjabi University Patiala

---

Abstract - *To reduce the power dissipation which is the main requirement in low power digital design Reversible logic is used . It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. Reversible logic is gaining wide importance as a logic design style for modern nanotechnology and quantum computing with minimal heat generation because the existing irreversible designs are reaching their physical limits. The use of reversible logic therefore, provide the improvement in computer architecture and arithmetic logical unit designs. An important block in the microprocessors is Arithmetic and Logical Unit (ALU). This paper provides the review on Reversible Arithmetic and Logic Unit.*

Keywords: Reversible logic gates.

1. INTRODUCTION

Reversible Logic Synthesis has been quite actively pursued over the last decades, mainly due to the fact of magical power reduction using reversible logic. According to Moore's law the numbers of transistors will double every one and half year. Thus, energy conservative devices are the need of the day. Heat dissipation can be minimized with manufacturing optimization methods. Landauer's Principle [10], shows that a circuit which is logically reversible will, in principle, be thermodynamically reversible as well and investigated that for every bit loss, KT * log 2 joules of heat is generated. As this amount of heat is too small today, Zhirnov shown that it is very difficult to remove the heat as the numbers of CMOS (Complementary metal–oxide–semiconductor) devices increases, which has made research in this area an important topic.

A circuit in which at end there is no data lost is called reversible, hence provide the solution to the problem discussed by Landauer and this may provide a great achievement for the semiconductor world. Bennett [17] showed that zero heat dissipation would only be possible, if a circuit consists of only reversible gates. The main application of reversible logic is Quantum Computing. A quantum computer will be viewed as a quantum network (or a family of quantum networks) which consist of quantum logic gates and each gate performing an elementary unitary operation on one, two or more than two-state quantum systems is called qubits. Quantum networks must be built from reversible logical components.

2. BASIC REVERSIBLE LOGIC GATES

In the existing literature, there are several numbers of reversible gates such as the Feynman gate and Fredkin gate. The quantum cost of any circuit depends on number of 1x1 and 2x2 reversible gates needed to design that circuit. The quantum cost of reversible gate with 1x1 and 2x2 configurations are considered as unity. The 1x1 NOT gate and 2x2 reversible gates are use to realize the 3x3 reversible gates generally. The 2x2 reversible gates are Controlled-V and Controlled-V+ (V is a square-root of NOT gate and V+ is its Hermitian). The Feynman gate also known as Controlled -NOT gate (CNOT).

2.1 NOT Gate

A NOT gate is 1x1 gate represented as shown in Fig - 1. Since has 1x1 configuration gate, its quantum cost is unity.

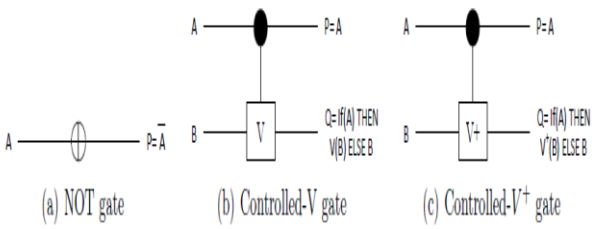

Fig - 1 Not Gate

Not gate as shown above can be used as control gate and this gate have zero quantum costs as this have only one

input and one output so same in irreversible and reversible.

2.2 Fredkin Gate

Fredkin gate is a 3x3 reversible logic gate with three inputs and three outputs. The Fig - 2 shows the block diagram of a Fredkin gate. Fredkin gate, maps the inputs A, B, and C to outputs as P=A, Q =$\bar{A}$B + AC, and R = AB + $\bar{A}$C respectively.

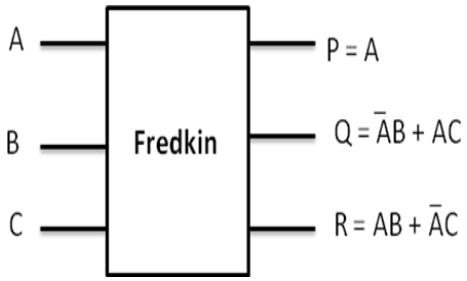

Fig - 2 Fredkin gate

A Fredkin gate can work as 2:1 MUX, as it is able to swap its other two inputs depending on the value of its first input. Referring the Fig - 2, the first input A works as a controlling input, while the both B and C work as controlled inputs. Thus, when A=1 the inputs B and C will give outputs as Q=C and R=B and thus input gets swapped. If A=0 the inputs B and C will give outputs as Q=B and R=C.

2.3 Feynman Gate (CNOT Gate)

The Feynman gate (FG) or the controlled-NOT gate (CNOT) is a 2x2 reversible gate. The inputs A and B are mapped to outputs as P=A and Q=A⊕B respectively. Here, A is the controlling input and B is the controlled input whereas P and Q are the two outputs. Since the Feynman gate is a 2x2 reversible gate, it has a quantum cost of 1. Fig - 3(a) and 3(b) shows the block diagram and the quantum representation of the Feynman gate. Each output in reversible logic can be used only once so fan out is not allowed. Feynman gate is helpful in this regard as same output can be generated on both output terminals at same time, thus avoiding the fan-out problem as shown in Fig - 3(c). It can also be used for generating the complement of a given input signal as shown in Fig - 3(d**).**

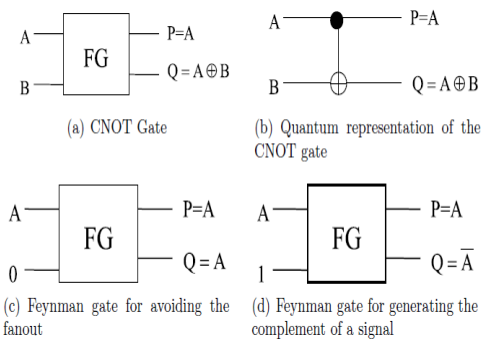

Fig - 3 CNOT gate, its quantum implementation and its useful properties

2.4 Toffoli Gate

The Toffoli gate (TG) is a 3x3 reversible logic gate with three inputs and three outputs. The input of Toffoli gate as A, B and C are mapped to P = A, Q = B and R = ((A B) ⊕ C) respectively.

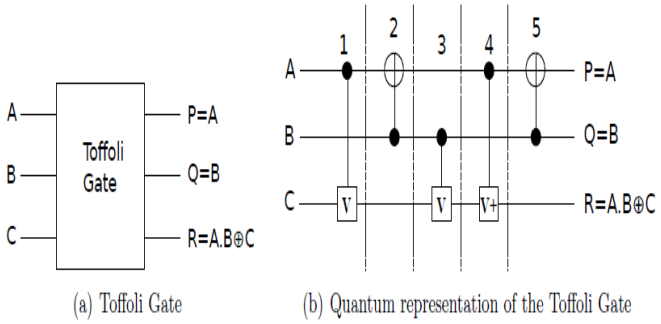

Fig - 4 Toffoli Gate and its quantum implementation

Fig - 4(a) shows the block diagram of a Toffoli gate. A Toffoli gate has a quantum cost of 5 as it can be implemented using 2V gates, 1V + gate and 2 CNOT gates. Fig - 4(b) shows the quantum implementation of a Toffoli gate.

2.5 HNG Gate

The HNG gate is a 4x4 reversible logic gate with three inputs and three outputs as shown in Fig - 5. The inputs of HNG gate as A, B, C and D are mapped to P = A, Q = B, R = (A ⊕B⊕ C) and S= (A⊕B) C⊕AB⊕D respectively. The reversible HNG gate can perform operation as a reversible full adder. If the input vector IV = (A, B, Cin, 0), then the output vector becomes OV = (P= A, Q= Cin, R= Sum, S= Cout).

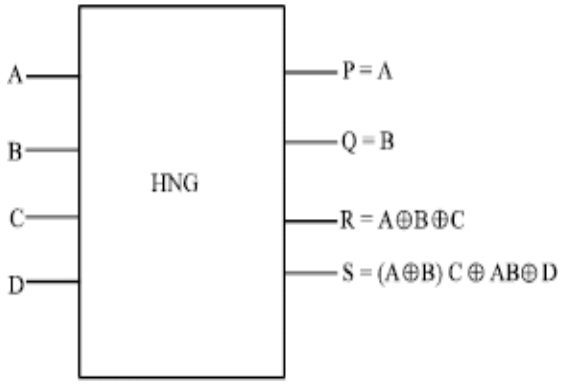

Fig - 5 HNG Gate

3. RALATED ISSUES AND WORK DONE

- **Priyal Grover and Hemant Verma [1]** present paper "Design, Layout and Simulation of 8 Bit Arithmetic and Logic Unit (2015)" in International Journal of Electrical and Electronics Engineers. In this presented work, an 8-bit ALU is designed, implemented and simulated using the Electric CAD and SPICE software. The proposed design is an 8-bit ALU that can perform: A AND B, A + B (addition), A OR B and A - B (subtraction) and all possible arithmetic and Logical operations. Physical design of every sub module is carried out using C5 process 300 nm process technologies. The process technology used here is C5 process provided by MOSIS. This ALU has design flexibility and speed is less.
- **Shefali Mamtaj et.al. [2]** present paper "An Optimized Realization of ALU by Using Control Unit of Reversible gates (2014)" in International journal of Advanced Research in Comp. Science and Software Engineering. A control unit is proposed in this paper which consists of reversible gates. This control unit is more efficient with respect to the existing control unit. This paper also represents an optimized realization of arithmetic logic unit by using the proposed control unit and DKFG reversible gate. This ALU has less quantum cost and garbage outputs in Arithmetic and Control Unit is approximately equal to conventional circuit.
- **Ajay Kumar Sharma and Anshul Jain [3]** present paper "Designing of Low Power Low Area Arithmetic and Logic Unit (2014)" in International Journal of Innovative Research in Computer and Communication Engineering. This paper describes the design technique for low power, low area Arithmetic and logic unit design. In this paper number of gate and power are reduced .The area of design also reduced. So this ALU has low power, low area and design complexity.
- **Chetan Kumar et.al. [4]** Present paper "Implementation of 16 bit Arithmetic Logic Unit using Toffoli Reversible logic gate (2014)" in International Journal of Innovative Science, Engineering & Technology (JISET). In this paper a traditional ALU is realized using AND, OR reversible logic gates. The power dissipation in terms of loss of information bits is reduced significantly when logic gates were replaced by reversible gates. The proposed reversible 16-bit ALU reduces the loss of power reusing the bits. Simulation of these circuits is done by Mentor graphics tools and language used for programming is very high speed hardware integrated circuit hardware descriptive language, Verilog. This ALU is made up of Toffoli Gate only and observed low power consumption on simulation.
- **Vijay G.Royet.al. [5]** present paper "Low Power 8 Bit quantum ALU Implementation Using Reversible Logic Structure (2014)" in International Journal of Science and Research (IJSR). In this work, novel programmable reversible logic gates are used in the design of a reversible Arithmetic Logic Unit. Using 1 bit ALU, an 8 bit ALU has been designed and verified. The proposed 8 bit ALU is also compared with the existing 8 bit ALU with reference to few important parameters such as propagation delay and power dissipation. The major advantage of proposed ALU is the increased number of operations with certain number of select inputs with low power consumption. This ALU can be utilized in low power VLSI design, nanotechnology, quantum computing and optical computing. This ALU has more operation and slow speed.
- **Akanksha Dixit and Vinod Kapse [6]** present paper "Arithmetic& Logic Unit (ALU) Design using Reversible Control Unit (2012)" in International Journal of Engineering and Innovative Technology (IJEIT). The author proposed the design of ALU based on a Reversible low power control unit for arithmetic

& logic operations. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output DPeres gates. In this paper a novel design of Arithmetic & Logical Unit is presented using Reversible control unit. This Reversible ALU has been modeled and verified using Verilog and Quartus II 5.0 simulator. Comparative results are presented in terms of number of constant inputs, number of gates, Quantum cost and number of garbage outputs. This ALU has less constant input and more quantum cost.

- **Zhijin Guan et.al. [7]** present paper "An Arithmetic Logic Unit Design Based on Reversible Logic Gates (2011)" in IEEE. This paper proposed the design of Arithmetic and Logical Unit (ALU) based on reversible logic gates as logic components. By using reversible logic gates instead of using traditional logic gates such as AND gates and OR gates, a reversible ALU whose function is the same as the traditional ALU is constructed. The presented reversible ALU reduces power loss by reusing the logic information bits logically. The reversible ALU in this paper has great significance to the realization of the more complex and systematic reversible circuits This ALU has more operational output and makes use of C++ language.
- **Avinash G. Keskar and Vishal R. Satpute [8]** present paper "Design of Eight Bit Novel Reversible Arithmetic and Logic Unit (2011)" in IEEE. This paper covers various aspects about reversible computing and reversible logic gates. Furthermore in this paper we have tried to design a reversible implementation of eight bit arithmetic and logic unit, optimal in terms of number of gates used and number of garbage outputs produced. The proposed circuit can be used in the designing of large reversible systems which is the necessary requirement of quantum computers. We have tried to design the reversible logic implementation of ALU optimal in terms of number of gates and garbage outputs produced. This ALU has more operation and complex in design.
- **Y.Syamala and A. V. N. Tilak [9]** present paper "Reversible Arithmetic Logic Unit (2011)" in IEEE. In this paper, the design of a reversible Arithmetic Logic Unit (ALU) is presented making use of multiplexer unit as well as control signals. ALU is one of the most important components of CPU that can be part of a programmable reversible computing device such as a quantum computer. In multiplexer based ALU the operations are performed depending on the selection line. The control unit based ALU is developed with 9n elementary reversible gates for four basic arithmetic logical operations on two n-bit operands. The series of operations are performed on the same line depending on control signals, instead of selecting the desired result by a multiplexer. The later design is found to be advantageous over the former in terms of number of garbage outputs and constant inputs produced. This ALU has better efficiency and more quantum cost.
- **R. Landauer [10]** present paper "Irreversibility and Heat Generation in the Computational Process (1961)" in IBM Journal of Research and Development. R. Landauer's showed, the amount of energy (heat) dissipated for every irreversible bit operation is given by KT ln2, where K is the Boltzmann's constant (1.3807×10-23 JK-1) and T is the operating temperature. At room temperature (300 K), KT *ln2 becomes 2.8×10-21 J, which is small but not negligible. He also showed that only the logically irreversible steps in a computation carry an unavoidable energy penalty.
- **C.H. Bennett [11]** present paper "Notes on the History of Reversible Computation (1998)" in IBM Journal of Research and Development. Bennett showed that kT*ln2 energy dissipation would not occur, if operations are performed using reversible gates, since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation.
- **Monika Rangari et.al.[12]** present paper "Design of Reversible Logic ALU using Reversible logic gates with Low Delay Profile (2015)" in International Journal of Advanced Research in Computer and Communication Engineering. This paper proposed the design of 1-bit reversible ALU using reversible logic gates. The analysis of proposed ALU is done on FPGA SPARTAN6 device. The proposed design is compared in terms of garbage outputs, quantum cost and propagation delay. On the basis of 1- bit

reversible ALU architecture the 4-bit reversible ALU is also designed.

- **Ravi Raj Singh et.al.[13]** present paper "Efficient Design of Arithmetic Logic Unit using Reversible Logic Gates (2014)" in International Journal of Advanced Research in Computer Engineering & Technology (IJARCET). This paper proposed the design of ALU which has better performance in terms of transistor cost and quantum cost. The carry save adder block does not involve the propagation of carry bits and proposed ALU is realized by using that. The proposed work leads to an improvement in terms of gate count and quantum cost, as compared to earlier works in reversible ALU designs. The simulation and verification of the ALU is done using Revkit tools, Xilinx and Cadence.
- **Darshan H et.al.[14]** present paper "Design and Synthesis of 8 Bit Reversible Arithmetic & Logical Unit (ALU) (2015)" in ITSI Transactions on Electrical and Electronics Engineering (ITSI-TEEE). This paper presents the design of 8 bits reversible ALU which perform numbers of arithmetic and logical operations. The paper proposes 2 types of reversible ALU design. The design-1 ALU uses Peres Full Adder Gate (PFAG) and the design-2 ALU uses HNG gate as an adder circuit. Both the proposed designs are compared in terms of quantum cost, garbage output and gate count. The proposed 2 designs of ALU are compared with a conventional 8 bit ALU in terms of propagation delay and power dissipation. The final result shows that the ALU design-2 is better than to propose ALU design-1 and the conventional ALU.
- **Khushboo Ahirwar et.al.[15]** present paper "FPGA Implementation ALU Based on Reversible Logic (2014)" in International Journal of Engineering Research & Technology (IJERT). The proposed design makes use of two novel 4*4 reversible logic gates (MRG and PAOG) with minimal delay, and may be configured to produce a variety of logical calculations based on programmable select input lines on fixed output lines. The proposed ALU design is verified and analyzed over the existing ALU design. The proposed design is implemented for SPARTEN3 FPGA board and is synthesized using Xilinx ISE software and simulated using MODEL SIM 6.5b.

4. PROPOSED METHODOLOGY

The irreversible Arithmetic and Logic Unit (ALU) consume significant amount of power due to loss of bits during operation. Due to this loss of bits heating problem becomes unavoidable in many situations. To improve the power performance of irreversible Arithmetic and Logic Unit (ALU), we make use of reversible Arithmetic and Logic Unit (ALU). So in this research work we have studied various reversible logic gates for designing proposed reversible Arithmetic and Logic Unit (ALU).

5. CONCLUSION AND FUTURE SCOPE

The new reversible Arithmetic and Logic Unit **(**ALU) designs are advantageous to irreversible Arithmetic and Logic Unit **(**ALU) and favor low power dissipation and also consume less area which is desirable for realization of a reversible central processing unit. The results of the research can be exploited very effectively in quantum computing and low power design. The future scope of this research includes the applicability of Moore's law in the next few decades through the quantum computing using reversible logic. This reversible Arithmetic and Logic Unit **(**ALU) can be used in applications such as quantum computing, nanotechnology, optical computing, low power VLSI designs etc.

REFERENCES

[1] Priyal Grover and Hemant Verma, "Design, Layout and Simulation of 8 bit Arithmetic and Logical Unit" International Journal of Electrical and Electronics Engineers (IEEE),Vol. 07, Issue 02, July- December 2015.

[2] Shefali Mamtaj, Biswajit Das, Anurima Rahama "An Optimized Realization of ALU for 12 Operation by using a Control Unit of Reversible Gates", International Journal of Advanced Research in Computer Science and Software Engineering (IJARCSSE), Vol. 04, Issue 01, January 2014.

[3] Ajay Kumar Sharma and Anshul Jain, "Design of Low Power Low Area Arithmetic and Logical Unit" International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE), Vol. 02, Issue 12, December 2014.

[4] Chetan Kumar, Dr. Rekha.K .R and Dr. Natraj K .R, "Implementation of 16 bit Arithmetic and Logical Unit using Toffoli Reversible Logic Gate" International Journal

of Innovative Science, Engineering and Technology (IJISET), Vol. 01, Issue 06, August 2014.

[5] Vijay G.Roy, P.R.Indurkar and D.M.Khatri, "Low Power 8 bit Quantum ALU Implementation using Reversible Logic Structure", International Journal of Science and Research (IJSR), Vol. 03, Issue 07, july 2014.

[6] Akanksha Dixit and Vinod Kapse, "Arithmetic and Logical Unit Design using Reversible Control Unit",International Journal of Engineering and Innovative Technology (IJEIT), Vol. 01, Issue 06, June 2012.

[7] Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang and Lihui Ni, "An Arithmetic and Logical Unit Design based on Reversible Logic Gates", International Journal of Electrical and Electronics Engineers (IEEE), 2011.

[8] Avinash G. Keskar and Vishal R. Satpute, "Design of 8 bit Novel Reversible Arithmetic and Logical Unit" International Journal of Electrical and Electronics Engineers (IEEE),2011.

[9] Y.Syamala and A. V. N. Tilak, "Reversible Arithmetic and Logical Unit" International Journal of Electrical and Electronics Engineers (IEEE), 2011.

[10] R.Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, Vol. 05, 1961.

[11] C.H. Bennett, "Notes on the History of Reversible Computation", IBM Journal of Research and Development, Vol. 32, 1998.

[12] Monika Rangari, Prof. Richa Saraswat and Dr. Rita Jain, "Design of Reversible Logic ALU using Reversible logic gates with Low Delay Profile" International Journal of Advanced Research in Computer and Communication Engineering, Vol. 04, Issue 4, April 2015.

[13] Ravi Raj Singh, Sapna Upadhyay, Saranya S, Soumya, Jagannath KB and Hariprasad SA, "Efficient Design of Arithmetic and Logical Unit using Reversible Logic Gates" International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), Vol. 3, Issue 4, April 2014.

[14] Darshan H, Mohanraj R, Kavya H B, Monisha U K and Saroja Maralabhavi, "Design and Synthesis of 8 Bit Reversible Arithmetic & Logical Unit (ALU)" ITSI Transactions on Electrical and Electronics Engineering (ITSI-TEEE), Vol. 3, Issue 03, 2015.

[15] Khushboo Ahirwar, Sachin Bandewar and Anand Kumar Singh, "FPGA Implementation ALU Based on Reversible Logic" International Journal of Engineering Research & Technology (IJERT), Vol. 3 Issue 1, January 2014.

[16] Pradeep singla and Naveen Kr. Malik, " A Cost Effective Design of Reversible programmable logic array" International Journal Of Computer Application, Vol. 41, March 2012.

[17] C.H. Bennett, "Logical Reversibility of Computation" IBM J.Research and Development, November 1973.