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Implementation and validation of SAE J1850 (VPW) protocol solution for diagnosis application

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Abstract - *This project is about the diagnosis of vehicle. The aim of this project is to interchange digital information between on board emission related ECU of road vehicles and personal computer through SAE OBDII tool. This communication established in order to facilitate inspection, test diagnostic. Repairer or owner can access vehicle parameters for diagnosis purpose. To communicate with subsystem of vehicle like ECU, J1850 (VPW) protocol is used. This project consist host (personal computer), OBD (On Board Diagnosis) device, J1962 connector, USB. OBD device consist of hardware of J1850 (VPW) protocol. Host establishes communication with ECU thorough J1850 (VPW) protocol. To implement J1850 (VPW) protocol Freescale processor is used. Processor consists of BDLC (Byte Data Link Controller). The BDLC module is a serial communication module which allows the user to send and receive messages across a Society of Automotive Engineers (SAE) J1850 serial communication network. Host sends the request to obtain parameter from ECU. This request is passed through USB to J1850 device. J1850 device communicate with ECU and obtain response. In this communication timing constrains are very important. To deal with real time environment it is necessary to choose RTOS (Real time Operating system). In this project Vxworks RTOS is used.*

Key Words: **OBD (On Board Diagnosis), BDLC (Byte Data Link Controller), J1850 (VPW), Vxworks RTOS, Diagnostic protocol**

1. INTRODUCTION

Now a day's one of the most important world problems is to save our planet, keep our planet clean and reduce the emissions caused by vehicles. There is one solution to reduce these emissions is development of good testing system of vehicles. On Board Diagnostic (OBD) is a system which introduced by the "California Air Resources Board". OBD systems are incorporated in computers to monitor vehicles components which may affect emissions when they are malfunctioning. OBD systems provide access to users to monitor various key components of vehicle. These systems always detect malfunction of components and inform before owner or technician aware of this problems.

There is requirement to interchange digital information between vehicle key components such as ECU (Engine Control Unit) and OBD tool. This communication between vehicles components and OBD is required for diagnosis of systems. On board diagnosis is automotive term which is referred as vehicle self-diagnosis and report to owner when there is a problem. When there is problem occurs which may lead to increase emissions then OBD system send warning to alert driver that there is need of repair the vehicle systems.

To implement OBD system there are several protocols to communicate OBD tool with vehicle components. One of them is SAE J1850 (VPW) protocol. Attributes of the J1850 (VPW) protocol include an open architecture, low cost, master-less, single-level bus topology. In automobiles there is too much harness so there is radiations problem which affect the signals. The reason behind choosing of SAE J1850 (VPW) is it offers one of the lowest radiated emissions encoding schemes possible due to the minimization of bus transitions per data bit. Some key attribute of VPW are its ability to compensate for clock mismatch and ground offsets, it offers the low number of transitions per bit and it is suited for arbitration as well.

2. Introduction to J1850 (VPW)

SAE J1850 standards are used in on board and off-board vehicle. It is open architecture, single level, low cost and master-less protocol. SAE J1850 protocol can be implemented by two methods. First is Pulse Width Modulation (PWM) with 41.6 kbps signal rate and is Variable Pulse Width (VPW) with 10.4 kbps signal rate. It is used for data sharing and diagnosis in vehicles.

2.1 Variable Pulse Width (VPW)

VPW modulation is an encoding scheme which is developed by General Motors. VPW protocol has10.4 kbps signal rate. It has several advantages over PWM scheme. Automotive environment demands for low radiated emissions. VPW encoding scheme offers low radiated emissions. It is possible to reduce emissions due to minimization of transitions per data bit. VPW require only one transition for each transmitted bit where PWM

require two transitions per transmitted bit. VPW obtain one transition per bit through unique definitions of data bits. High bus voltage is dominant on bus.
Dominant symbols

- Active bus: Long dominates short pulses
- Passive bus: Short dominates long pulses

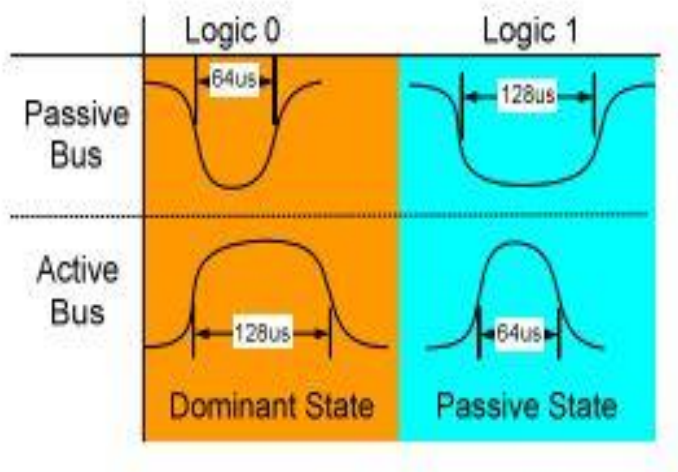

Fig- 1: Dominant state and passive state symbols

2.2 Characteristics of Variable Pulse Width (VPW):

1. Baud rate is 10.4 kbps
2. 40 m max length (wire) can be used.
3. 32 max nodes (no. of ECU) can be added on bus.
4. Single wire voltage signalling is used.
5. High bus voltage is nominally 7v, Range 4.5v to 20v
6. Low bus voltage is nominally <3.5v, Range 3.5v to 0v.
7. High voltage is dominant.
8. Zero symbol dominant is dominant.
9. Carrier Sense Multiple Access with Non-Destructive Arbitration (CSMA/NDA) is used to avoid collision.

2.3 SAE J1850 (VPW) Message Frame

IFS	SOF	Header (8/24)	Data	CRC (8)	EOD	NB	IFR data	CRC (8)	EOF	IFS

Fig -2: SAE J1850 (VPW) message frame

According to SAE J1850 (VPW) each message is 101 bit times or 12 bytes (excluding SOF, EOF, EOD and NB).

Frame consists of following fields:

- **SOF** (Start of frame symbol)-All messages transmitted onto J1850 (VPW) starts with long active SOF symbol. It is 200us in length.
- **Header**-It is one byte or three bytes in length. It consist of information like header type, priority, addressing.
- **Data**-It consist information represented in "ones" and "zeros".
- **CRC** (Cyclic Redundancy Check)-It is used by receivers for each message to determine any error is occurred during transmission.
- **EOD** (End of Data Symbol)-It is long passive symbol which indicate transmission of data by originator is completed.
- **IFR** (In Frame Response Bytes)-An IFR used by remote receiving nodes to actively acknowledge a transmission.
- **EOF** (End of Frame)-It is passive period symbol used to signify end of frame which allows synchronization between nodes during continuous message transmission.
- **NB** (Normalization Bit)- The NB provides an active separation between the passive EOD symbol and the first data bit of the IFR response.

3. Proposed System

The main aim of this system is to interchange data between vehicle component e.g. ECU (Electronic Control Unit) and personal computer (Host). This communication is done through J1850 (VPW) protocol with 10.4 kbps data rate.

3.1 Project Flow

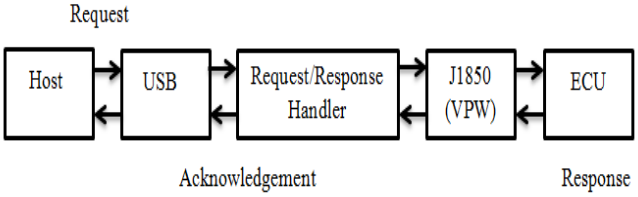

Fig- 3: Project flow

Whenever host want to communicate with ECU, host send request to USB. This request is in the form of frame .Frame consist of module ID, frame type, command code and data. This frame is sending request handler task which check frame and according to it choose protocol. When request is for J1850 (VPW) then it forward request to ECU and obtain response. The whole implementation is divided into following two parts,

- Hardware design to implement J1850 (VPW)
- Firmware design to establish communication with host.

3.2 System Hardware design

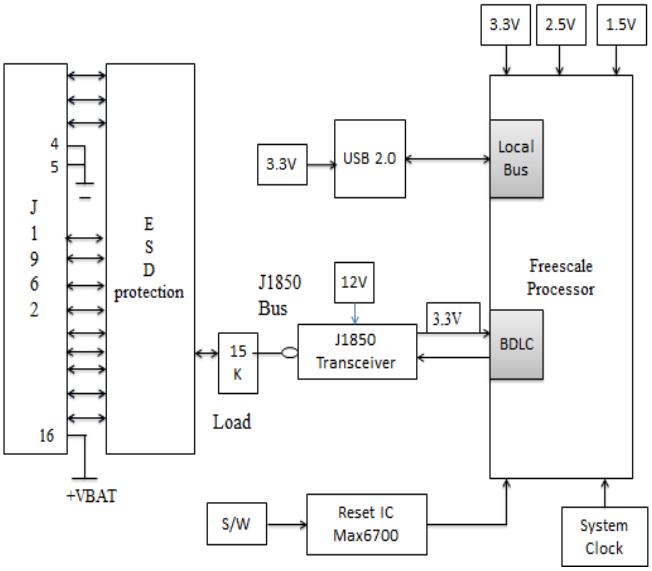

Fig- 4: Hardware block diagram

Hardware system is intermediate part between host and ECU. It is responsible for accepting data from ECU and sends to host and vice versa. Freescale processor is responsible for error checking, framing and flow control.

a) J1962 connector

SAE J1962 is diagnostic connector. It is 16 pin connector. It Allows connecting OBD device to vehicle subsystem e.g. ECU. In this project ECU is connected with hardware through this connector.

b) ESD (Electrostatic discharge) protection circuit

Today's automobiles contain number of wires and electronic components like processors, sensors. These Electronic modules are sensitive to electromagnetic disturbances (EMI), electrostatic discharges (ESD).So caution must be taken wherever electronic modules are used in the automotive environment.

c) J1850 (VPW) Transceiver

J1850 (VPW) bus uses signal levels (Nominally 0V -12V). This signal levels are incompatible with Freescale processor inputs and outputs, there is necessity of external circuitry to match these voltage levels. The J1850 (VPW) is single wire bus, so there is necessity to separate single wire into two transmission and reception paths required for processor. In this project transceiver is implemented using discrete logic.

Following screenshot shows signal level shifting is done with discrete logic:

In Fig. 5 yellow color is indicating signal on bus and violet color is indicating signal on transmitter of discrete transceiver. Figure shows that signal level on bus is modulated.

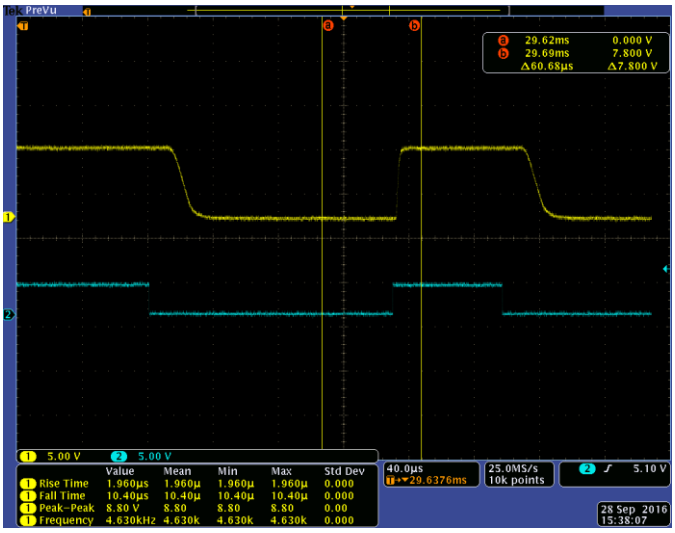

Fig-5: Signal transmitted on bus

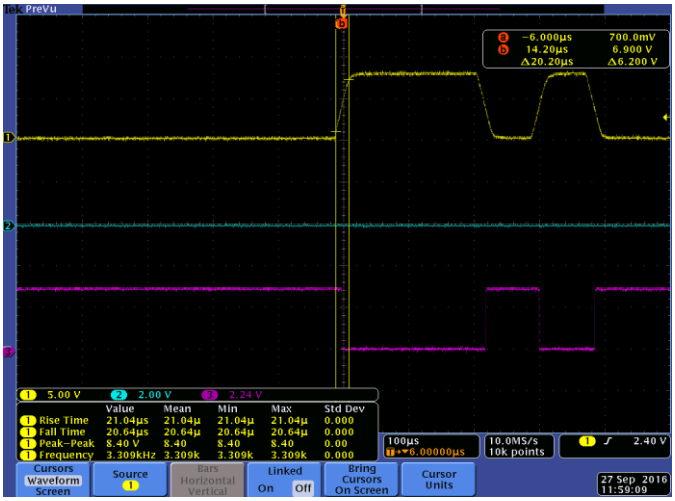

Fig- 6: Signal received from bus

In Fig. 6 yellow color is indicating signal on bus and violet color is indicating signal on receiver of discrete transceiver.

d) Freescale Processor

The Freescale processor MPC5200B is selected in this project. This processor supports automotive, networking, media, consumer, and industrial control applications. It enables high-speed data transfers and fast processing.

This processor supports operating system as Vxworks, Qnx etc. This processor have inbuilt J1850 Serial communication Module (Byte Data Link Controller).

BDLC Module: The BDLC module is a serial communication module. It is used to send and receive data on SAE J1850 (VPW) serial communication module. BDLC performs all of the network access, arbitration, message framing and error detection duties. The BDLC module detects several types of transmit and receive errors which can occur during the transmission of a message onto the J1850 bus. Errors detected are like transmission error, CRC error, bus fault, framing error and symbol error.
Features of BDLC module are:

1. 10.4 Kbps Variable Pulse Width (VPW) Bit Format
2. BREAK symbol generation Supported
3. Collision Detection
4. Hardware Cyclical Redundancy Check (CRC) Generation and Checking
5. Dedicated Register for Symbol Timing Adjustments
6. Polling and CPU Interrupt Generation with Vector Lookup Available

3.3 Firmware System Design

The main function of firmware is to act like middle layer for data transmission between host and J1850 protocol device.

a) Vxworks RTOS

To deal with real time environment it is essential to choose RTOS (Real time Operating system). This project contains three parts i.e. application, I/O system and J1850 driver. Application part which consist of number of API such as start communication, set parameters, build response, build acknowledgement. So there are number of events, interrupts, requests. To handle all this semaphore, message queue, events are required. So there is need of RTOS. In this project Vxworks RTOS is used.

VxWorks is a real-time operating system. It is developed as proprietary software by Wind River Systems. The key features of Vxworks are high performance, scalable RTOS. It supports ARM, Pentium, Intel X-Scale, Super H and other popular processors for embedded system design. Fast execution of application codes is possible because Vxworks supports kernel mode execution of tasks. Support of powerful development tools that make Vxworks easy and efficient to use. Many simulation tools, time-performance analysis tools, debug and test tools are provided, which makes VxWorks as an RTOS that supports development of almost any embedded application.

b) Firmware Flow

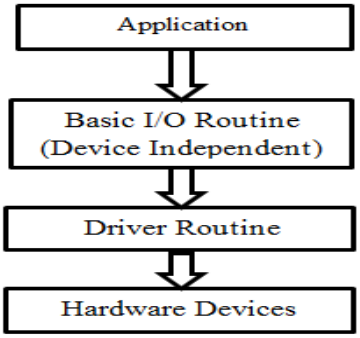

Fig- 7: Firmware flow

If host want to send any parameter to ECU then first frame is formed in application then it is send to I/O routine .I/O routine call basic write call and send data toJ1850 driver routine. Finally driver routine sends that data to J1850 bus. Total firmware is divided into three parts. They are application, I/O system and J1850 driver routine.

1. Application: Application consists of number of API's like start communication, send response to host, accept request from host, set communication parameters. Application is a user routine. It consists of main task that handle all activities of J1850 module.

2. I/O Routine: I/O routine is intermediate between application and J1850 driver. Vxworks I/O system is like a switch, which route user request to appropriate driver routine. Internally the Vxworks I/O has unique design that makes it faster and more flexible. The VxWorks I/O system is designed to present a simple, uniform, device-independent interface to any kind of device.

3. J1850 Driver routine: J1850 driver creates interface between Freescale processor and J1850 transceiver. This routine accepts data from upper layer send it to transceiver and vice versa.
Functionality provided by J1850 driver routine is

   - To transmit a stream of bytes on J1850 bus
   - To receive a stream of bytes which have been transmitted on J1850 bus
   - To initialise and configure BDLC module
   - To initialise and configure transmission and reception lines.

- To detect and initiate further processing for errors during transmission and reception.

3.4 Project Setup

Project setup contains two OBD devices, personal computer which acts as host, USB cables, and back to back connector. Device 1 acts as protocol device and device 2 acts as ECU. When Host want to communicate with ECU, The communication is done through J1850 (VPW).Device 1 and Device 2 are connected to each other by back to back connector. When host want to access any parameter from ECU then first host send request in the form of frame. Frame is passed through USB to device 1, device 1 send it to device 2.Device sends response to host through device 1.

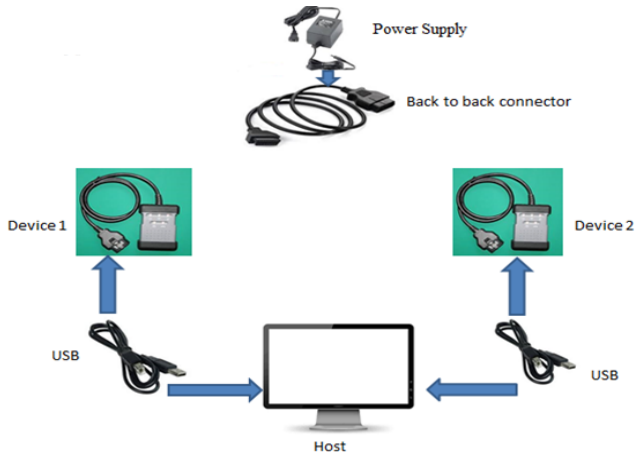

Fig- 8: Project setup

4. Results

4.1 Implemented J1850 Symbol timing Diagram

1. Start of frame : 220us

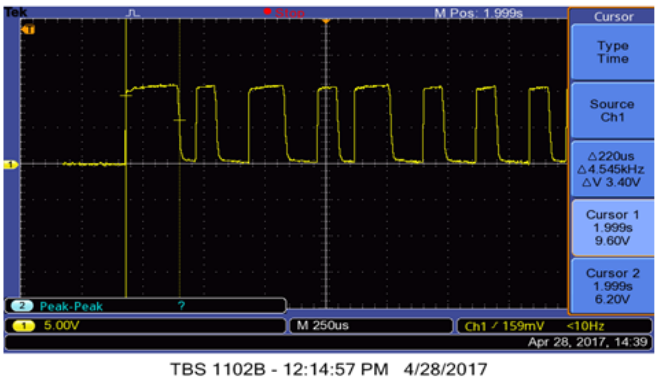

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Fig-9: Start of frame

2. Active Zero: 130us

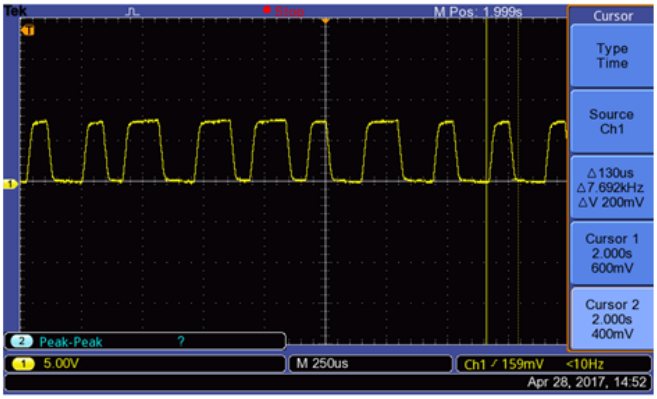

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Fig- 10: Active Zero

3. Active One: 70us

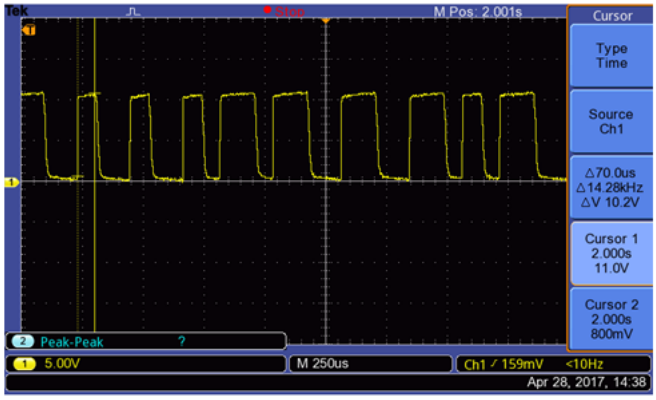

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Fig-11: Active One

4. Passive zero: 70us

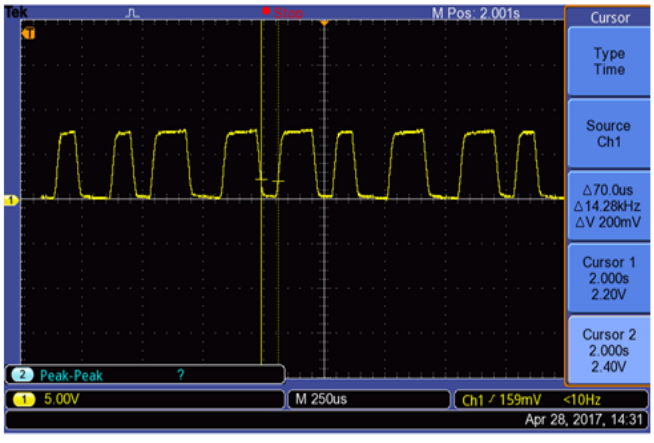

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Fig-12: Passive zero

5. Passive one: 130us

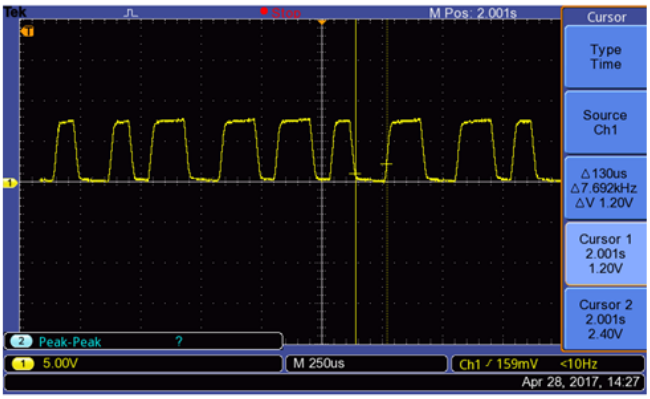

Fig-13: Passive one

Table 1: Symbol Timing values

Symbols	Standard value	Observed value
Start Of Frame	200us	220us
Active zero	128us	130us
Active one	64us	70us
Passive zero	64us	70us
Passive one	128us	130us

5. Conclusion

Hence the communication between ECU and host is established using Vxworks RTOS and Freescale processor through SAE J1850 protocol. SAE J1850 (VPW) protocol is fulfilling requirements class B communication protocols. Variable pulse width is single wire protocol which helps to reduce wire harness in automobile environment. This protocol is low cost, master- less protocol which consists of arbitration, CRC, and acknowledgement capability, so it can be used for number of application.

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