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Design and implementation of two stage operational amplifier

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Abstract -*in this presented paper design and implementation of two stage operational amplifier operates at 2.9V to 3.7V power supply at 180nm CMOS technology. The proposed two stage op amp produces high gain. Design and simulations results are verified using CADENCE tool. This design has accomplished a high power supply rejection ratio (PSRR) greater than -80db and other performance parameters such as input common mode range (ICMR), common mode rejection ratio (CMRR) and slew rate is verified.*

Key Words: Bandgap reference(BGR)1,power supply rejection ratio(PSRR)2,common mode rejection ratio(CMRR)3, Input common mode rejection range(ICMR)4.

1. INTRODUCTION

Operational Amplifier

The implementation of two stage operational amplifier is the most essential building blocks of the electronics system. In CMOS technologies the design of operational amplifiers continues to pose a challenge as the supply voltage and transistor channel lengths scale down. At different aspect ratio, there is a trade-off among speed, power, gain and other performance parameters. The design and implementation of a CMOS OPAMP is more difficult to get considerable DC gain with high unity gain frequency.

In this paper the aim of the design methodology is to propose straightforward yet desired equations for the design and implementation of high gain two staged CMOS operational amplifier. To do this, a simple analysis with some meaningful parameters phase margin, gain bandwidth, etc is performed. The method manipulate a very wide variety of amplifier architectures, but in this paper we apply the method to a specific two stage CMOS operational amplifier.

The presented paper simulation results have been obtained by 180nm CMOS technology. After the simulation, in ordered to optimize the better performance most of the transistors size still needed to be modified. The advantages of two stage op-amp have good gain, high output swing, low noise and good bandwidth over folded cascode. And it needs compensation, low PSRR value compared to folded cascode. Now a day design of an operational amplifier is to get high gain and simultaneously optimizing all process parameters has become mandatory.

II. DESIGN OF TWO STAGE OPERATIONAL AMPLIFIER

The designed circuit is to meet the required specifications is shown in fig.1. The topology of this circuit is that of a standard CMOS op-amp. The designed CMOS operational amplifier circuit consists of three subsections, namely differential gain stage, second gain stage and bias strings. The main aim of this topology was able to successfully meet all of the design specifications. [1]. The circuit operation has explained below.

- **Circuit Operation**

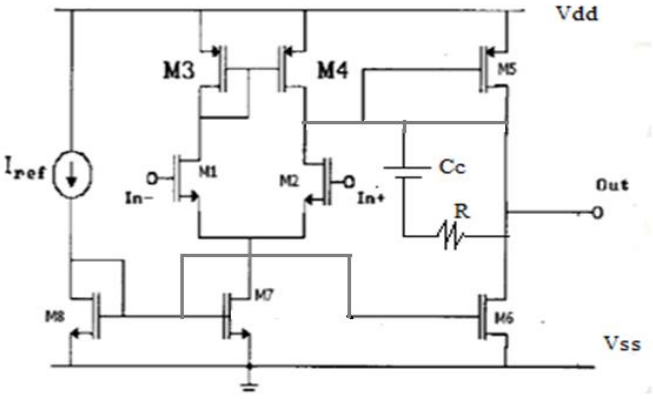

Fig.1 Circuit diagram of two stage operational amplifier

B. Differential Gain Stage

The differential gain stage consists of M1, M2, M3 and M4 form the first stage of the operational amplifier. Transistors M1 and M2 are standard NMOS which form the basic input stage of the differential amplifier. The gate of M1 and M2 are the inverting and non-inverting inputs with respect to transistors. The two main resistances that contribute to the output resistance are that of the input transistors and also the output resistance of the active load transistors, M3 and M4. The gain of the two stage operational amplifier is the Transconductance of M2 times the total output resistance at the drain of M2.

A differential input signal applied across the two input terminals that will be amplified according to the gain of the differential stage. In this circuit have advantages by using the current mirror active load transistors M3 and M4. The use of

active load devices gives a very large output resistance. The current mirror topology helps to conversion of the input signal from differential to single-ended. And load helps with common mode rejection ratio. The current from M1 is mirrored by transistors M3 and M4 as shown and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage will gives the single-ended output voltage. And also which constitutes the input of the second gain stage.

C. Second Gain Stage

This stage consists of transistors M5 and M6, as the name indicates, is to provide additional gain in the amplifier. Output from the drain of M2 and amplifies it through M5 which is called as common source configuration. Similar to the differential gain stage, this stage employs an active device M6, to serve as the resistance for M5. Gain of this stage can be determined by the Transconductance of M5 times the effective load resistance comprised of the output resistance of the M5 and M6. Where M5 acts as the load, M6 is acts as the driver.

D. Bias String

The biasing of the operational amplifier is achieved with four transistors. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. In this circuit proper biasing of other transistors in the circuit (M1-M5) is controlled by the node voltages. M5 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load as are the transistors M1 and M2 as shown in above fig.1.

The designed and implemented in this project is a two stage operational amplifier with an n-channel input pair. And op-amp uses a dual-polarity power supply Vdd and Vss so the given ac signals can swing above and below ground.

At the output the capacitance is to be connected as shown in fig.2.The design of two stage op-amp includes all the process parameters into account and which contribute in performance of overall gain of the system. High gain, bandwidth, and good power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) are some of the desired features of a good operational amplifier.[5].

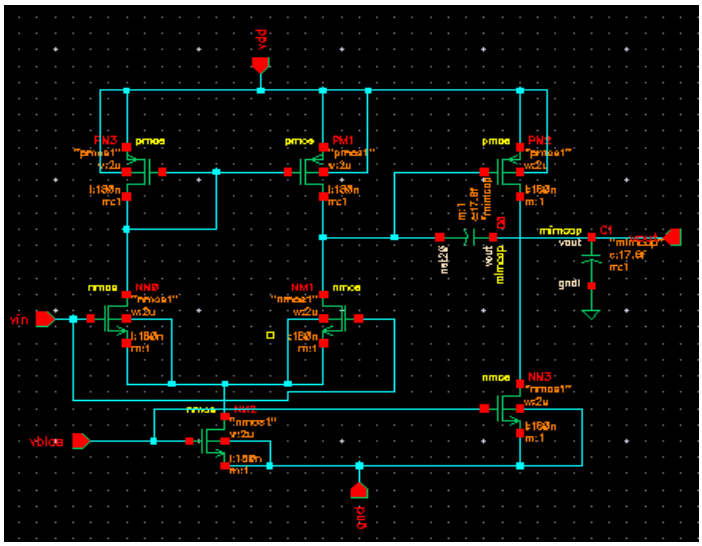

Fig. 2 Schematic of two stage operational amplifier

III. DESIGN CHOICE OF TWO STAGE OPAMP

TRANSISTORS	W Values(in um)	L Values(in um)
M1, M2	8	1
M3, M4	8	10
M5	32	10
M6	12	8
M7	6	8
M8	1	8

IV. DESIGN METHODOLOGY OF OP-AMP

Two stage operational amplifiers provide high gain and high output swing. For low frequency applications the gain is one of the most critical parameter. Overall gain is given by $A_V=A_{V1}*A_{V2}$ Where

AV=gain of op amp
A_{V1} (gain of 1st stage op amp) =gm1 (rds2|| rds4)
A_{V2} (gain of 2nd stage op amp) =gm7 (rds6|| rds7)

Maximum Output swing = *VDD – |VOD5|*
Minimum Output swing = *|VOD6|*
$gm1=(2u_{n,p}*Cox(w/l)*Id)^{1/2}$
Assuming $u_n*Cox=150uA/V^2$; $u_p*Cox=60uA/V^2$
Temperature coefficient =[(Vmax-Vmin) / (delta T* Voltage at 27'C)]*10^6
$R_0=1/ 2pir_0C_0$
ICMRmax = *VDD-VOD3+Vt1*
ICMRmin =*Vgs1+VOD7*
Slewrate (v/s) = *i/C = I7 / Cc*

III. SIMULTION RESULTS

1. **STB Analysis** In STB- Analysis we determine Phase margin, Gain and GB of the OP-Amp.

- Start frequency = 100mHz
- Stop frequency = 100 MHz

Output**:** The output results of AC analysis is as follows

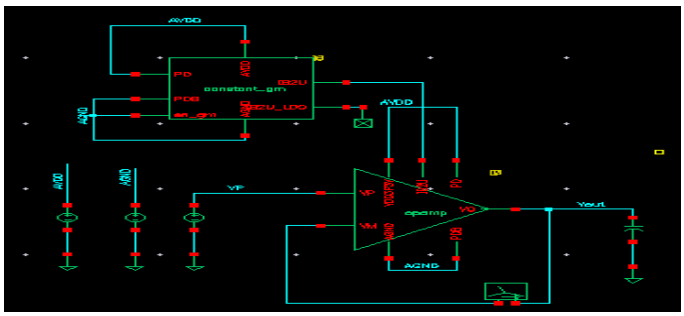

Fig. 3-test bench of STB analysis

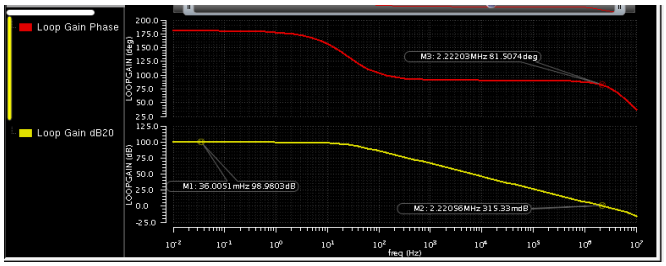

Fig.4 Gain and phase margin of two stage opamp

Gain = 98.98 dB ; UGB = 2.22MHz; PM= 81.507deg

2. CMRR (Common Mode Rejection Ratio)

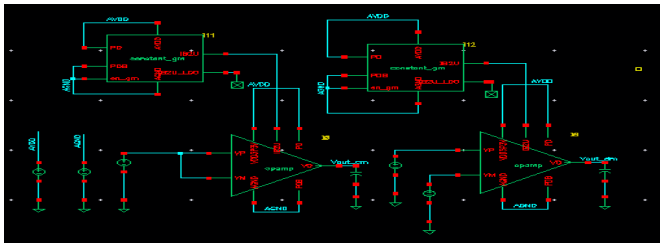

Fig.5-Test bench of CMRR

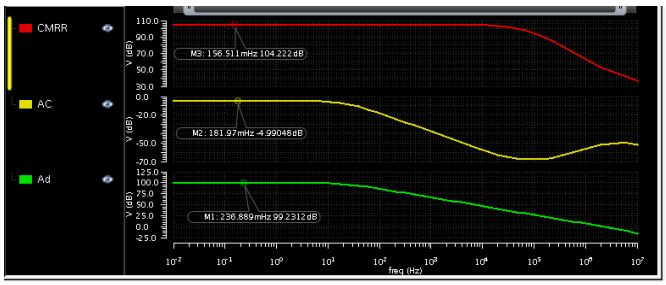

Fig. 6- Waveform of CMRR

CMRR = 20 log (Adm/ Acm)
CMRR =Differential gain – Common mode gain
= 99.23dB – (-4.99dB) =104.22dB

3. PSRR (Power Supply Rejection Ratio)

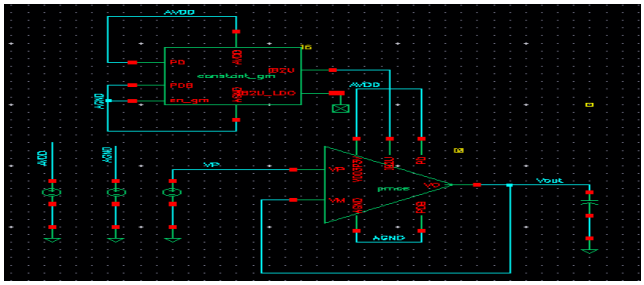

Fig.7-test bench of PSRR

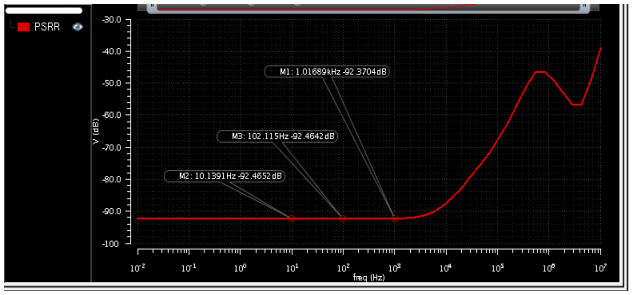

Fig. 8- waveform of PSRR

PSRR = 20 log (Ripple on Output / Ripple on Supply)
PSRR =-92.46 db @ 10Hz, 100Hz, 100KHz

4. INPUT COMMON MODE RANGE(ICMR)

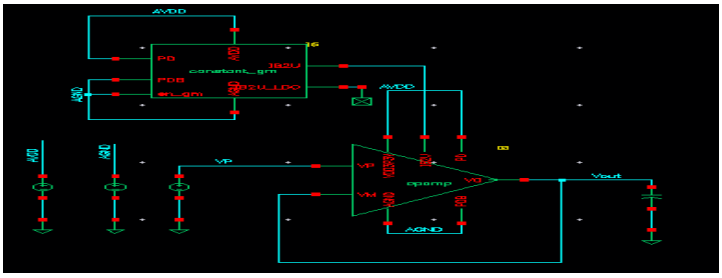

Fig.9-Test bench of ICMR

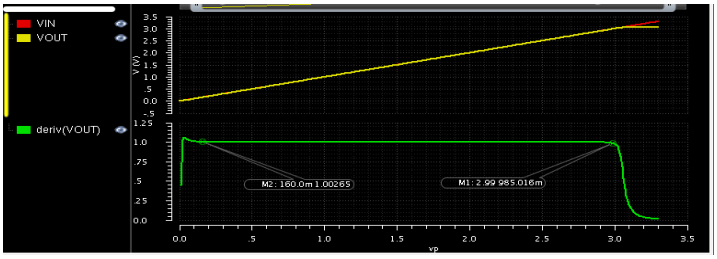

Fig.10- waveform of ICMR

Minimum ICMR = 160mV; Maximum ICMR = 2.99V

4. Slew Rate

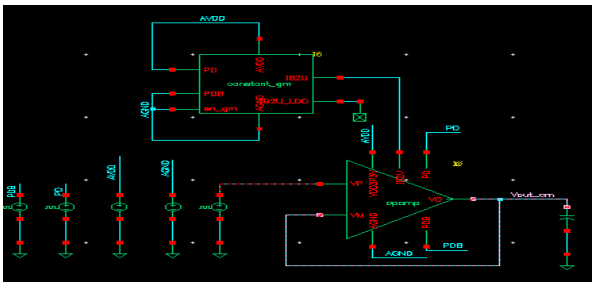

Fig.11- Test bench of slew rate

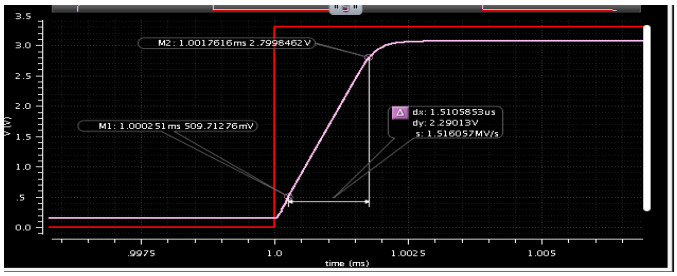

Fig.12- waveform of Positive slew rate

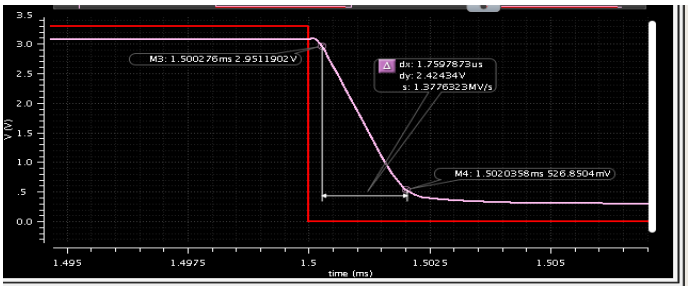

Fig.13- waveform of Negative slew rate

Positive slew rate = 1.51 V/us;Negative slew rate = 1.37 V/us

6. CURRENT CONSUMPTION

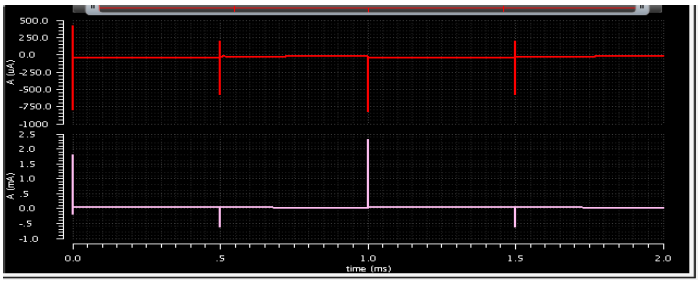

FIG.14- WAVEFORM OF TRANSIENT RESPONSE

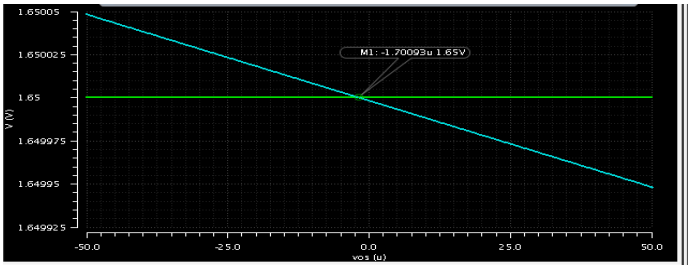

FIG.15-WAVEFORM OF INPUT VERSUS OUTPUT

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Option
1	V2/PLUS		☐	☑	yes
2	V1/PLUS		☐	☑	yes
3	avdd_crnt	34.6373u	☑	☐	
4	agnd_crnt	34.7194u	☑	☐	

FIG.16- TOTAL CURRENT CONSUMPTION TABLE

INPUT OFFSET = 1.7UV

7. NOISE ANALYSIS

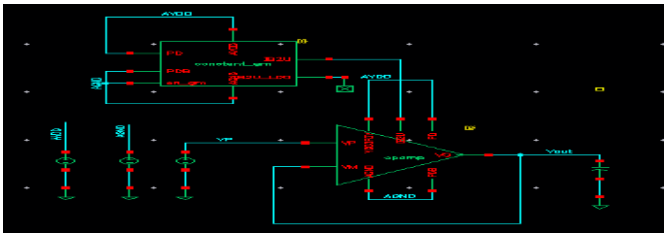

FIG.17- TEST BENCH OF NOISE ANALYSIS

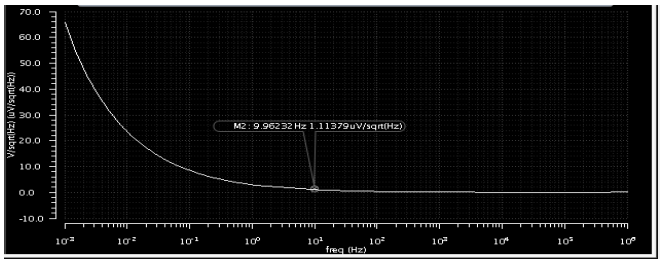

FIG.18- WAVEFORM OF INPUT NOISE

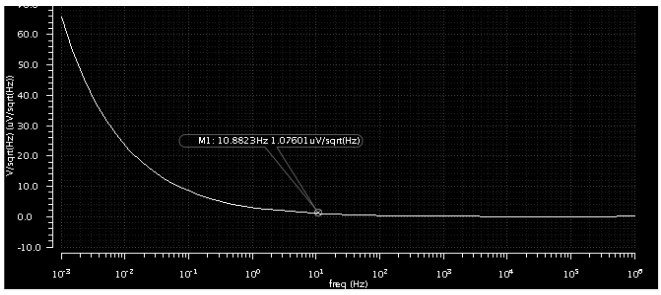

FIG.19- WAVEFORM OF OUTPUT NOISE

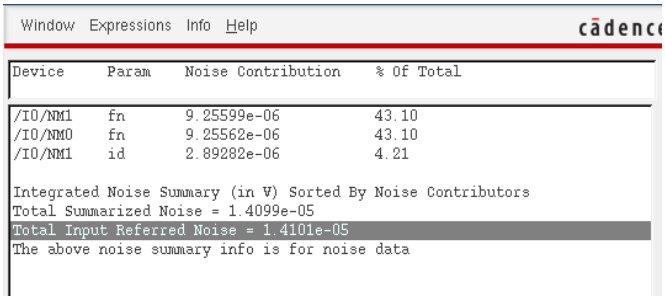

FIG.20- TOTAL NOISE TABLE

IV.SIMULATED RESULT TABLE

PARAMETERS	VALUES
CMRR	104.21db
ICMR	Min icmr = 160mV Max icmr = 2.9mV
PSRR	-92.46 dB
SLEWRATE	Positive slewrate=1.51 V/us Negative slew arte = 1.37 V/us Input offset voltage= -1.7uV
(STB ANALYSIS) Phase margin Gain UGB Frequency	81.507 deg 98.98 dB 2.22MHz
NOISE ANALYSIS	14.099uV/sqrt (Hz)

CONCLUSION

This presented paper analyzed the behaviour of a two stage CMOS op-amp. The simulated result shows that the designed operational amplifier has successfully satisfied all the given specifications. By using CADENCE tool results are to be verified for the different parameters.This presented paper operates in saturation mode and regulates its bias current. The designed and implemented two stage operational amplifier achieved high PSRR of -92.46db and high gain bandwidth of 98.98db, UGB frequency of 2.22MHz.

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