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Implementation of FPGA based Memory Controller for DDR2 SDRAM

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Abstract - *Multimedia applications plays very important role in the field of VLSI design and embedded systems. They need large amount of memory storage with higher bandwidth and higher speed. To overcome this hazard a memory controller is required. A memory controller is a device that stores the data and gives it back whenever required. Real time recording of an audio data and finally storing it without losing the data is difficult task. This paper describes Double Data Rate Synchronous Dynamic Random Access memory controller for storing the audio data. The design uses finite state machine (FSM) architecture that is developed for testing of this algorithm. The tool used to simulate this design is Xilinx ISE design suit. The hardware used to synthesize this design is FPGA Spartan-3 kit.*

Key Words: **FSM, DDR2, SDRAM, FPGA, Xilinx**

1. INTRODUCTION

Memory controller is very important component in the field of VLSI design. DDR2 SDRAM is the higher version of DDR SDRAM. This project can be used in many of the applications such as mobile phone communication, audio/video conferencing, audio based web search, weather forecasting and many more applications. The major difference between these is the prefetch length. The prefetch length of DDR SDRAM is 2n whereas that of DDR2 SDRAM is 4n meaning the internal bus width of DDR2 SDRAM is 4 times wider than the external bus width.

Now let us compare DDR SDRAM with DDR2 SDRAM. At certain clock frequency DDR2 SDRAM transfers twice the data per clock cycle than DDR SDRAM. The power consumption of DDR SDRAM is 2.5V and that of DDR2 SDRAM is 1.5V. The chip density of DDR SDRAM is 1 GB and that of DDR2 SDRAM is 4 GB. Thus DDR2 SDRAM has higher speed, density and low power consumption then DDR SDRAM.

2.IMPLEMENTATION

Figure 1 represents the basic block diagram of DDR2 SDRAM. It has differential clock CK and CK#. All the input signals and address signals are samples at the crossing of positive edge of CK and negative edge of CK#. CKE is the clock enable which should be kept high for all the operations. CS# is the chip select which should always be low to keep the chip active. RAS#, CAS# and WE# are the three command inputs which performs all the operations such as read, write, refresh, bank active, precharge etc of DDR2 SDRAM. A0 to A13 is the 14-bit of row address and it has a 16-bit of bidirectional data bus. DM is the data mask which is the input for write operation to occur.

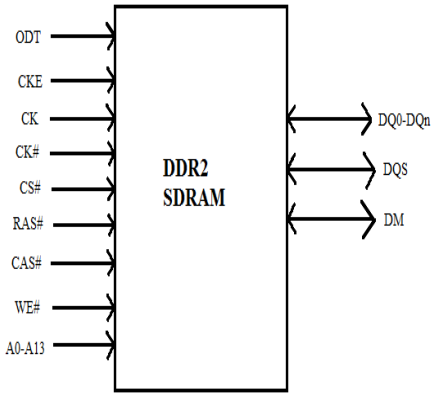

Fig -1: Block diagram of DDR2 SDRAM

Function	CKE Previous Cycle	CKE Current Cycle	CS#	RAS#	CAS#	WE#	BA2–BA0	An–A11	A10	A9–A0	Notes
LOAD MODE	H	H	L	L	L	L	BA	OP code			4, 6
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH exit	L	H	H	X	X	X	X	X	X	X	4, 7
			L	H	H	H					
Single bank PRECHARGE	H	H	L	L	H	L	BA	X	L	X	6
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank ACTIVATE	H	H	L	L	H	H	BA	Row address			4
WRITE	H	H	L	H	L	L	BA	Column address	L	Column address	4, 5, 6, 8
WRITE with auto precharge	H	H	L	H	L	L	BA	Column address	H	Column address	4, 5, 6, 8
READ	H	H	L	H	L	H	BA	Column address	L	Column address	4, 5, 6, 8
READ with auto precharge	H	H	L	H	L	H	BA	Column address	H	Column address	4, 5, 6, 8
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
Power-down entry	H	L	H	X	X	X	X	X	X	X	9
			L	H	H	H					
Power-down exit	L	H	H	X	X	X	X	X	X	X	9
			L	H	H	H					

Fig -2: Truth table of DDR2 SDRAM

When DM is low the input is masked and when DM is sampled high the write operation occurs. DQS is a bidirectional data strobe and ODT is on die termination

which improves the signal quality. Figure 2 represents the truth table for DDR2 SDRAM which shows all the operation required for this project.

3.DDR2 SDRAM OPERATIONS

There are five operations refresh, precharge, bank active, write and read.

3.1 Refresh

Refresh means reading the data from a particular address and rewriting the same data on that particular address without modifying it.

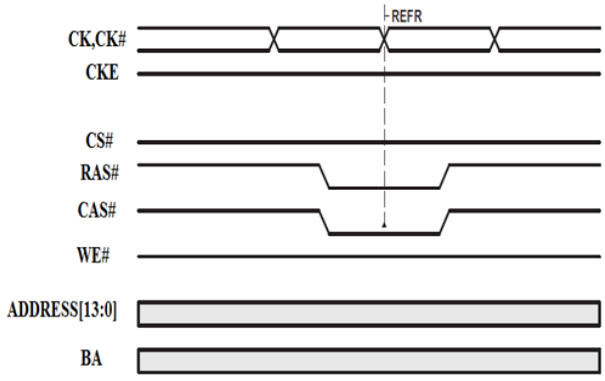

Fig -3: Waveform for refresh operation

Figure 3 shows the wave form for refresh operation. When the clock is enabled (CKE=1) and when CS, RAS, CAS these signals are low and WE is finally sampled high the refresh operation occurs. And when CS, CAS, RAS are sampled high it enters into idle state. The data must be refreshed after every 64ms so that the data is not lost. This is the refresh operation.

3.2 Precharge

Precharge is used to open a row in a selected bank or open a row in all the banks. Figure 4 shows the wave form for precharge operation.

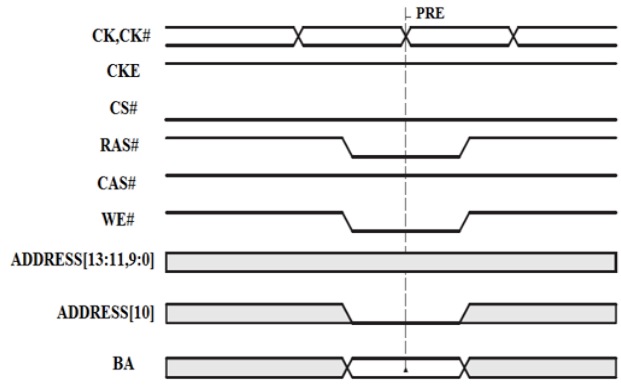

Fig -4: Waveform for precharge operation

When the clock is enabled (CKE=1) and when CS, RAS, WE these signals are low and CAS is high the precharge operation occurs. The A [10] bit of row address should be low while precharge operation. And when CS, CAS, RAS are sampled high it enters into idle state.

3.3 Bank Active

Figure 5 represents the wave form for bank active operation. When the clock is enabled (CKE=1) and when CS, and RAS these signals are low where as CAS and WE are high the bank active operation occurs. And when CS, CAS, RAS are sampled high it enters into idle state.

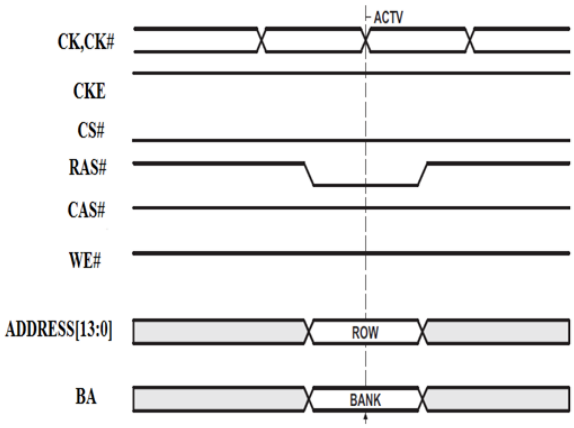

Fig -5: Waveform for bank active operation

3.4 Write

Figure 6 represents the wave form for write operation. When the clock is enabled (CKE=1) and when CS, CAS and WE these signals are low where as RAS is high the data is written onto the particular bank and the write operation occurs. And when CS, CAS, RAS are sampled high it enters into idle state. While the write operation occurs the A [10] bit of row address should be low and the correct column address should be present for the data to be written.

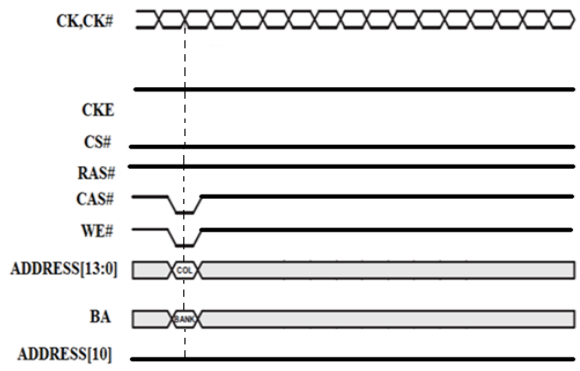

Fig -6: Waveform for write operation

3.5 Read

Figure 7 represents the wave form for read operation. When the clock is enabled (CKE=1) and when CS and CAS these signals are low where as RAS and WE are high the data is read from the particular bank and the read operation occurs. And when CS, CAS, RAS are sampled high it enters into idle state.

While the read operation occurs the A [10] bit of row address should be low and the correct column address should be present for the data to be read.

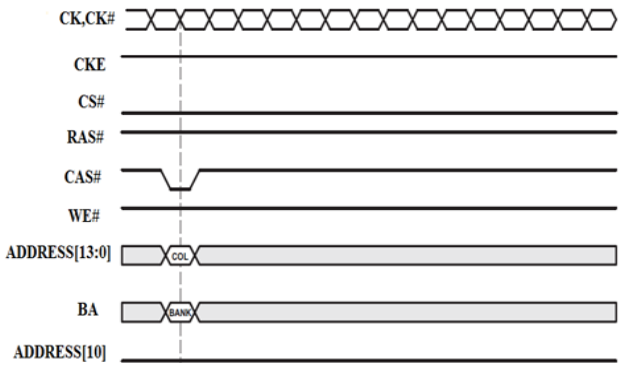

Fig -7: Waveform for read operation

4.STATE MACHINE

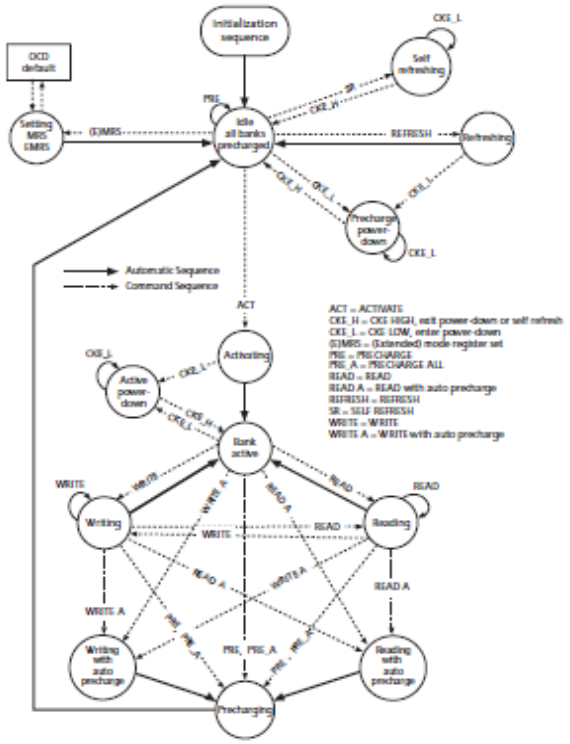

Fig -8: State machine

Figure 8 represents the combined state machine when any one of the signal is given high the operation occurs according to the truth table.

5.Results

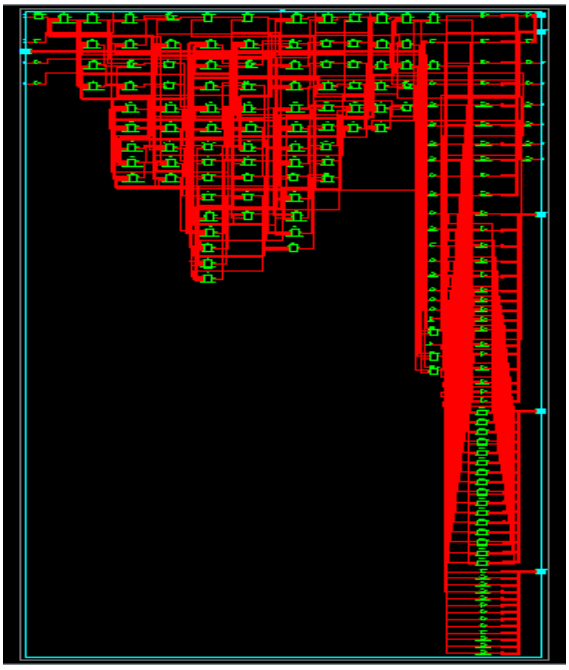

Fig -9: Tec schematic of reconfigurable device

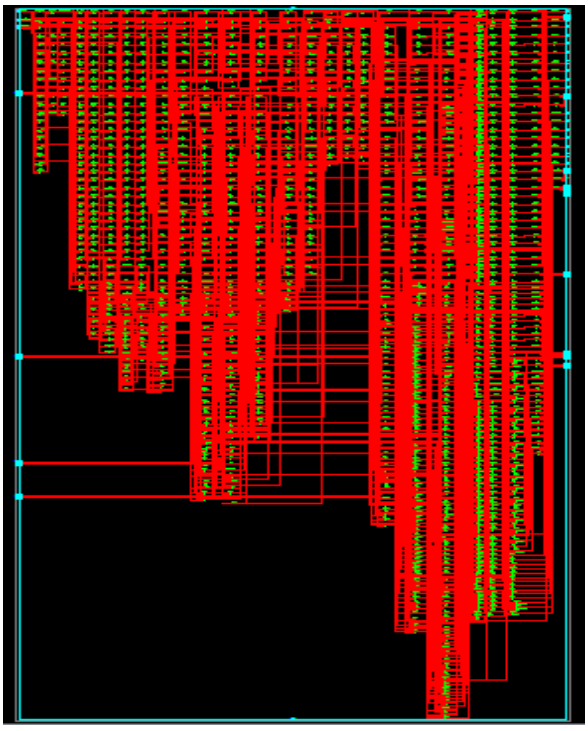

Fig -9: Tec schematic with IP

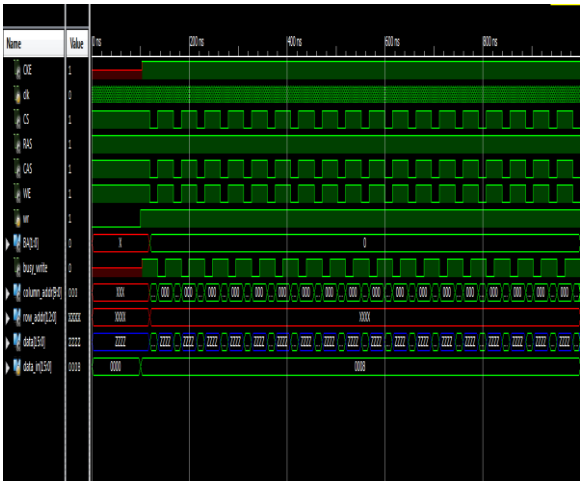

Fig -10: Simulation result of write signal

The above figure represents the write waveform for DDR2 SDRAM according to the command given the operations are performed. When CS, CAS and WE these signals are low where as RAS is high the write operation occurs. When CS and CAS these signals are low where as RAS and WE are high the read operation occurs.

6.CONCLUSIONS

SDRAM has become the major component in VLSI design industry. DDR2 SDRAM memory controller can be used in many other applications such as image processing, video processing etc. We can optimize the memory controller in area, power, latency etc. There are many researches going on DDR2 SDRAM controller in the VLSI industry by the scientists now days.

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[3] Benny Akesson, Kees Goossens and Markus Ringhofer published a paper with title 'A Predictable SDRAM Memory Controller'.

[4] Prof. Arun.S.Tigadi1, Padmashree. G International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization)Vol. 5, Issue 8, August 2016 Design and Implementation of Memory Controller for Real Time Video Acquisition using DDR3 SDRAM.