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DESIGN AND IMPLEMENTATION OF 6T SRAM USING FINFET WITH LOW POWER APPLICATION

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Abstract- *CMOS devices are facing many problems because the gate starts losing control over the channel. These problems includes increase in leakage currents, increase of on current, increase in manufacturing cost, large variations in parameters, less reliability and yield, short channel effects etc Since conventional CMOS is used to design SRAM, but it is also facing the problem of high power dissipation and increase in leakage current which affects its performance badly. Memories are required to have short access time, less power dissipation and low leakage current thus FINFET based SRAM cells are recommended over CMOS based SRAM cells. Reducing the leakage aspects of the SRAM cells has been very essential to enhance the stability of the cell. Therefore many low power techniques are used to reduce the power dissipation and leakage currents. These include Multithreshold CMOS (MTCMOS), variable threshold CMOS (VTCMOS), Stacking technique, power gating, Self controllable voltage level (SVL) technique etc. In this paper we propose use of MTCMOS technique to design a FINFET SRAM cell and compare it with FINFET SRAM cell in terms of dynamic power dissipation. All the simulation are done on symica using 14nm technology and predictive technology model (PTM).*

Key Words: **FINFET, SRAM, Dynamic Power dissipation, Energy Efficiency, CMOS, MTCMOS**

1. INTRODUCTION

With the advancement in the VLSI field, FINFET SRAM has been evolved as a revolutionary technology to offer 7nm size of transistor design to compensate for the need of superior storage system. The basic reason of this revolutionary technology is because of the three dimensional design of the gate which lowers its controlling dependencies over conventional drain and source terminal. The conventional transistor design faces the problem of short channel effect, which is completely removed by present design principle of FINFET. Conventional MOSFET also faces the problem due to variations of arbitrary dopant which is also removed due to FINFET as there is no channel doping mechanism in it. In FINFET circuits lower levels of supply voltage occurs in comparison to the planer CMOS circuits as there are also less number of energy points as well as less number of points for product of delay and energy. Therefore we get better stability in the voltage due to FINFET. At the same time, memory storage system like SRAM suffers due to high occupancy of cache memory in the chip area as well as it also suffers from maximum energy consumption of the chip power [6].

1.1 CMOS BASED SRAM

An SRAM cell is the key component storing a single bit of binary information. Memory circuits, mainly caches, are predicted to occupy more than 90% of the chip silicon area in the foreseeable future. This makes its design and test to be robust without any room for errors. A 6T CMOS SRAM cell is very popular in the IC industry due to its lowest static power dissipation among various circuit configurations. In addition, the CMOS Cell offers superior noise margins. A typical MOSFET-based 6-T SRAM cell is shown in Figure 1. It has two cross coupled inverters forming a latch and two ntype access transistors. The gate terminal of the access transistors is connected to the word line (wl) and source terminal is connected to bit line (bl) and bit line bar (blb) respectively. Whenever the memory element is to be used for read or write operation, the access transistors must be switched ON. There is a requirement that SRAM cell should provide wider noise margin and high speed but it is a major problem because if we require high speed then the leakage power increases [6].

Another problem with conventional planar SRAM is that large scaled technologies are used in design principle of SRAM that provides smaller size with minimum supply voltage. This provides us with narrow difference between the cut-off voltage and the supply voltage. Sometimes this narrow difference becomes highly unstable especially when design requires increases in number of transistors with reduced size in order to maintain large storage points [6]. Device design for an SRAM is governed by the stability, power consumption, and access time of an SRAM cell.

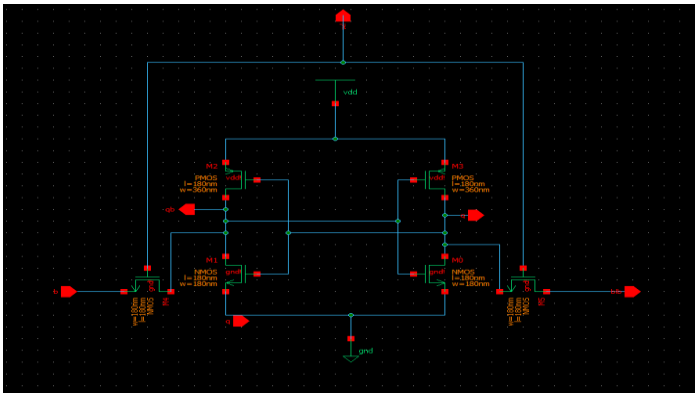

Fig.1.1 Schematic of CMOS based SRAM

1.2 FINFET BASED 6T SRAM CELL

It is expected that memories will be the major occupancy in the future design. Because of this fact scaling turns out to be considerably all the more difficult and important. In FINFET the electrostatic control of a gate is enhanced because of gate control from numerous sides of the fin. Short channel effects, for example, subthreshold degradation, Vth roll of width length and drain induced barrier lowering (DIBL) are improved due to multigate MOSFET. Memories are required to have short access time, less power dissipation and low leakage current thus FINFET based SRAM cells are recommended over CMOS based SRAM cells. FINFET based SRAM cells are more popular due to the low power dissipation. FINFET based 6T SRAM cell structure differs from the conventional 6T SRAM [7]. It has two cross coupled inverters as basic memory element and two FINFET based access transistors. The gate terminal of the access transistors is connected to the word line (wl) and source terminal is connected to bit line (bl) and bit line bar (blb) respectively. Whenever the memory element is to be used for read or write operation, the access transistors must be switched ON. During writing and reading operation of the SRAM cell, the access transistors are turned on through the word line while they are turned off during hold condition. The FinFET based 6T SRAM cell design is shown in Fig 1.2.

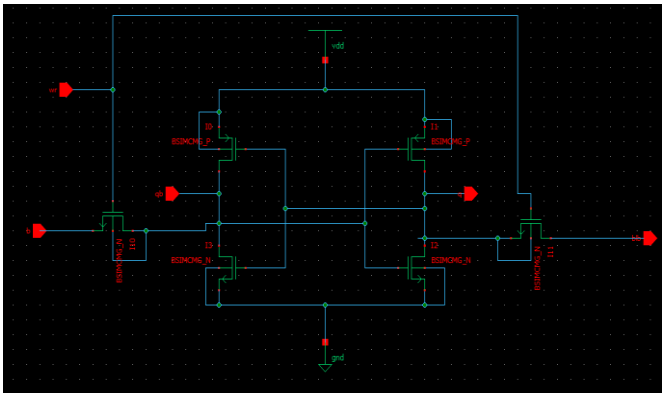

Fig.1.2 Schematic for FINFET based SRAM

2. DESIGN TECHNIQUES FOR REDUCING THE LEAKAGE POWER FOR LOW POWER SRAM

Most microelectronic frameworks invest impressive time and energy in a standby state. The vitality of the DC-DC converter to enter or leave a low power mode must be considered deliberately. In the event that the cost of transitioning to and from a low standby power state is sufficiently low then the policy of entering the low power state when the system is in idle state might be adopted. In that place the expected duration of the standby state must be precisely computed and considered when we are using a power management approach. In the following area, techniques are exhibited for decreasing the subthreshold leakage currents that are in STANDBY or ACTIVE model. One such technique is multithreshold CMOS (MTCMOS).

2.1 MULTITHRESHOLD CMOS (MTCMOS)

Multi-threshod CMOS (MTCMOS) is a variety of CMOS chip innovation which has transistors with multiple threshold voltages (Vth) keeping in mind the end goal is to improve delay or power. The gate voltage where a inversion layer is formed at the interface between the gate oxide layer and the substrate (body) of the transistor is simply the threshold voltage of transistor. Low Vth devices switch fastly, and are in this way valuable on critical delay paths to limit clock periods. The drawback is that low Vth devices have significantly higher static leakage power. High Vth devices are utilized on non-critical paths to decrease static leakage power. High Vth devices causes reduction in static leakage by 10 times as contrast to low Vth devices.

In the ACTIVE mode, the sleep transistor is turned on. The function of the circuit remains same. In the STANDBY state, the transistor is switched off, which disconnects the gate from the ground. Note that to bring down the leakage, the threshold voltage of the sleep transistor must be larger. If this condition is not adopted, the sleep transistor will have a high leakage current, which will make the power gating less viable. Less leakage might be accomplished if the width of the sleep transistor is smaller than the joined width of the transistors in the pull down circuit. To ensure the correct usefulness of the circuit, the sleep transistor must be deliberately sized to diminish its voltage drop while it is on. The voltage drop on the sleep transistor diminishes the effective supply voltage of the logic gate. Additionally, it causes increase in threshold voltage of pull down transistors because of the body effect [7].

2.2 DESIGN OF MTCMOS FINFET SRAM

In MTCMOS technique, low threshold voltage transistors gets disconnected from power supply by utilizing high threshold sleep transistor on the top and base of the logic circuit. Transistor having low threshold voltage (low-Vth) is utilized to plan logic. The sleep transistors are controlled by

the clock signal. During the dynamic mode, the clock signal is made high, causing both high Vth transistor to turn on and give a virtual power and ground to the low Vth logic circuit. At the point when the circuit is in-standby mode, the sleep signal is made to go low, compelling both high Vth transistor to cutoff and detach power supply source (VDD) cables from the low Vth logic circuit. This outcomes in a low leakage current from power supply source to ground in standby mode. One drawback of MTCMOS procedure is the number of sleep transistors and its sizing gets troublesome for very large circuits. Fig 1.3 shows the schematic of FINFET based SRAM CELL using MTCMOS technique.

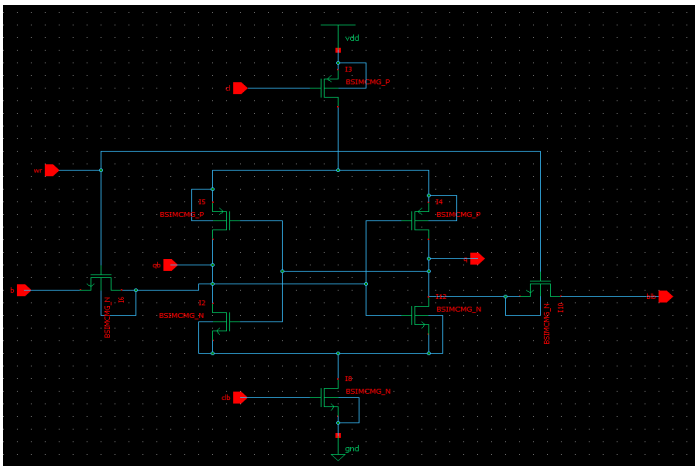

Fig.2.1 schematic of FINFET based SRAM Cell using MTCMOS technique

3. IMPLEMENTATION OF FINFET SRAM USING MTCMOS

This technique reduces standby power by using the pFET switches with higher threshold voltage Vthp in between power supply and low Vth SRAM cell transistor for disconnecting the power supply and nFET switches with higher threshold voltage Vthn using in between ground and low Vth SRAM transistor for disconnecting the ground from low Vth SRAM cell. In the active mode low Vth transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high Vth sleep transistors are switched off which cause detachment of low Vth transistor from supply voltage and ground thereby reducing sub-threshold leakage current. There are some serious issues concerned with MTCMOS technique such as the need for additional fabrication process for higher Vthp and higher Vthn and the fact that data cannot be restored by the storage circuits based on this technique. Fig.1.4 shows the implementation of FINFET based SRAM cell using MTCMOS technique.

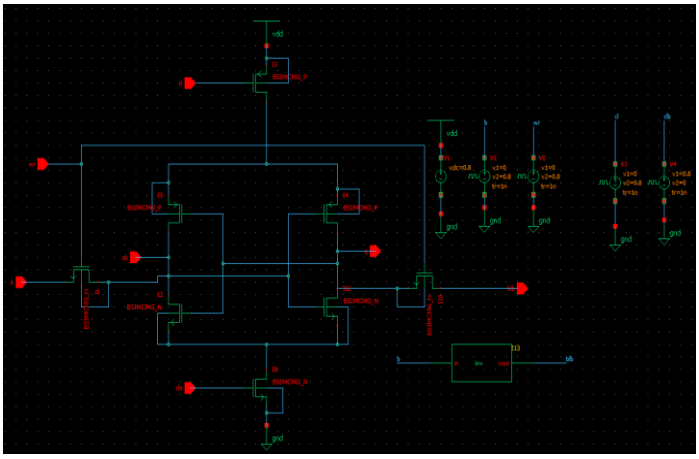

Fig 2.2 shows the implementation of FINFET based SRAM cell using MTCMOS technique

3.1 WAVEFORM OF WRITE OPERATION OF FINFET SRAM USING MTCMOS

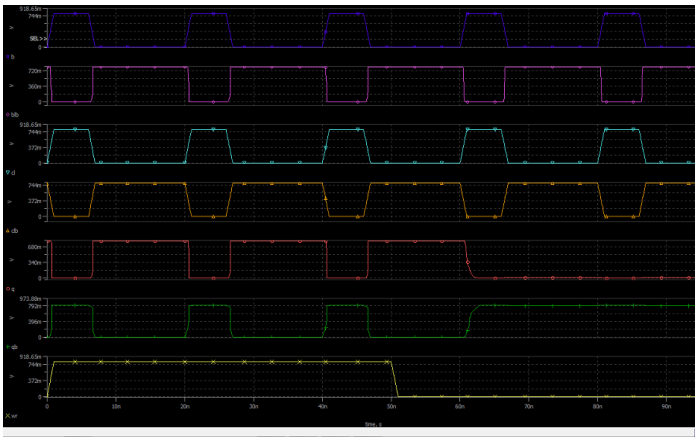

Table -1: Table 1.1 compares power consumption of low power FINFET SRAM with some conventional SRAM and FINFET SRAM

Dynamic power consumption in CMOS SRAM during write operation	240nw
Dynamic power consumption in FINFET SRAM during write operation	21.07nw
Dynamic power consumption in MTCMOS SRAM during write operation	11.26nw

4. RESULTS

Simulation of MTCMOS FINFET SRAM is done using 14um technology on symica tool. Dynamic power dissipation is computed which is simply product of power supply and the current. In case of MTCMOS SRAM it is computed by multiplying current component at the drain terminal of PFET transistor (which is Q in above design) by power supply. The dynamic power dissipation obtained in case of MTCMOS FINFET SRAM is 11.26nw. The MTCMOS technique reduces dynamic power dissipation by 46.5% as compared to dynamic power dissipation of FINFET SRAM.

3. CONCLUSIONS

This work explains the designing of FINFET SRAM cell using MTCMOS. **S**tatic memory cells basically consist of two back to back connected inverters. The output of the second inverter is connected to the input of the first inverter. It also consists of two access transistors. The source terminal of access transistors are connected to the bit line. The write and read operation are enabled only when access transistors are turned on through the word line and turned off during hold condition. The sleep transistor are connected between the power supply and low Vth circuit or between the low Vth circuit and the ground. The dynamic power dissipation is calculated by multiplying current component at the drain terminal of PFET transistor (which is Q in above design) by power supply. Proper simulation results that justify the operation of each design are given. All circuits are designed on symica software using 14nm technology.

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