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Design and Implementation of Wallace Compressor Multiplier using Vedic Mathematics

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Abstract -*For arithmetic multiplication various Vedic multiplication techniques like Urdhvatiryakbhyam, Nikhilam and Anurupye have been used. It has been found that Urdhvatiryakbhyam Sutra is the most suitable which gives minimum delay for multiplication of all types of numbers. With the advent of new technology in the domain of VLSI, communication and signal processing, there is an ever growing demand for the high speed processing and low area design. In this paper, a modified compressor based multiplier is introduced that is 4:2 compressor and the Wallace compressor architectures. In addition to that it uses Vedic mathematics to get a high speed multiplication operation. In various applications of digital signal processing, multiplication is one of the key components. Vedic technique removes the redundant multiplication steps thus it reduce the propagation delay in processor and hence it reduce the hardware complexity in terms of area and memory requirement. This Vedic multiplier was coded in VHDL by using Xilinx ISE 13.2. The synthesis results indicated that the computation time delay for 4:2 compressor multipliers was 15.83ns and 12.71ns for Wallace compressor Vedic Multiplier.*

Key Words: multiplier, 4:2 compressors, Wallace compressor, Xilinx 13.2, etc.

1. INTRODUCTION

The processor speed depends on its multiplier's performance. This in turn raises the demand for multipliers for which operate with high speed as well as maintain low area and moderate power dissipation. Over the past few decades, several new novel architectures have been introduced, designed and explored. Booth's and modified Booth's algorithm based multipliers are quite popular in having modern VLSI design with some short comes. In these multiplier algorithms, the multiplication process, involves several transitional step before arriving at the final value. The intermediate stages include several additions, subtractions and comparisons which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since the speed is the major concern in any system, utilizing such type of architectures is not a good approach as it involves several time consuming operations.

1.1Digital Logic Design

A digital computer stores data in terms of digits (numbers) and proceeds in discrete steps from one state to the next state. The states of a digital computer typically involve bits. Digital logic is the basis of any electronic systems, such as computers and cell phones. Digital logic is rooted in binary code, a series of zeroes and ones each having an opposite value. This system facilitates the design of electronic circuits that convey information, including logic gates. Digital logic gate functions include and, or and not. The value system translates input signals into specific output. Digital logic facilitates computing, robotics and other electronic applications. The advent of integrated circuit technology has made it easier to design digital circuits. Today, the designer is not required to know the basic operation of various components such as capacitors, transistors etc. This involves complex mathematical calculations. For a given set of inputs the digital circuit always produces the same output at any instant of time unlike analog circuits whose outputs vary with variation. Digital signals are more robust and simple than analog signals with respect to temperature and process variations.

1.2 Vedic Multiplier

The Sanskrit word "Veda" is derived from the word "Vid", meaning to know without limit. The word "Veda" covers all veda-sakhas known to the humanity. Figure 1 shows basic block diagram of multiplier. The input signal is step by step compressed and multiplication operations perform to obtain the result.

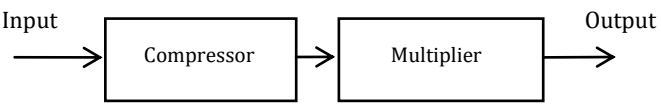

Fig -1: Basic Block Diagram of a Multiplier

A mathematician, Sri Bharati Krishna Tirthaji rediscovered Vedic mathematics that being there during

ancient India period. It basically depends on Vedic sutras. These sutras deal with arithmetic, analytical, algebra, geometry, trigonometry, etc. The Vedic mathematics sutras pave a great role in application of engineering and technology like signal processing, control engineering and VLSI due to its simplicity. Using Vedic mathematics all the partial products required for multiplication are obtained; then these intermediate partial products are added based on the Vedic mathematics algorithm to obtain the end result. This becomes advantages of having very high speed approach to achieve multiplication [3]. In this paper, a novel method is explore to further enhance speed of a Vedic multiplier by replacing the existing half adders and full adders of the Vedic mathematics based multipliers with compressors based adders. Compressors, in its several variants, are logic circuits which are skilled of adding more than 3 bits at a time as divergent to a full adder and capable of acting with a lesser gate count and higher speed in comparison with an equivalent full adder circuit.

The application of sutras saves a lot of time and effort in solving the most of the problems, when compared to the formal methods presently prevailing in this field. Despite the solutions appear mysterious; the application of the sutras is perfectly logical and rational. The computation made on the computer chase in a way, the principles implicit in the sutras. The Vedic sutras provide not only methods of calculation, but also give a way of thinking for their application.

Vedic multiplier is mainly based on the 16 sutras which are based on various fields of mathematics such as algebra, geometry, calculus, etc. Therefore the application of Vedic sutras to solve specific problems in Mathematics involves rational thinking, which helps to improve intuition.

2. VEDIC MATHEMATICS- BACKGROUND

Vedic mathematics was proposed by former Jagadguru Sankaracharya of Puri and he proposed a set of 16 sutras (aphorisms) and 13 sub-sutras (corollaries) from the Atharva Veda and then he developed methods and techniques for explain the principles containing the aphorisms and their corollaries, founded by Swami Bharati Krishna Tirtha (1884—1960), and named it as Vedic mathematics. The Vedic sutras can be applied to problems various fields and covers almost each and every branch of mathematics. They can be applied to multiplex problems which involve a large number of mathematical operations.

In general to perform the multiplication, the formula which is Tiryaghbhyam sutra known as “vertically and crosswise” and it can be applied to all type of multiplication. The specialty of this sutra is that partial product generation and addition can be done simultaneously. It is more efficient in binary multiplication and it is suitable for parallel processing which reduces delay in a design.

Vedic mathematics is part of four Vedas (books of wisdom). It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 13 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in atharva Veda because these formulae were constructed by swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That’s why Vedic mathematics has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristic, Vedic Mathematics has already crossed the boundaries of India and has become a leading topic of research abroad. Vedic Mathematics deals with several basic as well as complex mathematical operations. Thus methods of basic arithmetic are extremely simple and powerful [4, 9].

2.1 Multiplication using Vedic Mathematics

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.

These methods can be directly applied to plane and spherical geometry, trigonometry, conics, calculus (both differential and integral), and applied mathematics. In conventional mathematics the step required for calculation are more, in order to reduce the step for calculation in Vedic mathematics plays great role. This is so because the Vedic formulae are to be based on the natural principles on which the human mind works. Figure 2 indicate the line diagram for multiplication of two 2 digit numbers which perform the 2 digit multiplication operation. Take a two numbers, multiply the numbers in the unit place and put the product under unit place. Cross multiply first unit place tens place number and add the two products and place the answer to the left of the unit place's answer. Multiply the numbers in the tens place and place the answer to the left side of the previous answer step. This is a very interesting part of the mathematics and it presents some effective algorithms that can be applied to various branches of engineering [4].

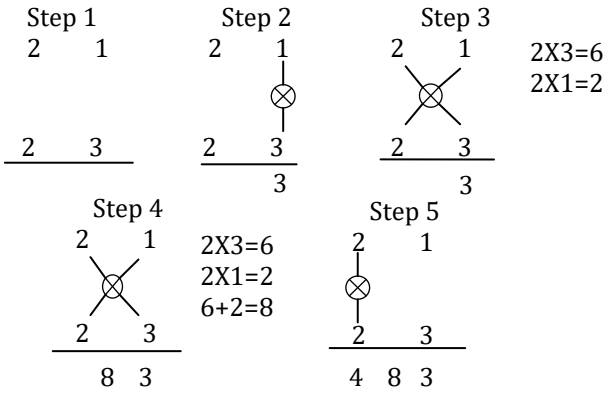

Fig- 2: Line Diagram for Multiplication of Two 2 - Digit Numbers

The multiplier architecture can be generally classified into three types. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second one is the parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the time consuming serial multiplier and the area consuming parallel multipliers.

3. DEVELOPMENT OF VEDIC MULTIPLIER

Tiryaghbhyam sutra is more efficient in binary multiplication and it is suitable for parallel processing which reduces delay in a design.

3.1 Compressor Based Adder

Several 4:2 and 7:2 compressor architectures have been used. Higher order compressors proposed used in the design. Compressor is used to reduce the number of bits in output and it easily swap the half adder and full adder output of the circuitry.

A) Compressor -3:2

A full adder is a 3:2 lossy compressor, it sums three one-bit inputs and returns the result as a single two-bit number; that is, it maps 8 input values to 4 output values. Thus, for example a binary input of 101 results in an output of 1 + 0 + 1 = 10 (decimal number 2). The carry-out represents bit one of the results, while the sum represents bit zero. There are various possible designs for the circuit most common are Dadda and Wallace trees. This type of circuit is mostly used in multipliers. The 3:2 Compressors can add 3 inputs having a single bit and produces 2-bit output. The gate level structure of 3:2 compressors is as shown in below figure 3.Full adder is also called as 3:2 compressor and the structure given below made of two half adder.

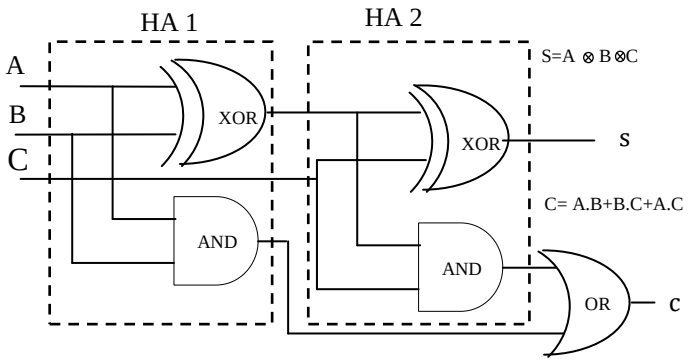

Fig- 3: Gate Level Structure of 3:2 Compressors

B) Compressors- 4:2

Compressors 4:2 can add 4 single bit inputs and one carry input bit, which produces 3-bit output. Figure 4 shows the basic block diagram for 4:2 compressor and figure 5 shows the full adder design by using logic gates.

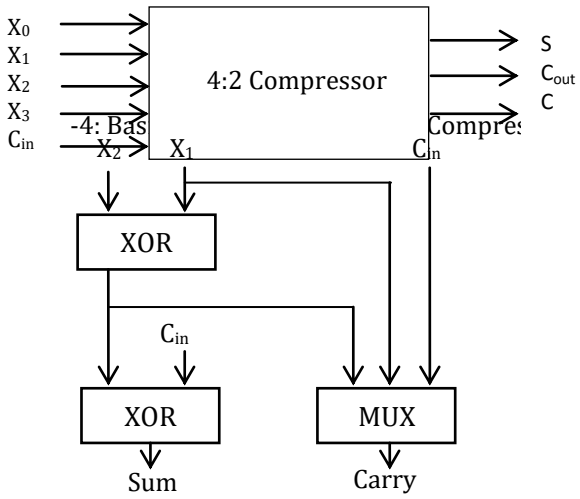

Fig -5: Full Adder Design by Using Logic Gates

It can be observed that the critical path is smaller in comparison with an equivalent circuit to add 5 bits by using full adders and half adders. The Figure 5 shows the Full adder design by using logic gates.

3.2. Wallace Tree Compressor

A Wallace tree implementation of a digital circuit for multiplying two integers, the following three steps:

1. Multiplication
2. Partial product reduction
3. Grouping

In this Wallace tree method, half adder for summation of 2- bit and full adder for summation of 3-bit was used. Here multiplicand of higher than 8-bits was more beneficial, because the addition of partial products was low in Wallace

tree and hence increases speed. Figure 6 shows partitions of the partial products of Wallace multiplier. This figure indicate grouping of 2-bit for half adder and 3-bit for full adder with compressed step by step data. In this process firstly multiplication of any two numbers carried out to generate the partial product. This partial product divided into three rows. Out of those, group of 2-bits consider as half adder and 3 bits as full adder. Both adders perform their operation which results into two rows, these two rows termed as Sum and Carry respectively. In that result forth partial product considered and converted into three rows, after that same procedure followed as mentioned above.

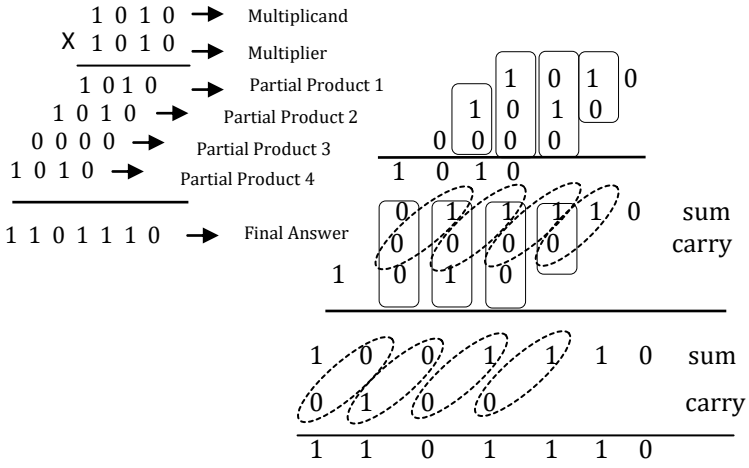

Fig-6: Partitions of the Partial Products of Wallace Multiplier

4. RESULTS AND DISCUSSION

The designing of Vedic multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Where smaller blocks are used to design the bigger one. The Vedic multiplier is designed using VHDL, as its give effective utilization of structural method of modeling. The individual block is implemented using VHDL. The functionality of each block is verified using simulation software Xilinx 13.2.

4.1 Performance Analysis of Multiplier

The system is based on 4:2 compressor and Wallace compressor techniques of Vedic multiplier. These two techniques are used in design the structure of 16 and 32-bit multiplier. Results of software implementation was observed and compared by implementing these multiplier structures on Xilinx FPGA platform. Analysis of different multipliers was observed with the help of design summary overview which allows a quick access to design overview information and synthesis reports. Performance analysis of different multiplier was done based on various parameters.

RTL schematic for 32x32 Vedic multiplier with 4:2 compressor is as shown in figure 7.There are three ports namely, data input (IN_1), data input (IN_2), data output (P), all signals are active high.
The representation of three ports:

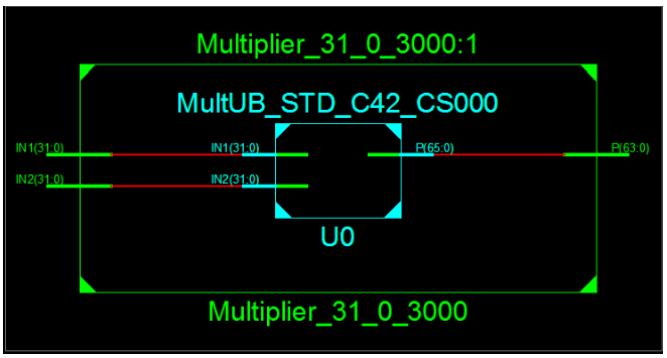

Fig -7: Schematic for 4:2 Compressor Vedic Multipliers

Analysis of 32X32 Multiplier with 4:2 Compressors

Analysis is carried out by designing 32-bit multiplier using 4:2 compressor multiplier architecture in Xilinx ISE Simulator. Slice flip flops are resources on the FPGA that can perform logic functions. Logic resources are grouped in slices to create configurable logic blocks. A slice contains a set number of LUTs, flip-flops and multiplexers. An LUT is a collection of logic gates hard-wired on the FPGA. LUTs store a predefined list of outputs for every combination of inputs and provide a fast way to retrieve the output of a logic operation.

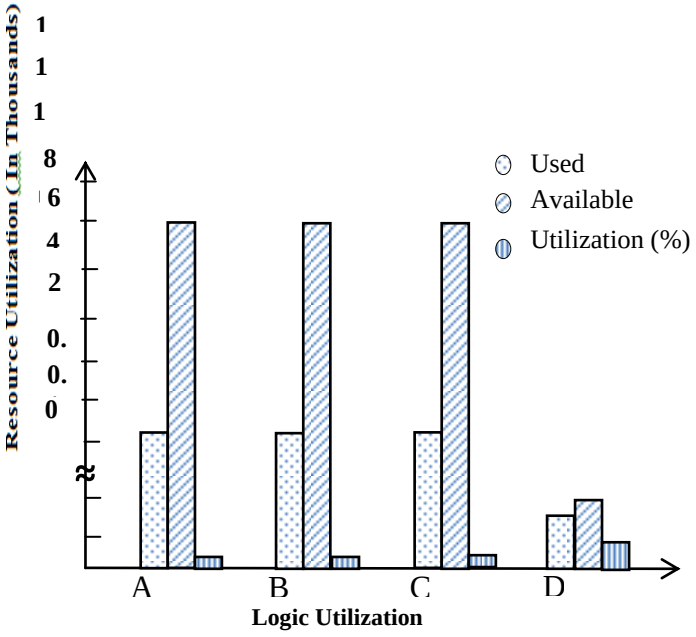

Fig – 8: Area Comparisons of 4:2 Compressor 32-bit Vedic Multipliers

Table 4.1 Resource Utilization for 32-Bit 4:2 Compressor Vedic Multiplier

Parameters	Resources		
	Used	Available	Utilization (%)
Number of Slices LUTs(A)	2330	12480	18
Number of LUT'S Flip-flops Pair used(B)	2330	12480	18
Number used as logic(C)	2330	12480	18
Number of bonded IOBs(D)	128	172	74

Resource utilization for implementation of 4:2 compressor Vedic multipliers enlisted in table 4.1 based on the percentage of resources consumed it is quite possible to estimate the area of the design. Figure 8 shows graphical representation of area comparisons of 4:2compressor 32-bit Vedic multipliers. It also expresses the complexity of the design.

The schematic for 32x32 Vedic multiplier with Wallace compressor is as shown in figure 9.There are Three ports namely, data input (IN_1), data input (IN_2), data output (P), all signals are active high.

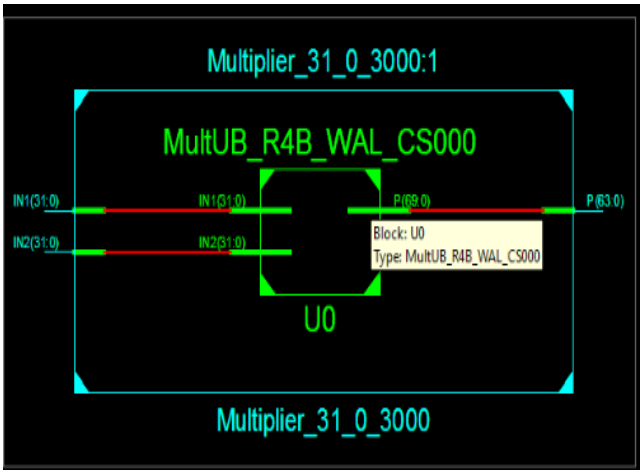

Fig-9: Schematic for Wallace Compressor Vedic Multiplier

Analysis of 32X32 Multiplier with Wallace Compressor

Analysis is carried out by designing 32-bit multiplier using Wallace compressor multiplier architecture in Xilinx ISE simulator. Slice flip flops are resources on the FPGA that can perform logic functions. Logic resources are grouped in slices to create configurable logic blocks. A slice contains a set number of LUTs, flip-flops and multiplexers. An LUT is a collection of logic gates hard-wired on the FPGA. LUTs store a predefined list of outputs for every combination of inputs and provide a fast way to retrieve the output of a logic operation.

Resource utilization for implementation of Wallace compressor Vedic multipliers enlisted in Table 4.2 Based on the percentage of resources utilized it is quite possible to estimate the area of the design. This table explained about available and used resources with percentage of utilization. For example 12480 available resources while 1560 used resource so percentage utilization found to be 12%, the same procedure for remaining parameters. It also expressed the complexity of the design. Figure 10 represents the Area comparisons of Wallace compressor 32-bit Vedic multipliers.

Table 4.2 Resource Utilization for 32-Bit Wallace Compressor Vedic Multiplier

Parameters	Resources		
	Used	Available	Utilization (%)
Number of Slice LUT's(A)	1560	12480	12
Number of LUT's Flip-flops pair used(B)	1560	12480	12
Number used as logic(C)	1560	12480	12
Number of bonded IOBs(D)	128	172	74

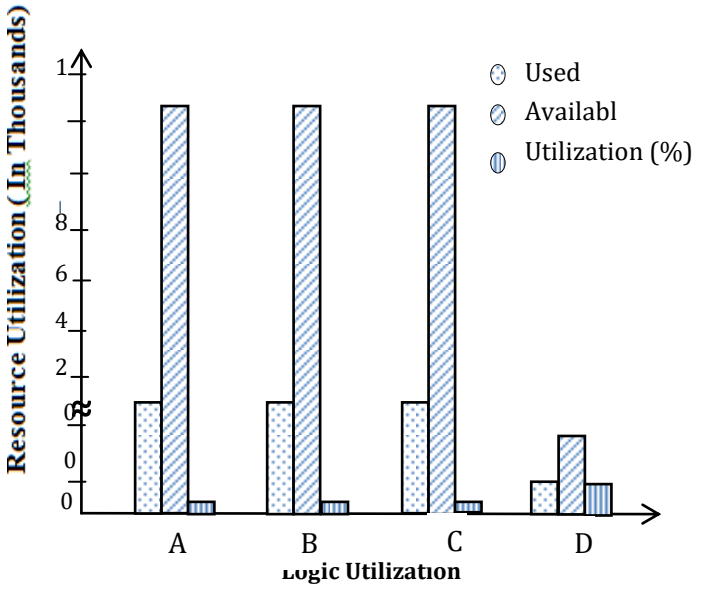

Fig – 10: Area Comparisons of Wallace Compressor 32-Bit Vedic Multipliers

4.2 Comparative Analysis

The three different multiplications 8, 16 and 32-bit perform by using 4:2 compressors and Wallace compressor Vedic multiplier is compared for time delay and area obtained from resource utilization.

4.2.1 Comparative Analysis for Resource Utilization of Different Multiplier

Table 4.3 and 4.4 provides comparison of resource utilization using three multipliers required in designing of 4:2 Compressor and Wallace Compressor respectively. The maximum path delay for 8-bit multiplier observed to be 10ns while for 16-bit and 32-bit bit multiplier it observed to be 16 and 18ns respectively. These conclude that as number of bits increases, path delay reduces. Hence at higher bit multiplier get minimum path delay compared to lower bit multiplier. After referring previous algorithm it is observed that our propose algorithm requires minimum path delay.

Table 4.3: Comparative Analysis for Resource Utilization for 4:2 Compressor Multipliers

Parameters	Multiplier		
	8-Bit	16-Bit	32-Bit
Number used as logic	124	659	2330
Number of Slice LUTs	124	659	2330
Number of IOs	32	64	128
Maximum path delay(ns)	10	16	18

Table 4.4: Comparative Analysis for Resource Utilization for Wallace Multiplier

Parameters	Multiplier		
	8 Bit	16 Bit	32 Bit
Number used as logic	98.0	432.0	1560.0
Number of Slice LUTs	98.0	432.0	1560.0
Number of IOs	32.0	64.0	128.0
Maximum path delay(ns)	10.9	15.8	18.8

Delay is the main constituent factor in any design that decides the performance of the system. For efficient system delay should as minimum as possible. Table 4.5 provides the comparative analysis of time for 4:2 compressor multiplier and Wallace tree Multiplier. It indicate that 4:2 compressor Vedic multipliers requires more time for operation due to more number of gates that of Wallace tree Vedic multiplier.

The designs of 32x32 bits Vedic multiplier have been design on Xilinx 13.2(vertex 7). The computation delay for 32x32 bits 4:2 compressor Vedic multiplier was 15.83 ns and for 32x32 bits Wallace tree Vedic multiplier were 12.71ns. It is therefore seen that the Wallace tree Vedic multipliers are faster than the 4:2 compressor. For vertex 5 the computation delay for 32x32 bits 4:2 compressor Vedic multiplier was 18.71ns and for 32x32 bits Wallace tree Vedic multiplier were 18.80ns. The Figure 11 shows comparative analyses for 4:2 and Wallace compressor 32-bit multiplier.

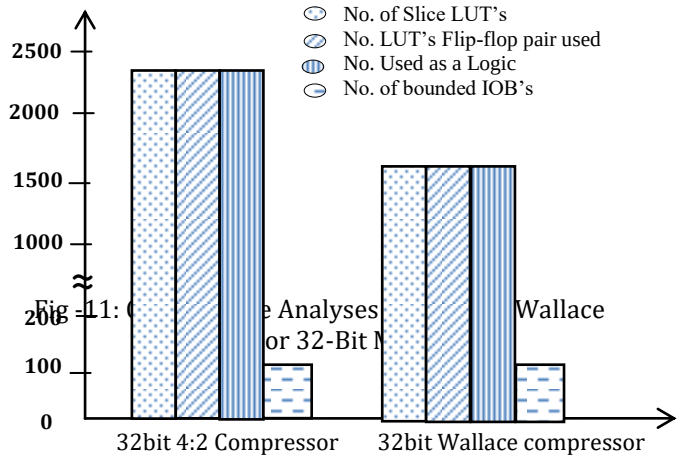

Fig -11: Analyses Wallace or 32-Bit M

Table 4.5: Comparative Analysis for 4:2 Compressor and Wallace Tree 32-Bit Multiplier

Parameters	32-Bit 4:2 Compressor Multiplier	32-Bit Wallace Compressor Multiplier
Number of Slices LUTs	2374.00	1560.00
Total Number of Path	15675988.00	7807402.00
Total Time Delay(ns)	18.71	18.80
Total Memory use(KB)	524600.00	531768.00

4.3 Experimental Result

Design of Vedic multiplier by using 4:2 compressor and Wallace compressor with their experimental result as follows.

4.3.1 Result of 4:2 Compressor Vedic Multipliers

The 32x32 bits Vedic multiplier has been design using Xilinx 13.2. The timing waveform of 16X16 bit,4:2 compressor Vedic multiplier is as shown in figure 12 which represent output obtained from various input vector provided in the test bench program during simulation. It has two inputs in1 and in2 and one outputs p. Figure 12 shows Timing Waveform for 4:2 compressor Vedic multipliers

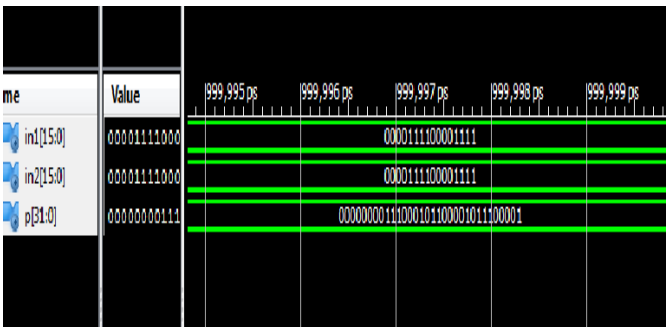

Fig-12: Timing Waveform for 4:2 compressor Vedic multipliers

4.3.2 Result of Wallace Compressor Vedic Multiplier

The 32x32 bits Vedic multiplier has been Design using Xilinx 13.2. The timing waveform of 32X32 bit Wallace compressor Vedic multiplier is as shown in figure 13 which represent output obtained from various input vector provided in the test bench program during simulation. It has two inputs in1 and in2 and one outputs p. The figure 13 shows Timing Waveform for 32-bit Wallace Compressor Vedic Multiplier

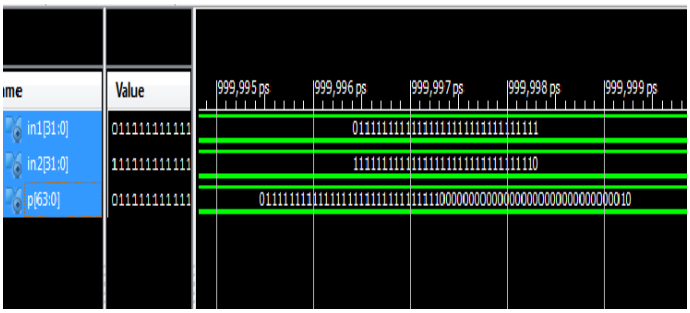

Fig -13: Timing Waveform for 32-Bit Wallace Compressor Vedic Multiplier

5. CONCLUSION

In this paper, a modified compressor based multiplier was constructed that uses Vedic mathematics to get a high speed multiplication operation.

The designs of 16x16 bits and 32x32 bits Vedic multiplier have been Design on Xilinx 13.2(vertex 7). The computation delay for 8x8 bits multiplier was 5.02ns, the computation delay for 16x16 bits multiplier was 9.09ns. The computation delay for 32x32 bits 4:2 compressor Vedic multiplier was 15.8 ns and for 32x32 bits Wallace tree Vedic multiplier was 12.7ns. It is therefore seen that the Wallace tree Vedic multiplier observed to be faster than the 4:2 compressor Vedic multiplier. For vertex 5 the computation delay for 32x32 bits 4:2 compressor Vedic multiplier was 18.71ns and for 32x32 bits Wallace tree Vedic multiplier were 18.80ns.

Urdhvatiryakbhyam, Nikhilam and Anurupye sutras used in proposed algorithm results in minimum delay, power and hardware requirements for multiplication of numbers. Use of a compressor observed to be easy processing element with less complexity which used in digital logic design for compression of data.

High speed realization multiplier with less area consumption has become more demanding over the years. Moreover, compression processing to multiplier being applied to increase the effective throughput. Delay and area observed to be constituent factors in VLSI design that limits the performance of any processor and multiplier which tends to be crucial elements that decides requirement of these factors. Working on less time delay consider as very essential requirement in many applications.

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