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A BRIEF REVIEW OF DESIGN OF HIGH SPEED LOW POWER AREA EFFICIENT MULTIPLIERS

M. AYEESHA NASREEN

ASSISTANT PROFESSOR, ECE, PALLAVAN COLLEGE OF ENGINEERING, TAMILNADU, INDIA

Abstract - *Multipliers are the major block of Digital Signal Processor, FIR filters and microprocessor. This paper discuss about various multipliers such as array multiplier, Wallace tree multiplier using optimized computing technique such as Vedic Multiplication, Partitioning Carry Select adder Algorithm and compare their performance based on parameters such as Delay, Area and Speed. Initially the array multiplier uses Shift and Add method, Partial Guarded method, temporal tilling method and Wallace multiplier uses fast parallel multiplying schemes. This proposed computing techniques will give high throughput, consume less area and power than this existing computing techniques. A new technique approximate computing of partial products is used in error tolerant applications such as data mining and multimedia signal processing to reduce complexity and increase efficiency.*

Key Words: Array Multiplier, Partitioning Carry Select Adder, Approximate Computing, Vedic Multiplication, Temporal Tilling, Parallel Multiplying Scheme.

1. INTRODUCTION

Multiplier is an important component of various processors. A customer needs a faster device with low power consumption and high speed. In digital circuits multipliers consume most of the power and if optimized multiplier is not used it will produce lag. There are different multipliers with different optimization techniques to get better performance. For some operations exact computing units are not needed. In such cases approximation techniques are used. It focuses on accumulation of partial products. This proposed multiplier can save few adder circuits.

1.1 Array Multiplier

Array multiplier performs multiplication of two numbers by shift and adds method. For a large word length it delays become very large. Using a new architecture dual array tree structure, the speed of the multiplier is increased twice that of the conventional array multiplier, the dual array structure is a regular structure consumes 30% larger silicon area. Though, array multiplier is regular due to its high power consumption, Partially Guarded Computation technique is used. This technique divides the adder and multiplier as two parts and allows only a certain part to perform the function while disabling the other parts, the switching activity is reduced, Which reduces the power consumption and area overhead. A low power array multiplier technique using temporal tilling which is a structure with higher throughput and found out that the multiplier performance has been increased.

1.2 Wallace Multiplier

In Wallace tree multiplier the sequential adding stages is reduced by a new fast parallel multiplying scheme to reduce partial product accumulation. In a modified Wallace tree multiplier half adders used in the reduction phase are reduced, instead very few full adders are used.

2. COMPUTING TECHNIQUES

In this paper we discuss about various computing techniques such as Vedic multiplication, Partitioning carry select adder algorithm and approximate computing techniques.

2.1 Vedic Multiplication

Vedic multiplication uses sutras such as 'URDHVA – TIRYAKBYHAM'. Consider a basic multiplication of 2-3 digit numbers using a line diagram [3].

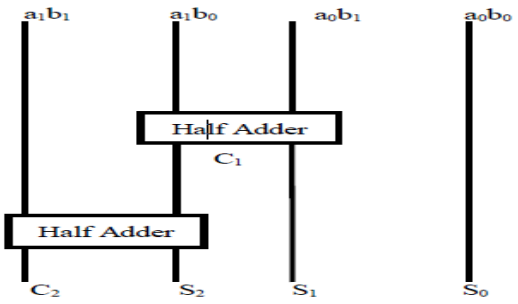

Fig -1: 2 bit Vedic Multiplier

In this method, digits on both sides of the lines are multiplied and the carry from the previous step is added, in this step one bit of the result and carry is generated. This carry is added to the next step and the process repeated. All the results are added to the previous carry.

When more than one line is there in one step, LSB generated in each step is considered as the result bit and rest of all bits are carry bits for the next step.

2.2 Partitioning Carry Select Adder Algorithm

In this architecture inputs are encoded into booth equivalent and a Wallace tree is used to optimize the partial products. The partial products are then added by a carry select algorithm, the carry select adder is partitioned into no of blocks, so the overall delay is minimized. This algorithm is used in Booth Encoded Wallace Tree Multiplier. Table 1 shows the delay comparison of various 32 bit multiplier in nanoseconds [2], Booth Recorded Wallace multiplier have the lowest delay while array multiplier have the highest delay. According to the experimental results the architecture of Booth Encoded Wallace tree multiplier have an average of 9.12% less delay and with less than 1% overhead.

Table -1: Delay in multipliers

	DELAY IN NS
Array multiplier	72.986
Wallace multiplier	53.198
Bypassing multiplier	62.520
Booth multiplier	55.700
Optimized Vedic multiplier	31.834
Booth Wallace multiplier (radix 2 with CLA)	28.600

2.3 Approximate Computing

To reduce complexity and increase efficiency in multimedia signal processing and data mining where exact computing units are not necessary and for error tolerant applications approximate computing multipliers are used, to reduce hardware complexity, truncation is widely employed in fixed width multiplier design [1]. The quantization error introduced by the truncated part is compensated by adding a constant or variable correction term. The implementation of this multiplier has three steps: Partial Product Generation, Partial Product reduction tree, a vector merge addition. From the sum and carry rows generated from the reduction tree a vector merge addition is performed and final product is produced. Mean relative error figures are as low as 7.6% and 0.02% for the proposed approximate multipliers, which are better than the previous works [1].

3. CONCLUSIONS

In this paper a review of various multipliers and their computing techniques were presented, among this multipliers Booth recorded Wallace tree multiplier is found to be 67% faster than Wallace tree multiplier, 53% faster than Vedic multiplier and 22% faster than radix 8 booth multiplier. Approximate Computing technique used in error tolerant application achieve power saving of 72% and 38% in two proposed multipliers compare to exact multiplier. Precision is better and mean relative error figures are low. Approximate computing gives highest peak signal to noise ratio.

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