International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 07 | July -2017 www.irjet.net p-ISSN: 2395-0072

Review on Tunnel Field Effect Transistors (TFET)

Prabhat Tamak[1], Rajesh Mehra[2]

[1]ME Scholar, [2]Associate Professor
[1,2]Department of ECE, NITTTR Chandigarh

Abstract - *The low consumption of power is depends upon lowering of voltage supply. In case of MOSFET (Metal Oxide Semiconductor Field Effect Transistor), reduction in supply voltage slow down the sub threshold swing which cannot be lowered by 60mv/decade. The down scaling of MOSFET increase the consumption of power (static and dynamic are two types of power consumption), out of which static power becomes too high. So, for low power consumption, high energy efficiency of circuit and small swing switch, TFET (Tunnel Field Effect Transistors) is promising alternative to MOSFET because it is a p-i-n diode whose tunnel current flows in between the bands of source and channel, that's why, these devices are very useful for the low power application due to their low value of leakage current and sub threshold swing. The only difference between TFET and MOSFET is switching mechanism, TFET based on band to band tunnel mechanism where as MOSFET mechanism is thermionic emission. In this paper, the various types of TFET are described which are available for design from initial stage to till today.*

***Key Words*: BTBT, MOSFET, Hetro-junction, Tunnel Field Effect Transistor, Sub threshold swing (SS), low voltage operating transistor**.

1. INTRODUCTION

CMOS (Complementary Metal Oxide Semiconductor) is most popular switch used in semiconductor devices and it is due to reason because it provides possibility of increase in drive current and cut-off frequency with down scaling of semiconductor device. Scaling of CMOS based on Moore's law which was given by G. Moore and predicts that in every 24 month, transistor present on a chip would double. But in recent years, the dimension of CMOS reached to nanometer where the management of power becomes the difficult for further scaling of MOSFET give rise to number of issues such as gate tunnel current, source/drain to channel, coupling and parasitic effects and short channel effects includes the drain induced barrier lowering, high leakage current and low value of ON to OFF current ratio [1]. So, to overcome these problems a new device TFET is come which is alternative for MOSFET. Tunnel transistors have been evolved in 1992 by T. Baba. Some of characteristics of TFET are as follows:

(i)Exhibits Sub threshold slope lower than 60mv/decade.
(ii) Used for low power applications.
(iii) BTBT mechanism used which reduces the leakage current.
iv) High ON to OFF current ratio.
v) Reduction in Short channel effects.

In particulars, we want devices which is similar to the field effect transistor (FET), in which tunneling current flow due to change in gate voltage, and, used the band to band tunnel mechanism in the ON state and in alteration between OFF and ON state[1]. The potential of this device to achieve the less OFF state current and low value of sub threshold swing beyond the 60mv/decade which is the bound for conventional MOSFET [2].

2. Literature Review

The short channel effects, velocity saturation, drain induced barrier lowering are the problems which are existing with MOSFET as scaling is done which limits the sub-threshold slope of MOSFET to 60mv/decade. In MOSFET channel length (L), channel width (w), gate oxide thickness (T_{ox}), depth of source/ drain junction and voltage are scaled by 1/k factor and channel doping concentration is by k where k is constant. When the above mention scaling factors are applied to drain current equation, and then drain current scaled by 1/k factor, which is given by

$$I_D = \frac{wuC_{ox}\left(V_G - V_{th}\right)^2}{2L} \qquad (1)$$

Where V_G is gate voltage, V_{th} is threshold voltage, C_{ox} is capacitance of unit area and μ is mobility of carrier. The scaling done in this way is known as R. Dennard scaling. Figure1 explains that Dennard scaling is not suitable for modern devices due to non-linear curve is in between the V_{DD} (supply voltage) and V_T (threshold voltage) as the length of channel reduced below 0.35μm [3].

It is clear from graph, when supply voltage decrease by some value, threshold value becomes half of starting value. For the modern technology the most important feature for scaling is to maintain gate overdrive voltage (V_{GS}-V_T or V_{DD}-V_T) constant. When gate overdrive voltage is decrease, ON current is decrease which negatively affect the ratio of ON and OFF current and dynamic speed [4].

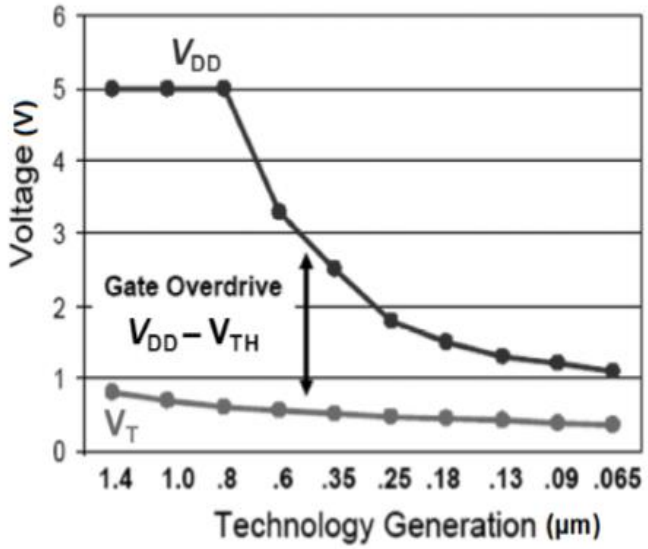

Fig-1: Trends of voltage v/s technology Generation [5]

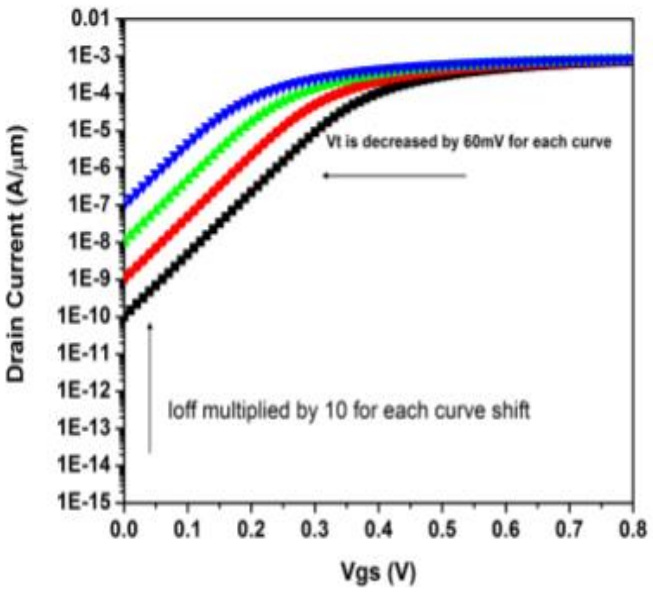

Fig-2: MOSFET Transfer characteristics with reduction in V_T [5]

It is clear from graph, when supply voltage decrease by some value, threshold value becomes half of starting value. For the modern technology the most important feature for scaling is to maintain gate overdrive voltage (V_{GS}-V_T or V_{DD}-V_T) constant. When gate overdrive voltage is decrease, ON current is decrease which negatively affect the ratio of ON and OFF current and dynamic speed [4]. Two possible solutions for high ON current is to (a) Increase in V_{DD}: With increase in V_{DD}, dynamic and static power consumption is increase because $P_{dynamic} = fC_L(V_{DD})^2$, $P_{static} = I_{leakage}V_{DD}$; where f is frequency operation, C_L is capacitive load and $I_{leakage}$ is the current when device is in OFF state.(b) Reduce in V_T: With reduction in V_T, OFF current is increase by 10 times which results in high leakage power as shown in Figure2. As the technology is shrinking today, the number of transistor per unit chip area increase which increase the leakage power and this leads to the standby power consumption in electronic devices. So, these are not the proper solution to problems mention above.

In order to overcome above challenges to the continued scaling of transistor, literature has proposed the new device known as TFET (Tunnel FET). TFET that has been evolved in 1992 by T.Baba, as one of promising alternative to the conventional MOSFET based on the various parameters and the advantage of TFET is low sub threshold current which leads to low leakage per device with high ON and OFF current ratio which is suitable for digital circuits and memory.

TFET based circuits are highly energy efficient and regarded as a green transistor. Tunnel FETs are interesting as low-power devices because of their quantum tunneling barrier. TFET provides low value of total energy at low supply voltage [6].

3. TFET Structure and Operation

The basic Structure of TFET is very similar to the MOSFET except that source and drain terminal are doped with opposite type and the most distinguish characteristics of TFET is the doping used for drain and source. A common TFET device structure consists of a P-I-N (p-type, intrinsic, n-type) junction, in which the electrostatic potential of the intrinsic region is controlled by a gate terminal and it is working under the condition of reverse bias [6]. Thermal injection is a mechanism for the source of carrier injection used in MOSFET but TFET utilize the BTBT as mechanism of source carrier. TFET basic structure consist three parts (Source, Gate and Drain). Source terminal is used as a source of majority carrier, Drain terminal is used to carry out the majority carrier and Gate terminal is used to controls the majority carrier moving from source to drain indirectly controls the drain current (Drain current depends on number of majority carrier reaching to drain). Channel is formed between the p-type and n-type region. Gate Oxide is used insulate the gate and to enable gate to control the electrostatic in the channel and oxide is insulator, gate oxide prevents the current leakage from channel to gate [7].

TFET belong from the family of abrupt slope device that are currently under the investigation for application that can be used for very low power. The critical quality of TFET is Sub-

threshold Slope (SS) lower the edge of 60mv/decade for Field Effect Transistor (FET) which is crucial for low power application. The structure of TFET consist a p-i-n diode, working under condition of reverse bias. The Thermal injection is a source of carrier injection mechanism in MOSFET but mechanism used by a Tunnel FET is band-to-band tunneling (BTBT) for injection of source carrier. In the OFF state, a large barrier potential is present between the channel and source, consequently tunneling in this not exists but the small leakage current exists [8]. When a voltage of gate (V_G) exceeds the voltage of threshold (V_T), barrier potential exists between the channel and source become contracted so that tunneling current can flow, it is known as the ON state for Tunnel FET. Due to use of different mechanism for injection of source carrier, Tunnel FET is present as comparable device to MOSFET, which is useful in achieving sub threshold slope below 60-mV/decade. TFET transmission probability is calculated using the Wentzel Kramers Brillouin (WKB) approximation:

$$T_{wkb} \approx \left[\frac{4\lambda\sqrt{2mE_g^3}}{3qh\left[E_q + \Delta\Phi \right]} \right] \qquad (2)$$

'm' is effective mass and E_g is band gap, λ is the screening tunnel length and describe extent of the transition region at the source-channel interface [9].

4. Different Structures of TFET

Based on the structure, TFETs can be broadly divided into two categories: planar and three dimensional structure. A planar TFET is a device in which current carrying surface is planar. This device can be made on a bulk Silicon wafer or on an SOI wafer. For better gate control over the channel, SOI TFETs are preffered over bulk TFETs. Surface Tunnel Transistor is first tunnel transistor deals with speed, power and IOFF/ION ratioThen first TFET basic p-i-n structure is invented which deals with speed, power, IOFF/ION, tuning range etc. After that feedback TFET, p-n-i-n TFET, NEMFET, Raised Buried Oxide TFET, Junctionless TFET, Double gate TFET (DG-TFET), Vertical TFET, Dopingless PNPN TFET are studied [10]. Along with these different structures of TFET DG-TFET and Dopingless PNPN TFET shows superior performance than other studied.

(i) Surface Tunnel Transistors

Surface Tunnel Transisitors was the first type of tunnel transisitors which consist the p-i-n diode strucutre with gate present over the intrinsic region. The device is fabricated with a different type of material on source and drain to study the charactersics of new device. The transfer characterstics of Surface Tunnel Transisitor exhibit the action of transisitor without saturaton which is similar to the operation of vaccum triode [11].

(ii) p-i-n structure TFET

It consists of a thin layer of grown on layer of buried oxide on substrate of silicon. The gate oxide is grown on silicon layer followed by deposition of source, drain and gate contacts. Source and Drain are formed by appropriate doping in silicon layer. In SOI TFET, the entire Silicon layer is depleted and buried oxide layer blocks all source to drain leakage path. It provides a better gate control over the channel because drain-body and source-body depletion region are small [12]. This also leads smaller source/drain to substrate capacitance.

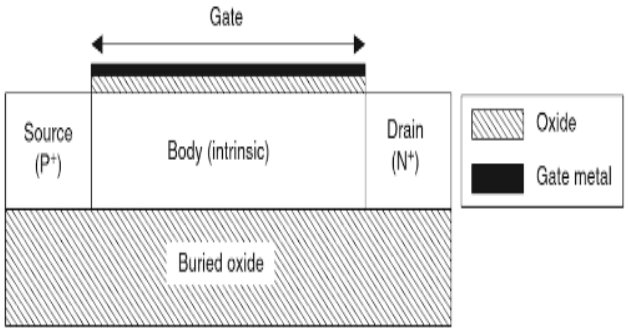

Fig-3: Schematic of a p-channel p-i-n TFET [12]

(iii) Feedback TFET

The main aim to design the feedback TFET is to achieve the steep sub threshold swing which defines the switching speed of device. It consist a gated side walls around the source and drain junction for the purpose of energy barrier. When a positive supply voltage is applied to gate at drain and source junction then some charge carriers get trapped at junction which lowers the potential of charge carriers and due to this barrier height get reduced which helps in providing the steeper sub threshold [13].

(iv) Raised Buried Oxide Tunnel FET

Raised buried oxide Tunnel FET is designed to enhance the ON current by using hetro- gate oxide and Silicon on Insulator with a raised buried oxide in drain to reduce the Miller's effect and to fulfill the requirements of ITRS [14]. This structure helps in improving the ON current, OFF current, ratio of ON to OFF current, steep sub threshold and reduced Miller's effect. It is achieved by using the low energy band gap material which helps in improving the tunneling probability.

(v) Junction- less TFET

The proposed Junction- less TFET is Silicon-channel heavily n-type-doped with different isolated gate (Control-Gate, P-Gate) and with different work-function. This is because of Junction- less TFET should be similar to conventional TFET

and the sub threshold swing of TFETs is lower than 60mV/decade. These are actually quantum mechanical devices which are based on band-to-band tunneling (BTBT) principle. These TFETs has higher electrical performance but lower variability than conventional MOSFET and this happens due to absence of p-n junctions. Junction-less TFET is attractive because of better tunneling current and lower band-gap hetero structure channel [15].

Asymmetric Junction-less are used for efficient ON-OFF switching, source and drain are optimized by using the asymmetric junction-less source-body region and junction drain-body region separately. Due to n drain- p+ body junction, the off-state tunnel barrier can be extended into the drain. Therefore, Asymmetric Junction-less TFET is an alternative approach for sub-10nm region [16].

(vi) Double Gate TFET

It consist the two gates in structure, one at the top (called front gate) and other at bottom (called back gate). This improves electrostatic control of gate on the channel because field lines terminate from back gate rather than terminating in the channel. The ON- current is increase because there are two channels from which current can flow. As the Doping concentration of source cannot be increased arbitrary because as we increase in doping concentration it raises Fermi level into CB, helps to reduce filtering effect presents on Fermi level within TFET and degraded sub threshold swing [19].

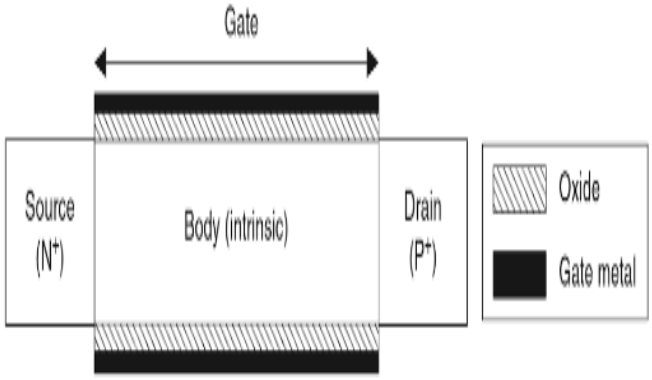

Fig-4: Schematic of p-channel Double Gate TFET [19]

(viii) Dual Material Gate (DMG) TFET

This is an important variation in structure of TFET, consist two gates with different work function along the length of channel. One gate covers the path near the source region and others cover the part near the drain region. Gate near the source region is known as tunneling gate, in this tunneling occurs at source-channel junction and other gate near the drain region is called as Auxiliary gate. Dual Material Gate structure is fabricated using sidewall spacer technique. Single Material Gate (SMG) has a high work function (4.8ev) consist more ON-current than the Single Material Gate with lower work function (4.4ev). With a high work function we can achieve higher ON-current which is correspondingly accompanied by high OFF-current which leads high Sub Threshold Swing and Power dissipation [20].

Dual Material Gate is able to combine the benefits of Single Material Gate with higher and lower work function; therefore, it provides the high ON-current equivalent to the Single Material Gate with higher work function (4.8ev) and low OFF-current which is equivalent to the Single Material Gate with lower work function (4.4ev). So, Dual Material Gate is able to provide Higher ON- current and high Sub threshold swing Slope. It has a lower Drain Induced Barrier Lowering (DIBL) effects when channel under the auxiliary gate has a high resistance which reduces the potential drop and also protects it from variation in drain bias [20].

(viii) Hetero-junction TFET

In Hetro-junction TFET, material used to make the source and drain region are of different types due to which it provides the higher tunneling current as comparison with homo junction. A Hetro-junction TFET device structure consists of a P-I-N (p-type, intrinsic, n-type) junction, in which the electrostatic potential of the intrinsic region is controlled by a gate terminal and it is working under the condition of reverse bias. Thermal injection is a mechanism for the source of carrier injection used in MOSFET but TFET utilize the BTBT as mechanism of source carrier. Hetro-junction TFET basic structure shown consist three parts (Source, Gate and Drain) [21].

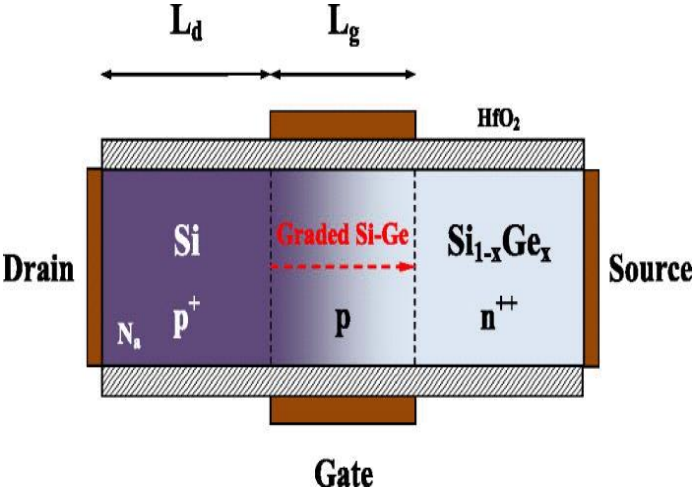

Fig-8: Structure of Hetero-junction TFET [21]

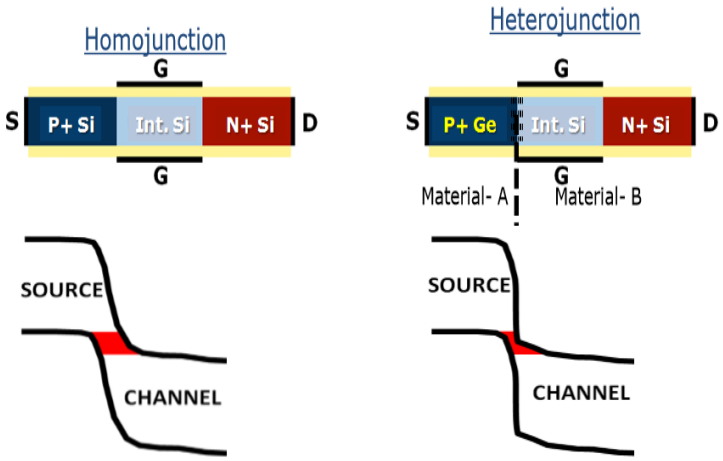

Fig-9: Tunneling Current with Homo and Hetro-junction

5. CONCLUSION

In this paper, Tunnel FET provides the better performance in comparison with MOSFET and different structures if TFET is explained. The limitations faced by CMOS: The motivation for small swing switches goes back to the scaling of conventional MOSFETs, and the continuing increase in their static power consumption. It explained that the leakage power increase comes from scaling down dimensions without scaling down the supply voltage, and from trying to keep gate overdrive high by reducing threshold voltage through shifting I_{DS}-V_{GS} characteristics and thus increasing I_{off}. Small swing device: TFET belongs to devices which have the small swing in sub threshold region. The sharp sub-threshold swing of TFETs results in a low I_{OFF} and high I_{ON} and hence, a higher ratio of ON and OFF current. TFET is extremely scalable and offers a solution to challenges proposed by aggressive scaling. For performance enhancement, the following approaches can be considered: gate oxide and SOI layer thickness reduction, lower band gap channel material, abrupt source doping profile and improvement in fabrication process. Due to performance enhancement, TFET is more compatible to use for the power applications.

REFERENCES

[1] Alan Seabaugh, "Quantaum Tunneling is a limitation in today's transistors, but could be the key to future devices", IEEE Spectrum, pp. 756-761, September 2013.

[2] Neha Thapa, Lalit Maurya, Rajesh Mehra, "Performance advancement of high-k dielectric MOSFET", International Journal of Innovations and Advancement in Computer Science, Vol. 3, Issue 3, pp. 98-103, May 2014.

[3] Aswathy, M., Nitha M. Biju, and Rama Komaragiri., "Comparison of a 30nm Tunnel Field Effect Transistor and CMOS Inverter Characteristics," 3rd International Conference on Advances in Computing and Communications, Cochin, pp 149-152, Aug. 2013.

[4] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions," IEEE Journal Solid-State Circuits, vol. 9, no. 5, pp. 256268, October 1974.

[5] Deepak Kumar's M. TECH thesis, "Tunnel FETs and Its Application to Digital Circuits," Indian Institute of Technology, Kanpur, pp. 1-4, June 2015.

[6] Peter Nilsson, "Arithmetic Reduction of the Static Power Consumption in Nanoscale CMOS," 13th IEEE International Conference on Electronics, Circuits and Systems, pp. 656-659, 10-13 December 2006.

[7] Adrian M. Ionescu and Heike Riel, "Tunnel Field Effect transistors as energy efficient electronic switches", Nature, pp.. 329-337, November 2011.

[8] Benton H. Calhoun and Anantha Chandrakasan, "Characterizing and Modelling Minimum Energy Operation for Subthreshold Circuits," International Symposium Low Power Electronics and Design, pp 90-95, August 2004.

[9] Thomas Nirschl, Stephan Henzler, Christian Pacha, Peng-Fei Wang, Walter Hansch, Georg Georgakos and Dons Schmitt-Landsiedel, "The Tunneling Field Effect Transistor (TFET) used in a Single-EventUpset (SEU) insensitive 6 transistor SRAM cell in ultra-low voltage applications," 4th IEEE Conference on Nanotechnology, pp 402-405, 2004.

[10] Book: S. M. Sze, "Physics of Semiconductor Devices," 2nd edition , John Wiley and Sons, Inc.,pp 96-102, 1981.

[11] Satish M Turkane and A. K. Kureshi, "Review of Tunnel Field Effect Transistor (TFET) ", International Journal of Applied Engineering Research, Vol. 11, N0. 7, pp. 4922-4929, 2016.

[12] Q. Zhang. "Low-Subthreshold-Swing Tunnel Transistors," IEEE Electron Device Letters, April 2006.

[13] T. Baba, "Proposal for Surface Tunnel Transistors," Japanese Journal of Applied Physics, Vol. 31, no. 4, pp. L455-L457, 1992.

[14] T. Uemura and T. Baba, "Direct Gate-controlled NDR Characteristics in Surface Tunnel Transistor," IEEE, pp. 456-458, 1996.

[15] Uygar E. Avci, Danirl H. Morris and Ian A. Young. "Tunnel Field-Effect Transistors: Prospects and Challenges", Journal of Electron Device Society, Vol. 3, No. 3, pp. 88-95, May 2015.

[16] W. Choi, B. G. Park, J. D. Lee and T. J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec", IEEE Electron Device Letter, Vol. 28, No. 8, pp. 743–745, August 2007.

[17] A.Maria Jossy, T.Vigneswaran, "A Perspective Review of Tunnel Field Effect Transistor with Steeper Switching Behavior and Low off Current (I_{OFF}) for Ultra Low Power Applications", International Journal of

Engineering and Technology (IJET) , Vol. 6, No. 5, pp. 2092-2104 , Oct-Nov 2014.

[18] Luca De Michielis, Livio Lattanzio and Adrian M. Ionescu,"Understanding the Superlinear Onset of Tunnel-FET Output Characteristic ", IEEE Electron Device Letters, Vol. 33, No. 11, pp. 1523-1525, November 2012 .

[19] Book: Sneh Saurabh, Mamidala Jagadesh Kumar, "Fundamentals of Tunnel Field- Effect Transisitor", pp. 52-72, 2nd edition, CRC Press ,2017

[20] Jagadesh Kumar Mamidala, Rajat Vishnoi and Pratayush Pandey, "Tunnel Field Effect Transistors: Modelling and Simulation " 1st edition, Wiley Press, pp. 63-68, 2017.

[21] S.H.Kim, H.Kam, C.Hu, and T.-J.K.Liu, "Ge-Source Tunnel Field Effect Transistors with Record High I_{ON}/I_{OFF}", VLSI Symposium Technical Digest, pp. 178–179, 2009.

[22] Gaurav Gupta, Rajesh Mehra, "MOSFET sub-threshold current reduction by varying substrate doping", IEEE International Conference on Advanced Communication Control and Computing Technologies, pp. 551-554, 2014.

[23] Anju Devi, Lalit Maurya, Rajesh Mehra, "Temperature Variation Effects in Si/Ge based MOSFET, Hybrid MOSFET and SiGe MOSFET on simulation study", International Journal of Innovations and Advancement in Computer Science, Vol. 3, Issue 3, pp. 67-72, May 2014.

[24] Mallikaarjunarao, Rajeev Ranjan, K.P.Pradhan and P.K.Sahu, "Dielectric engineered symmetric underlap double gate tunnel FET (DGTFET):An investigation towards variation of dielectric materials" Elsevier Super lattices and Microstructures, pp. 226-233, 2016.