International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 04 Issue: 07 | July -2017 www.irjet.net p-ISSN: 2395-0072

A survey on architectural modifications for improving performances of devices using FINFET techniques

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Abstract - *This survey paper presents the analysis of FinFET (Fin-type Field-Effect Transistors) based on their performances. FinFETs are promising substitutes for bulk complementary metal oxide semiconductor beyond 22nm level. FinFETs are dual-gate devices. The two gates of a FinFET can either be connected together or independently controlled for lower leakage or reduced transistor count. The main objective of this survey is to make engineers and researchers to get benefited into the techniques for civilizing performances in terms of power, speed and area and motivate them to develop good solutions for enabling low-power process.*

Key Words: body effect, soft error, process variation control, Read Static Noise Margin (RSNM), Asymmetric gate work function.

1. INTRODUCTION

The FinFET device consists of a thin silicon body, the thickness of which is denoted by t_{si}, enclosed by gate electrodes. The direction of current flow is parallel to the wafer plane, here the channel is formed which is perpendicular to the plane of the wafer. Due to this reason, the device is termed quasi-planar [1]. Figure 1 gives you an idea about the design of a multi-fin FinFET.

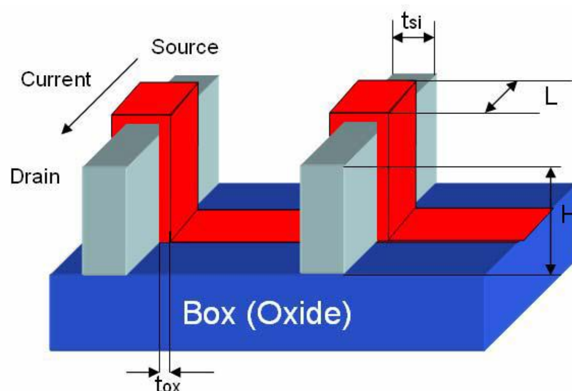

Fig.1 multi-fin FinFET

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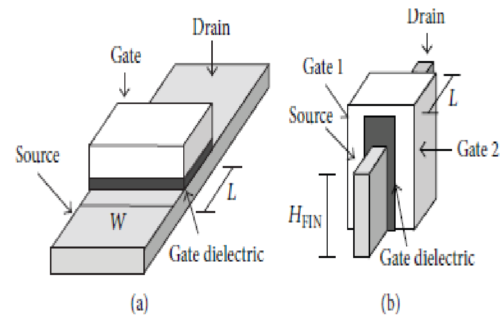

Fig.2.a) shorted gate b) independent gate

In shorted-gate (SG) FinFETs, both the gates are combined together, form a three-terminal device. This device can serve as a direct substitute for the conventional bulk-CMOS devices. In Independent-Gate (IG) FinFETs, the two gates are not connected together, it can be controlled separately [1]. E.J.Nowak et al.[2] have presented paper on double gate CMOS/FinFET Technology which describes FinFET device only sub threshold drain to source tunneling is significant while gate oxide tunneling and drain/source to body conduction are substantially reduced.

1.1 REDUCTION OF SHORT CHANNEL EFFECTS USING FinFETs

FinFETs gives better manage of short-channel effects and also promising alternative for the 22nm technology node and beyond. The lightly doped channel of FinFET improves its resistance to process variations [2].If FinFET back gate is reverse biased, it increases the threshold voltage (V_{th}) of front gate, thus reducing leakage at the rate of increased delay [3].If FinFET back gate is reverse biased, it increases the V_{th} of front gate, thus reducing leakage at the expense of increased delay. Unlike planner devices, a FinFET does not suffer from random do pant fluctuations due to its lightly doped channel. And also variations in the work functions of an n-FinFET &p-FinFET alter the V_{th}. The ratio between the leakage &dynamic power of a circuit can vary drastically depending on the operating temperature [4]. The slew rate of op-amp is significantly improved 273 to 5590 v/μs using FinFET & operational Tran's conductance amplifier. The gain and phase margin remain unchanged [6].Double Gate (DG)

MOSFET is to be the best for the device down scaling as it allows significant reduction of short-channel effects. The threshold voltage role-off decreases as the fin height decreases. In nano scale FinFET have short channel effects are eliminated significantly when the fin width is less than the fin height [8].

Doped FinFETs retain a variability advantage over conventional planar technology, if the channel doping is lower than a few $10^{18}/cm^3$[9].

The new Body-on-insulator FinFET can suppress the source/drain leakage beneath the channel region; it can maintain low S/D parasitic resistance and good heat dissipation capability, this device shows an effective suppression of the leakage current and excellent immunity to short-channel effects [12]. M.Nawaz et al. [35] have shown that the bulk FinFETs were approximately independent of back bias effect, with identical fin geometry bulk FinFETs and anti-punch implant shown the same Ion-Ioff behavior and approximately equal short channel effect like SOI (Silicon On Insulator) FinFETs.

1.2 IMPROVEMENTS IN POWER AND AREA MINIMIZATION

FinFET logic circuits achieve significant area and power reduction without voltage or transistor scaling even though they suffer greatly in circuit speed [14]. FinFET based processors allows lead to large spreads in delay & leakage under PVT(Process, Supply Voltage, Temperature)variations [15].Multi threshold voltage FinFET sequential circuit effective in reducing the power consumption under process parameter variations [16].

Feng Wang et al. [17] and it has been shown that FinFET circuits have better soft error immunity, and it has less vulnerable to process variation, FinFET-based circuit designs are much robust than the bulk CMOS counterparts.

Michael A.Turi et al. [26] have proposed a promising scheme of SG-high precharge swing scheme, it had some of the features delay was 48.1% and 59.9 % (less than the minimum low power scheme). Temperature has an exponential effect on leakage current and small effect on dynamic current.

2. ARCHITECTURE MODIFICATION FOR IMPROVING PERFORMANCES

Ting-Jung Lin et al. [19] have designed a Fine-grain Dynamically Reconfigurable 2.0 architecture (FDR) in that the logical elements is augmented with dedicated carry logic to facilitate arithmetic operations, The experimental result shown that the coarse-grain design can improve performance by 3.6Xcompared with the fine-grain FDR architecture, they have designed 22-nm FinFET technology, it enables more flexible and effective power management. Francesco Conzatti et al. [21] described the strain engineering in n and p type FinFETs by using strain measurements, mobility characterization and physical-based modeling. they have analyzed that the electron and hole measured mobility was found to be fairly insensitive to the fin width, then the simulation result shown that the electron mobility can be further improved by tensile strain in fin length direction, whereas the hole mobility can be increased by using a compressive strain in the same direction.

Vladimir Jovanovic et al. [23] have demonstrated the technology for ultra-high aspect ratio FinFETs on bulk silicon wafers. They have analyzed on nano scale gate length of FinFET fabrication process and reduction of source/drain series resistance would result in accessible technology well suited for high-frequency analog applications. Debajit Bhattacharya et al. [18] have presented a paper of Layout-based parasitic-aware design space exploration of FinFET content addressable memory, and also they observed that leakage power assumes slightly greater significance with a decreasing mismatch probability. Finally they observed noticeable differences in parasitic capacitance between two orthogonal layout styles (VSL &VML).

T.Rudenko et al. [24] shown that the narrow FinFET structure has reduced gate current densities compared to the quasi-planar (very wide fin) structures. This reduction was observed in both doped & undoped channel devices. M.Poljak et al. [25] have proposed a solution for the suppression of corner effects and related kink effect in wide-channel triple gate bulk FinFETs. In this method it does not require no additional masks, also they have obtained threshold voltage shift were 0.434V &0.287V. Field Enhancement of FinFET allows high program and erase speed and larger memory window, this programming and erasing characteristics must be taken into account in memory circuit design [13].

2.1 IMPROVEMENTS IN NOISE REDUCTION

Tatsuya OHGuro et al. [28] have proposed technique on fin patterning due to Side-Wall Transfer (SWT).This technique is useful to not only fabricate narrow fin line but also suppress fin width variation. The H_2 annealing after Si etching is useful for not only to improve the mobility of electron and hole but also to reduce flicker noise of FinFET. The noise in FinFET with fully depletion mode decreases which are similar to ultra thin SOI device, however FinFET has the disadvantage for RF performance due to larger gate capacitance comparing with planar MOSFET. Yiming Li and Chih-Hong Hwang [29] have analyzed 16nm bulk FinFET on the characteristics of random dopant effects. The result shown that for the same threshold voltage the immunity against fluctuation of the 16nm FinFET is superior to the planar device. It is about 2.5 times reduction.

E.Simoen et al. [30] have proposed paper on multiple-gate MOSFETs seem to yield acceptable 1/f noise levels and appear to be quite robust against floating body effect, for ultra-thin film devices, the quantization effects will become more & more important, this may also reflect in the low frequency noise behavior.

V.Subramanian et al. [31] have examined the impact geometrical parameter of fin width of FinFET devices, for fin width in the range of 25-75nm, the front gate coupling coefficient was small (~0.01), the trans conductance to-current ratio is weakly sensitive to fin widths, low frequency noise increases for narrow fins, which points to increased (1.5 times) interface trap density of fin side walls compared to the top surface.

2.2 IMPROVEMENTS OF SCALABILITY USING MULTIGATE FinFET TECHNIQUES

Romain Ritzenthaler et al. [5] have presented paper on pi-gate FETs, they described that increasing the number of gates allows a better scalability of multiple gate FET SOI devices, pi-gate FETS acting like a device with a number of gates between 3 & 4 offers increased front-gate control.

Mirko Poljak et al. [32] have shown that bulk FinFET with Source/Drain–to-body(S/D) junction shallower than gate-bottom has equal or better sub threshold performance than SOI FinFET. By reducing S/D junction depth, fin-width scaling for suppression of short-channel effects can be relaxed and bulk FinFET characteristics can be improved with no increase on process complexity &cost.

M.A. Pavanello et al. [33]analyzed the analog performances of nMOS triple-gate FinFETs with undoped body and TiN/HfO2/Sio2 gate stack using narrower FinFETs increases the early voltage with respect to wider ones when the device are operating in the onset of volume inversion. The mobility of long channel narrow FinFETs was observed to be larger than for wider ones improving the transconductance over drain current ratio in moderate inversion regime. The omission of the halo implantation improves both the carrier mobility & the early voltage for devices longer than 100nm, for FinFETs with un doped body and no halo implantation large gain devices can be achieved n-type FinFET have the potential improvements on current drive and trans conductance –to-drain current ratio than bulk.

2.3 MODELING OF ASYMMETRIC GATE WORK FUNCTION

Ajay N.Bhoj et al. [34] have evaluated Symmetric-Gate work function SG/IG-mode FinFET and Asymmetric-gate work function SG-mode FinFET head to head in a high-performance process and the result shown that Asymmetric gate work function SG-mode FinFETs with high-performance provide very steep sub threshold slopes. Ultra-low off currents and high-on currents in comparison to symmetric gate work function SG/IG-mode FinFETs. Single IG-mode device is sufficient to reduce leakage considerably without too much degradation in delay. Ajay N.Bhoj et al. [27] have shown that Asymmetric gate work function FinFET SRAM bit cells had a better dynamic write ability, Symmetric gate work function had unattractive transient characteristics.
K.Bennamance et al. [36] have found that the low field mobility was significantly degraded at small gate length in sub 100nm FinFETs and also demonstrated that the side wall mobility was about 25-30% lower as compared to the top surface conduction, the trap density in high conductivity metal gate stack has been found much larger than in pure Sio2 MOSFETS but with no further degradation at small fin widths with low frequency noise previous findings on fully depleted-SOI devices. T.Chiarella et al. [37] have developed on DOI substrates and low doped fins results in lower junction capacitance, higher mobility and voltage gain with reduced threshold voltage mismatch using an optimized integration to minimize parasitic capacitances and resistance and also they have demonstrated high-performing FinFET ring-oscillators with delays down to 10ps/stage for both SOI &bulk FinFETs.

Jaw-Juinn Horng et al. [38] have presented paper on combination structure of temperature & voltage sensor in a 16nm FinFET technology. The temperature sensor achieved 1^0C resolution over -10 ~90^oC range, the voltage sensor achieved 4mv output error over 0.38v to 0.56v. The total chip size is 0.01mm^2 and drawn 70uW total power from a 0.7V supply, depending on resolution the measurement time can change from 10μsec to 1.6ms.

2.4 SRAM based FinFETs performances

Double gate-FinFET based static random access memory reduces the soft error failure rate [7]. Lightly doped silicon fin improves the immunity to random do pant fluctuation, making a FinFET a promising candidate for subthreshold SRAM applications [10]. Ming-Long Fan et al. [11] have presented paper on FinFET and they found that 4T FinFET SRAM cell exhibits a better nominal Read static Noise margin than the conventional 6T cell. Kyoman Kang et al. [20] have proposed a differential SRAM architecture with a full swing local bit line. This architecture stores four bits in one block can achieve a minimum voltage of 0.42V and Read delay is 62.6 times lesser than that of 8T SRAM based 22nm FinFET technology. Mayank Shrivastava et al. [22] have presented paper on Implant-Free (IF) complementary metal-oxide semiconductor that gave better scalability with improved performance. The result has shown that approximately two times improvement in static random access memory and digital input/output performance.

3. CONCLUSIONS

From the results, derived in research papers, it is concluded that FinFETs are extremely fast and power efficient devices, its disadvantage being difficulties in fabricating it to perfection, being a very small device and its series resistance and extrinsic parasitic capacitance. Few papers have suggested changes in geometries, dimensions, change in materials used etc. They yielded considerable advancements in drain current, speed, threshold voltage, etc. Out of all, inclusion and change in spacers used proved a considerable improvement over others. They play a major role in deciding the parasitic capacitance of the FinFET. As there is a reduction in capacitance, they offer great performance in analog applications, in which these devices lag also, the threshold voltage is reduced because of which, power consumption too reduced. This can pose great advantage in using FinFETs for analog and high speed devices. The disadvantages of noise and low speed restricted from use of FinFET in such devices.

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