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Different leakage power reduction techniques in SRAM Circuits: A State-of-the-art Review

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Abstract - *In today's electronic devices, memory is a most important part that shares a major part of total circuit power. With the newer technology size of processing data is increasing which results in increase of memory and overall circuit size. The stored data is affected by the leakage power. There is a major power loss due to the leakage current. The leakage power loss is inversely proportional to size of the circuit which is undesired. The different leakage power reduction technique has been developed to overcome this problem. This paper presents the study of various leakage current in CMOS devices and the reduction techniques used to overcome this problem. In this paper a newer technique called lector (Leakage Control Transistor Technique) is explained.*

KEYWORDS: CMOS, (LECTOR) Leakage Control Transistor, SRAM cell, Sub-threshold, Leakage Current, Threshold voltage.

1. INRODUCTION

In last few years to accomplish the high performance CMOS device, scaling is used. As a result of scaling the delay and area of device are reduced. Additionally, a scaled device also has low supply voltage, reduced threshold voltage, gate oxide thickness and channel length which improves the performance of device. But the minimization of these features inversely affects the leakage current .as technology is scaled down, the leakage current becomes comparable with dynamic power dissipation. As shown in Fig -1. [10]

To reduce the leakage current of CMOS devices various techniques are used. These techniques are sleep transistor technique, Forced stack technique, Sleepy stack technique and the latest technique named as LECTOR technique. These techniques reduces the leakage by stacking leakage path using the off transistors. In LECTOR technique the leakage control transistors are used in between pull-up and pull-down network. In this technique one leakage control transistors is always near its cut-off region of operation without depending on of the input voltage. The Lector follows the concept that, "a state with more than one transistor in OFF state in a path between high to low voltage is less leaky compare to only one transistor OFF between any supply and ground path".

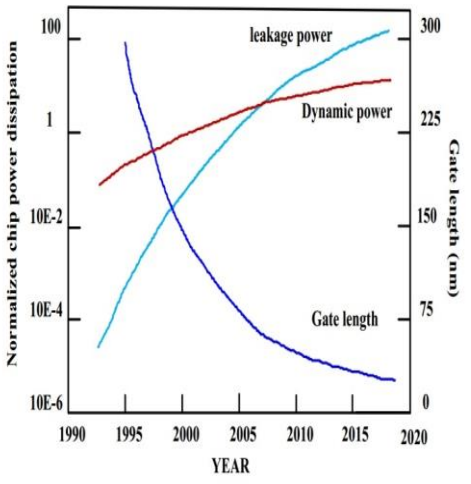

Fig-1: Power dissipation vs technologies

2. DIFFERENT LEAKAGE CURRENTS IN MOSFET DEVICES:

In a CMOS transistor there are two types state of working 1) Non-conducting 2) Conducting. In non-conducting state, there are three types of leakage currents which are sub-thresold leakage current, gate induced drain leakage current and punch through current.[2] In conducting state two leakage currents are gate tunnelling current and junction leakage current. All leakage currents are shown in fig -2.

2.1 DIBL (Drain Induced Barrier Lowering):

As higher voltage is applied on the drain terminal the depletion region of drain start interfacing with the source terminal. Due to this the barrier potential between drain and source is lowered. At this lower potential barrier charge carriers are injected by source without any effective role of

gate voltage. So, a leakage current flows between source and drain. It effectively increase the linear region current in the CMOS.

2.2 Junction reverses bias leakage current:

Junction leakage currents are presents in drain to body and source to body terminal. These terminals are reversed biased due to which a PN junction reverse leakage current flows.[4]

2.3 Sub threshold Leakage Current (Weak inversion):

Weak inversion current is the major contributor to the total leakage current of source. This current is present between source and drain when transistor is in weak inversion region (0 <Vgs <Vth). To make dynamic power dissipation under control, voltage supplied and the threshold voltage (Vth) has to be scaled down, to maintain a high drive current capability. The scaling of Vth results in increasing sub-threshold leakage currents. This current is composed of drift and diffusion currents. But the diffusion current is dominents. Weak inversion current varies exponentially with Vth and Vgs.[3]

2.4 GIDL (Gate Induced Drain Leakage):

This current leaking is between drain and well or substrate. At the gate-drain overlap region under the strong electric field, band to band tunnelling occurs. Due to this tunnelling effect GIDL current comes into picture Meanwhile, due to the collection of the electrons in the drain GIDL current (IGIDL) is produced. The GIDL current increases exponentially due to the threshold voltage, gate to drain potential and gate oxide thickness.[6]

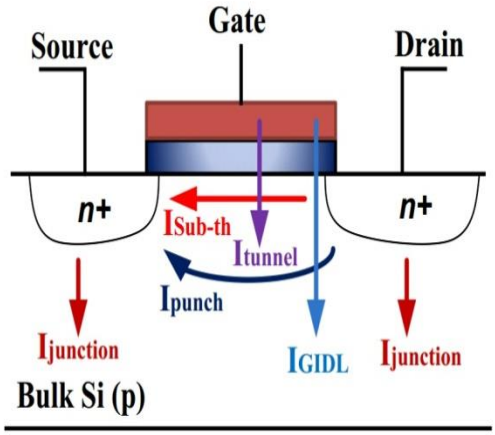

Fig - 2: Different leakage currents in CMOS.

3. SURVEY OF LEAKAGE POWER REDUCTION TECHNIQUES

3.1 Conventional 6T SRAM network in CMOS:

A low power 6T SRAM (fig-3) is designed by using two CMOS inverters which are cross connected. This topology of SRAM has very less static power dissipation .At sub-micron scale the leakage current is the major factor that effects the performance of SRAM. The output terminals of the CMOS inverters are used as the internal load lines of cell to store the data bits. Both lines have the values complimented to each others value.

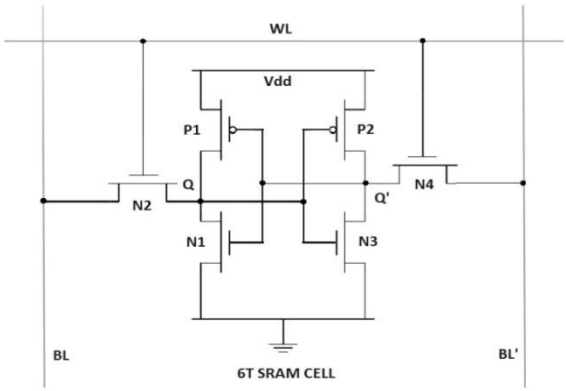

Fig – 3: Architecture of SRAM 6-T Cell

3.1.1 Write Operation:

The data bit is written by using the BL line and its inverted logic value is provided on BLB. The WL line is turned on. The bit lines overpower the cell with new value. If Q = 0, Q' = 1 and BL = 1, BL' = 0. This forces Q to high and Q' to low. Write operation is shown in fig-4.

3.1.2 Read Operation:

To read the data from the SRAM cell logic high values are given to BL and BLB. The WL input is provided a high value to enable the sharing of charge between lines. BL or BL' is pulled down to low depending on Q and Q'. If Q = 0, Q' = 1, BL discharges through N2-N1-GND and BL' stays high. But Q bumps up slightly. Read operation is explained in fig-5. [5]

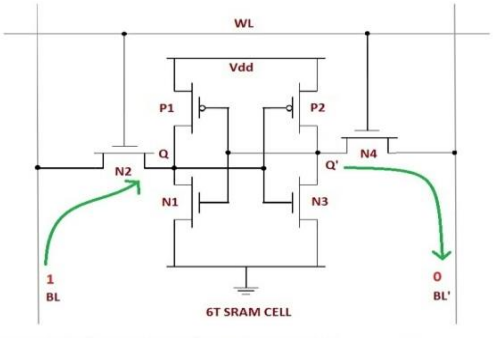

Fig – 4: Write operation of SRAM 6-T Cell.

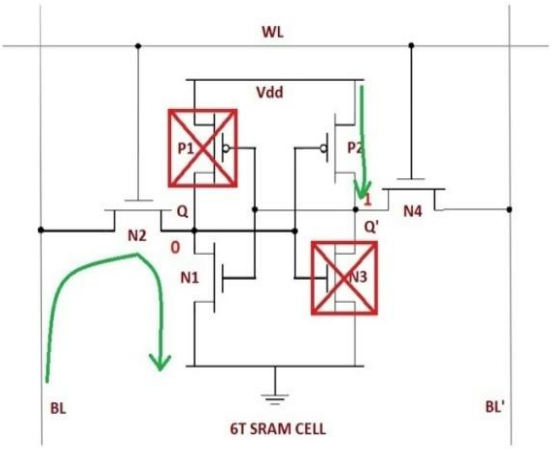

Fig – 5: Read operation of SRAM 6-T Cell

3.2 Sleep Transistor Technique:

This technique is used to isolate the pull-up and pull-down networks from VDD and GND respectively. By using this isolation in sleep mode of operation the leakage power is reduced dramatically. Sleepy transistors are use for this purpose as shown in Fig-6. But due to the extra circuitry area and delay of circuit are increased [7].

3.3 Forced Stack Technique:

This technique uses a duplicate transistor for every transistor in network. Each transistor bears the half of the original transistor width.[8] In the off state the duplicate transistor produce a low reverse current from gate to source. Due to this reverse current overall leakage current reduces SRAM using force stack technique is shown in fig-7**.**

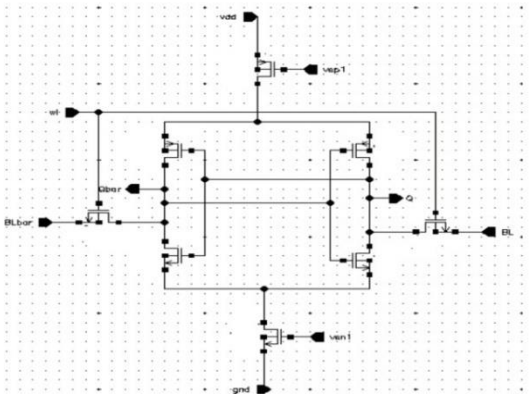

Fig - 6: SRAM Using Sleep Transistor Technique.

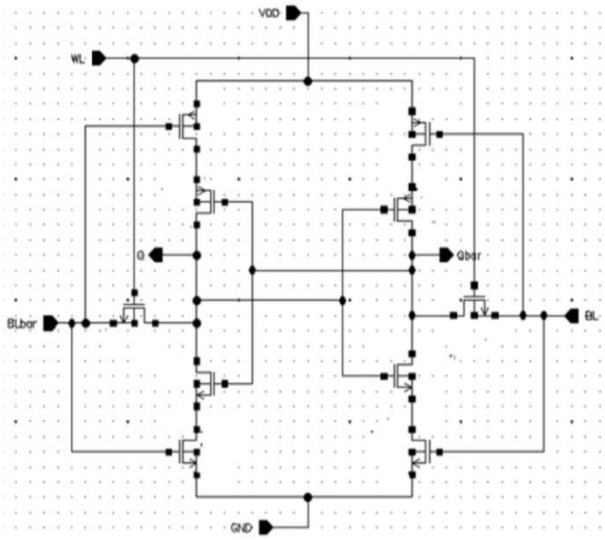

Fig -7. SRAM Using Forced Stack Transistor Technique.

3.4 Sleepy stack technique:

Sleepy stack technique is the combination of both techniques sleep transistor and forced stack method. This technique has lower leakage power dissipation, minimum delay and it also capable to retain the exact state. The sleep transistor of this technique works same as the sleep transistor technique. Sleep transistors are turned on during active mode and off in the sleep mode.

This method achieves the faster switching than forced stack method.

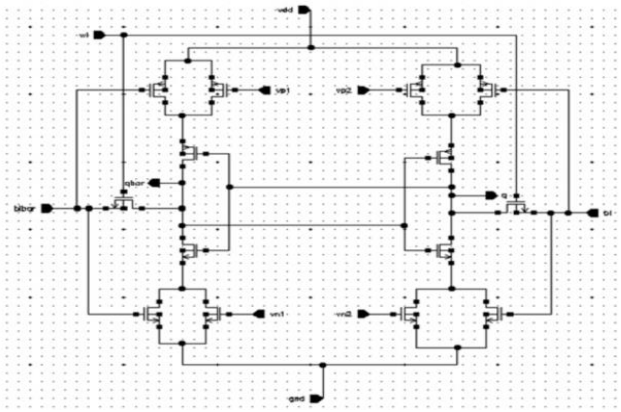

Fig - 8: SRAM Using Sleepy Stack Technique.

3.5 LECTOR approach in CMOS Circuit Design:

Lector approach which reduces the leakage is based on the stacking of transistors between the supply rails. In Lector technique two leakage control transistors are introduced between the pull-up and pull-down networks of a SRAM cell. In this technique one leakage control transistors is always near its cut-off region of operation without depending on of the input voltage. [1] The Lector follows the concept that, "a state with more than one transistor in OFF state in a path between high to low voltage is less leaky compare to only one transistor OFF between any supply and ground path". Thus by using this technique the path with less leakage from VDD to GND can be obtained with help to achieve a less power dissipating circuit.

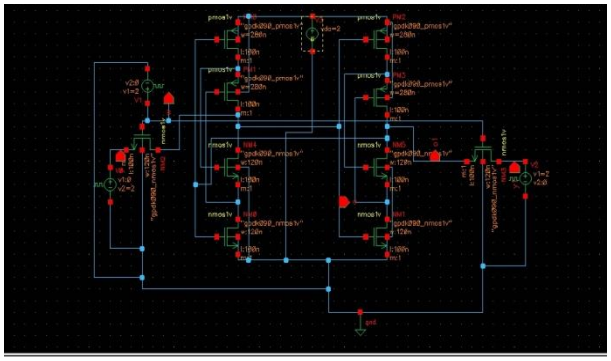

Fig – 9: LECTOR CMOS SRAM Circuit

CONCLUSION

The main purpose of this paper is to give a brief review of different steps taken for the reduction of leakage power loss for VLSI design. In present world of emerging technology the memory hardware is the most important part of any circuit. So from fabrication technology a power efficient design is always expected. The existing technique with LECTOR approach can be improved in future by fabrication methods to achieve more improved performance of memory circuit. It is concluded that this reduction technique will play an important role in reducing the leakage current.

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