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DESIGN OF AN EFFICIENT RECONFIGURABLE FIR FILTER FOR MULTI STANDARD DIGITAL UP CONVERTER

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Abstract - *Digital up converter (DUC) is widely used in communication systems for converting the sampling rate of signals. The function of DUC is to translate a signal from base band to intermediate frequency band. Finite Impulse Response (FIR) filter serves as a major component of DUC inorder to eliminate the distortion caused by up sampling process performed in DUC. In this paper two step optimization technique is proposed to design a reconfigurable multistandard DUC architecture for reducing delay. The proposed technique decreases number of multiplications and additions by reducing the number of input coefficients to multiplier block and successive addition unit. The three standards considered for multistandard DUC are namely Universal Mobile Telecommunication System (UMTS), Wideband Code Division Multiple Access (WCDMA), and Digital Video Broadcasting (DVB). For adopting these standards in the multi-standard DUC, a reconfigurable Root-Raised-Cosine (RRC) FIR filter is used. The two step optimization technique is further improved in the proposed system, by reducing number of input coefficients to First Coding Pass (FCP) block and thus effectively reducing its hardware utilization by 32%. Delay is reduced by 22.23% with the usage of carry select adder instead of ripple carry adder in multiplier block and partial product generator unit. The hardware simulation is done in Xilinx Spartan 3E FPGA using Xilinx 14.2 Vivado Design Suite.*

***Key Words*: Digital up converter, RRC filter, SDR System, Carry select adder, Reconfigurable architecture**

1.INTRODUCTION

The mobile computing and wireless communication applications require low power and high speed Digital Signal Processing systems (DSP). FIR filtering is one of the important operations in DSP. FIR filter is used to eliminate the noises and unwanted components present in the signal. Software Defined Radio (SDR) is one of the latest technologies in the wireless communication. SDR is a single device, which can handle multiple standards. In order to handle multiple standards, SDR comprises of a reconfigurable channel select filter at the base band level. The SDR helps to develop a reconfigurable FIR filter for multi standard DUC. Fig .1 shows the basic block diagram of DUC. It consists of interpolation filter, digital mixer and digital local oscillator.

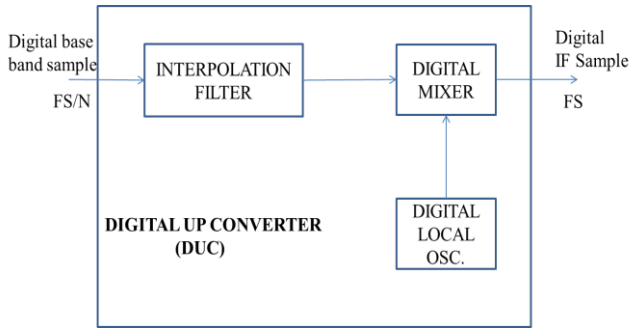

Fig-1: Block Diagram of DUC

DUC is widely used to increase the sampling rate of the input signal, when the signal is transmitted from the base band to intermediate band. This paper focuses on the implementation of an interpolation filter for multi standard DUC. Interpolator has an up sampler and a FIR filter. Up sampler increases the sampling rate of the base band signal by factor of N. N is known as the interpolation factor. This process of increasing sampling rate aids in the smoothening of output signal.

As a result of up sampling, the signal is prone to aliasing and interference effect. Overlapping of original signal with the noise signal is known as aliasing effect. This effect can damage the information kept in signal. The pulse shaping filter is required to shape the base band signal in order to remove the aliasing and interference effect. Pulse shaping filter is used to change the waveform of transmitted signals and thus makes the signal better suited to the communication channel.

Root Raised Cosine (RRC) filters are mostly used as the pulse shaping filter, because of its high inter-symbol interference, rejection ratio and high band width limitation criteria. The RRC filter has three different interpolation factors and two different roll-off factors. Wide band Code Division Multiple Access (WCDMA), Universal Mobile Telecommunication System (UMTS) and Digital Video Broadcasting (DVB) are the wireless communication standards that adopt the RRC filter because of its ability to reduce the Bit Error Rate (BER) by disallowing timing jitter at the sampling instant [1].The proposed system introduced in section 3. Section 4 presents the simulation result of the conventional and proposed systems. Finally, concluded in section 5.

2. CONVENTIONAL RECONFIGURABLE ARCHITECTURE

Architecture of reconfigurable RRC filter is shown in Fig 2. A data generator (DG), a coefficient generator (CG), a coefficient selector (CS) and an accumulation unit block are the major blocks of this architecture. In DG block, master clock (CLK) is used to give the sample output (RRCOUT), and CLK is divided in to three clock sources CLK4, CLK6 and CLK8 [1]. This is used to sample the serial input data RRCIN for different interpolation factor.

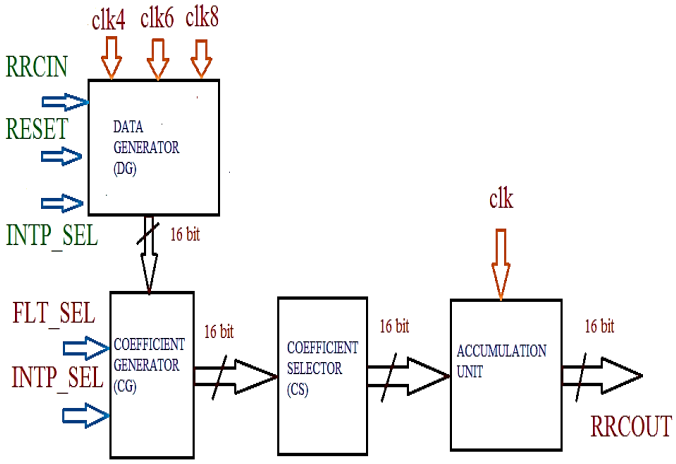

Fig-2: Architecture of the reconfigurable RRC filter

DG block is used to sample the input data (RRCIN) depending on the selected value of the interpolation factor (INTP_SEL). The 25, 37, and 49 tap filters with interpolation factors of 4, 6 and 8 respectively consists of 7 taps branch filters [25/4] = [37/6] = [49/8] = 7. Three different 16 bit shift register have been taken, where the same input has been sampled at three different sample clocks CLK4, CLK6, CLK8. The select line INTP_SEL chooses the appropriate shift register whose output is an up sampled data.

2.1 COEFFICIENT GENERATOR BLOCK

The data flow diagram of coefficient generator block is shown in Fig.3. The coefficient generator block has four blocks. They are First Coding Pass (FCP), Second Coding Pass (SCP), Partial Product Generator (PPG), Multiplexer and Final Addition Unit.

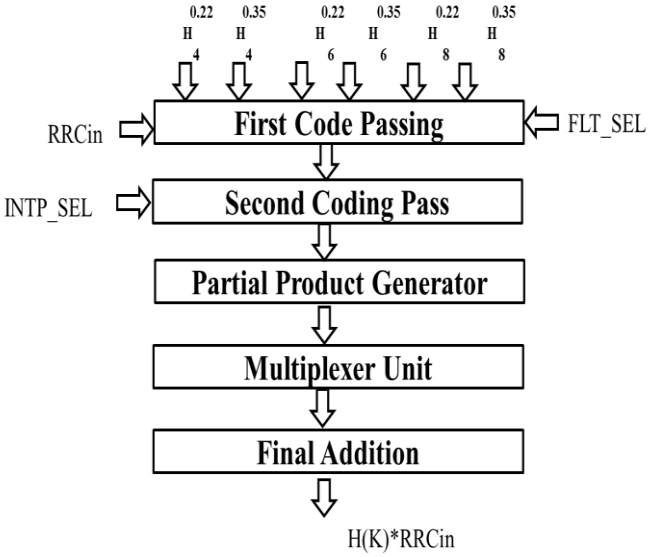

Fig-3: Data Flow Diagram of CG block

2.1.1 FIRST CODING PASS

In the FCP block, the two sets of 25, 37, and 49 tap filters coefficients differ only by roll off factors. The total number of 222 coefficients is given as input to the FCP block. The input coefficient is multiplexed through 2:1 multiplexer. The control parameter FLT_SEL is used as the selection line of the filter. Due to multiplexing operation the total number of 222 input coefficients is reduced to 111 output coefficients. This multiplexing technique decreases the requirement of multiplier block. Block diagram of FCP block shown in Fig 4.

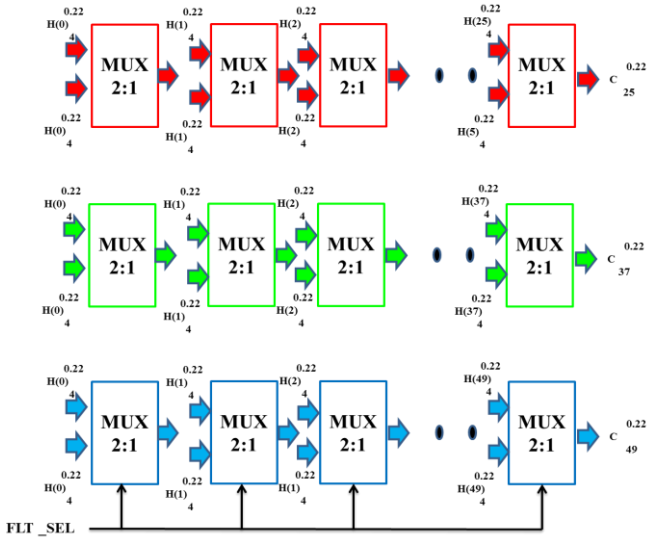

Fig-4: Block Diagram of First Coding Pass

2.1.2 SECOND CODING PASS

The three sets of coded coefficient generated from the FCP block is given as the input to the SCP block. Fig .5 shows the block diagram of SCP. The coded coefficient is again multiplexed through 2:1 multiplexer. The control parameter INTP_SEL selects the desired filter coefficient.

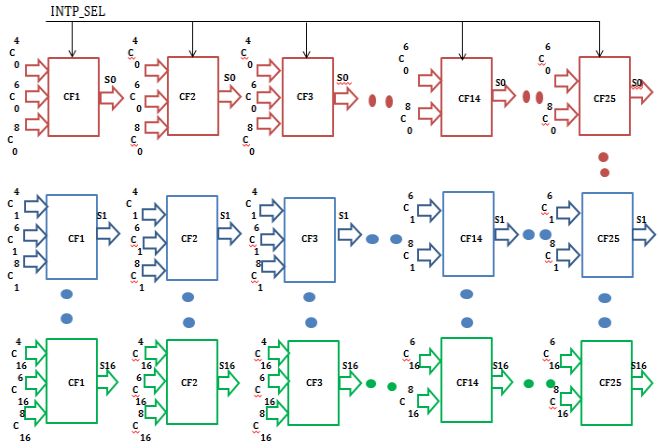

Fig-5: Block Diagram of Second Coding Pass

2.1.3 PARTIAL PRODUCT GENERATOR

Shift and add method is used to generate the partial product during the multiplication of input data and coefficient. Here a ripple carry adder is used for addition operation. In BCSE technique, the realizations of sub expression using shift and add method removes the common term present in a coefficient [6]. The block diagrams of PPG unit shown in Fig.6.

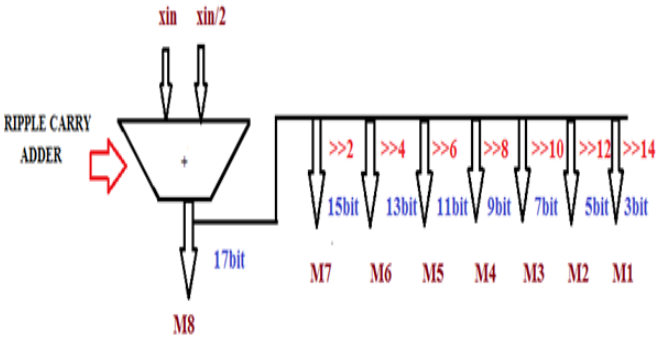

Fig-6: Block Diagram of Partial Product Generator

2.1.4 MULTIPLEXER AND FINAL ADDITION UNIT

The block diagram of multiplexer and final addition unit is shown in Fig.7. The output from the PPG block is given as the input to the multiplexer unit. In multiplexer unit two bit BCSE algorithms is used. Two bit BCSE ranges from 00 to 11. Out of these three BCSs, an adder is used only for the pattern 11. Here 16 bit coded coefficient is partioned in to eight groups of two bit. Each two bits acts as the selection line for eight 4:1 multiplexers. Using the former 2 bit coded coefficient, the appropriate data is selected from the PPG unit.

The addition unit performs the summation of all the output from the PPG block followed by eight multiplexer units. In addition unit, ripple carry adder is used for performing addition. The output generated from the ripple carry adder passes through 2's complement circuit. The output from final addition unit depends on the sign magnitude of the coded coefficient.

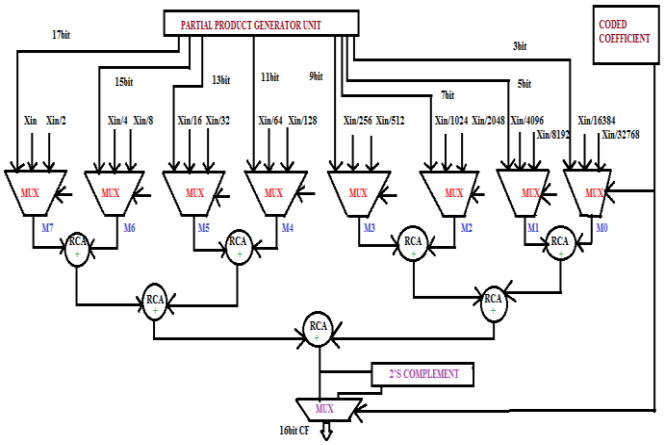

Fig-7:block diagram of multiplexer and final addition unit

3. PROPOSED RECONFIGURABL ARCHITECTURE

In the proposed system, the modification is done in the FCP block, PPG unit and final addition unit as shown in Fig.8.

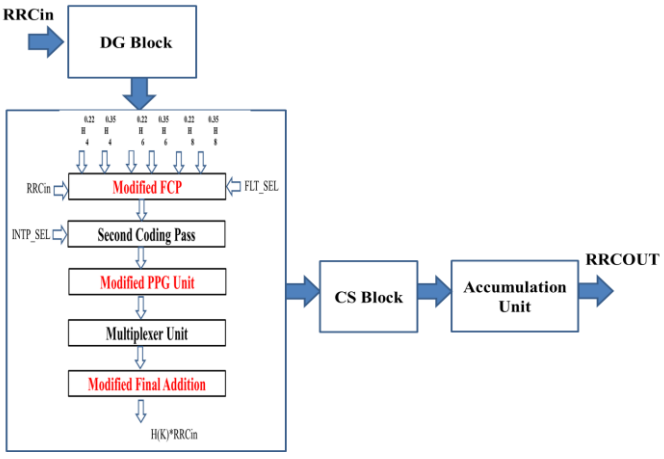

Fig-8: Modified Architecture of RRC FIR filter

In the modified FCP block, two set of 25, 37, and 49 tap filter coefficients are considered. They differ only by roll off factors. A total of two sets of 13 coefficients, each of 16 bit are given as input to the first row of multiplexers in FCP block, next two sets of 19 coefficients each of 16 bits are given as input to the second row of multiplexers in FCP block, a total of two sets of 25 coefficients each of 16 bit are given as input to the third row of multiplexers in FCP block. Hence the required number of multiplexers is reduced in FCP block. The input coefficients are multiplexed through 2:1 multiplexer. The control parameter FLT_SEL is used as the selection line of the filter. Block diagram of modified FCP shown in Fig.9.

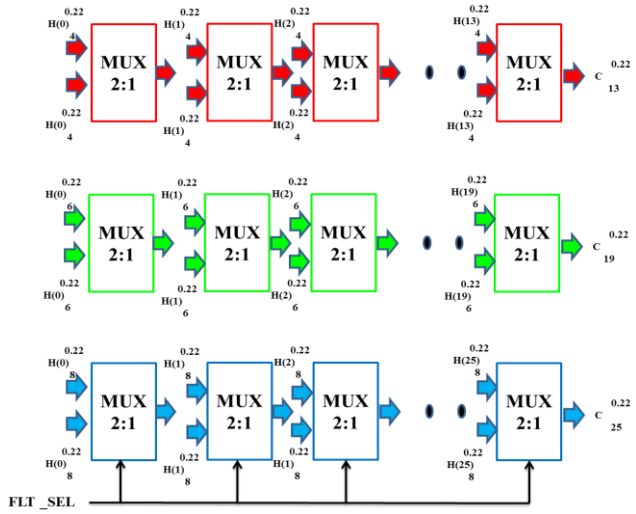

Fig-9: Block Diagram of Modified FCP block

Shift and add method is used to generate the partial product during the multiplication of input data and coefficient. Here an efficient Carry Select Adder (CSLA) is used instead of Ripple Carry Adder (RCA) for addition operation because of its reduced delay. Fig.10 shows the block diagram of modified PPG unit.

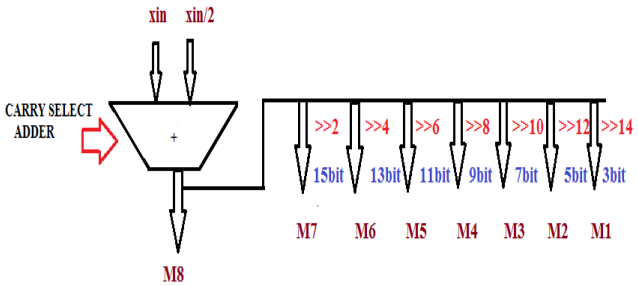

Fig-10: Block Diagram of Modified PPG unit

The addition unit performs the summation of all the output from the PPG block and eight multiplexer units. Addition unit uses an efficient CSLA instead of ripple carry adder for addition operation. The output generated from the carry select adder passes through 2's complement circuit. The output from final addition unit depends on the sign magnitude of the coded coefficient. Modified multiplexer and final addition unit are shown in Fig.11.

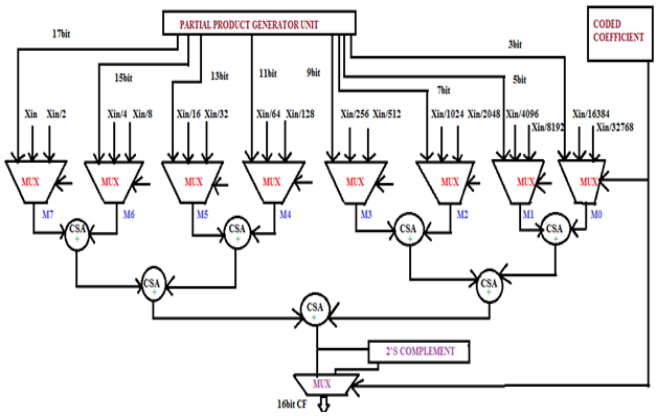

Fig-11: modified multiplexer and final addition unit

3.1 CARRY SELECT ADDER

Conventional CSLA uses multiple RCA for obtaining the partial sum and carry for input Cin =0 and Cin =1. Multiplexers are used to select the final carry and sum. Here we use an efficient CSLA shown in Fig.12. The basic concept of this CSLA is to utilize binary to excess-1 converter (BEC) instead of RCA with Cin =1 [7]. By using an efficient CSLA instead of conventional CSLA, the delay is reduced in the proposed system.

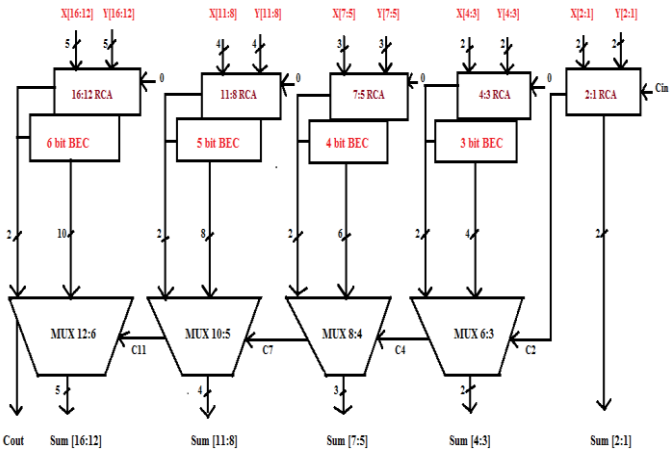

Fig-12: Block Diagram of 16 bit CSLA

The 16 bit CSLA is divided into five groups. Group 1 has one 2 bit RCA. Group 2 also has one 2 bit RCA which consists of one half adder and one full adder. When Cin =0, the multiplexer selects the output which is directly coming from 2 bit RCA. When Cin=1, the multiplexer selects the output coming from 2 bit RCA followed by three bit BEC. Three bit BEC is used instead of the next 2bit RCA present in the existing system. The BEC adds one to the output from 2 bit RCA. The carry generated from the group 2 is given as selection line of multiplexer in the group 3. The block diagram of group 2 is shown in Fig.13. By using this efficient CSLA, delay can be reduced.

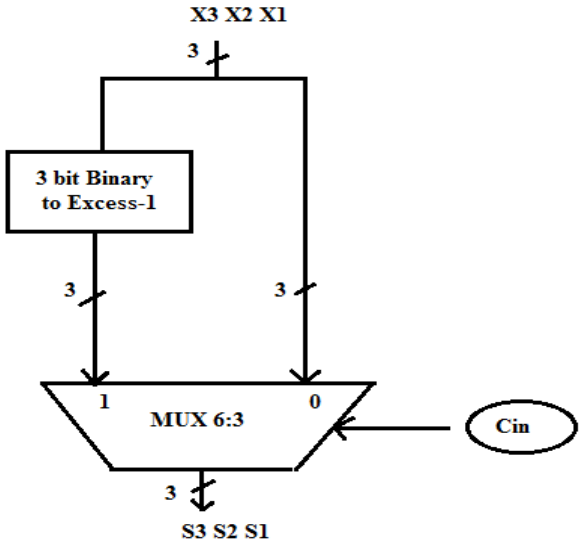

Fig-13: Block Diagram of group 2

4. SIMULATION RESULTS

Simulation and RTL Design of conventional RRC FIR filter and proposed RRC FIR filter is given below. Coding was done using Verilog HDL. Simulation was done using Xilinx ISE design suit 14.2.

Conventional RRC filter is designed. The simulation and RTL are given below. Fig.14 shows the simulation result of the conventional RRC FIR filter. The variable 'y' gives the filter output with 'rrcin' being the input to system. The variable 'INTP_SEL' and 'FLT_SEL' helps to select the desired filter coefficient.

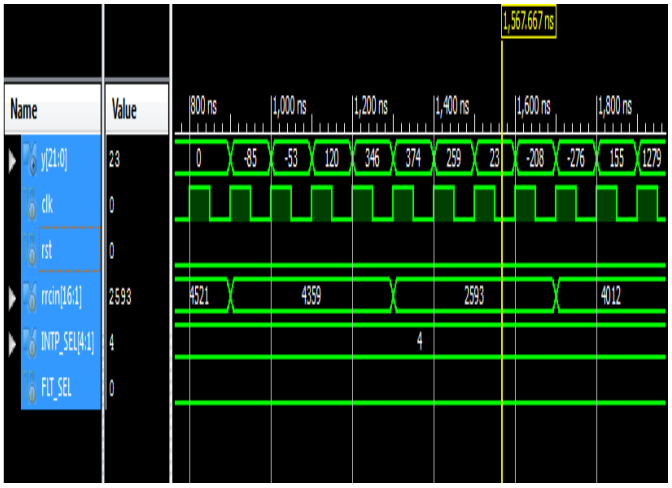

Fig -14: Simulation result of Conventional RRC FIR filter

The RTL of conventional reconfigurable RRC FIR filter is shown in Fig.15. It shows the circuit and interconnection of blocks inside the system.

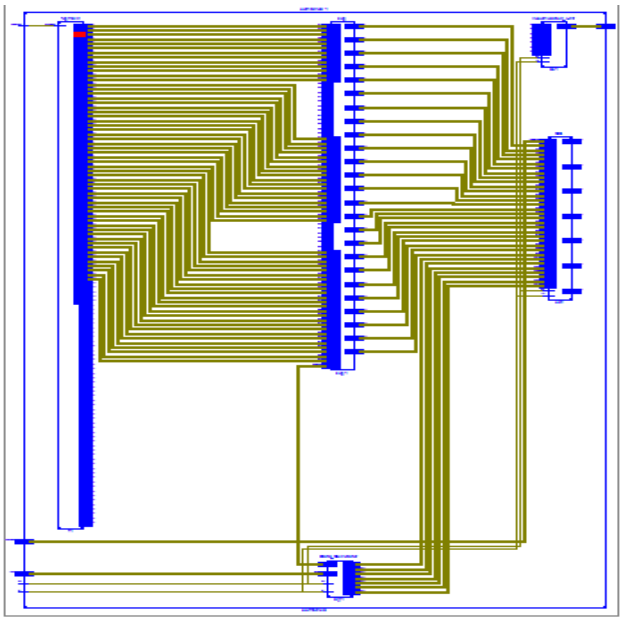

Fig-15: RTL Design of Conventional RRC FIR filter

Proposed RRC filter is designed. The simulation and RTL are given below. Fig.16 shows the simulation result of the proposed RRC FIR filter. The variable 'y' gives the filter output with 'rrcin' being the input to system. The variable 'INTP_SEL' and 'FLT_SEL' helps to select the desired filter coefficient.

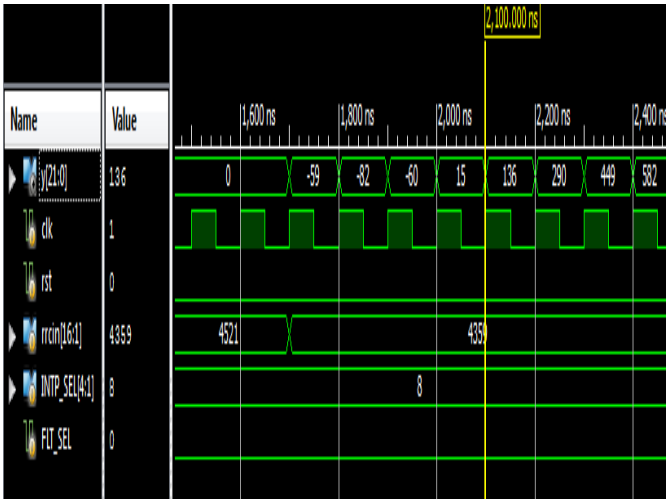

Fig-16: Simulation Result of Proposed RRC FIR filter

The RTL of proposed reconfigurable RRC FIR filter is shown in Fig17. It gives the circuit and inter connection of blocks inside the system.

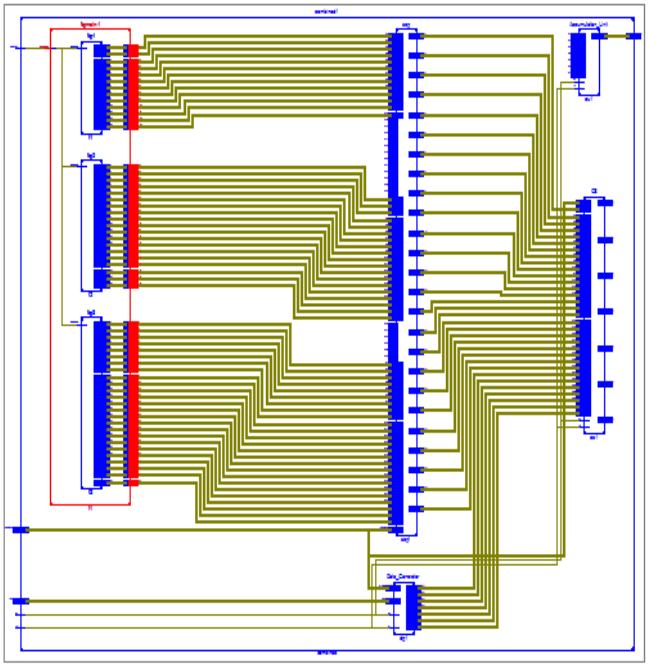

Fig-17: RTL Design of Proposed RRC FIR filter

Table-1: Device and delay utilization summary of PPG unit of RCA and proposed CSLA.

Summary of PPG UNIT	RCA	Proposed CSLA
No. of Slice Register	25	16
Delay(ns)	10.54ns	7.02ns

Table-2: Device utilization summary of RCA and proposed CSLA.

Summary of FCP Block	RCA	Proposed CSLA
No. of bonded IOBs	1887	969

Table-3: Delay analysis summary of RCA and proposed CSLA

Summary of Addition Unit	RCA	Proposed CSLA
Delay(ns)	25.10ns	22.06ns

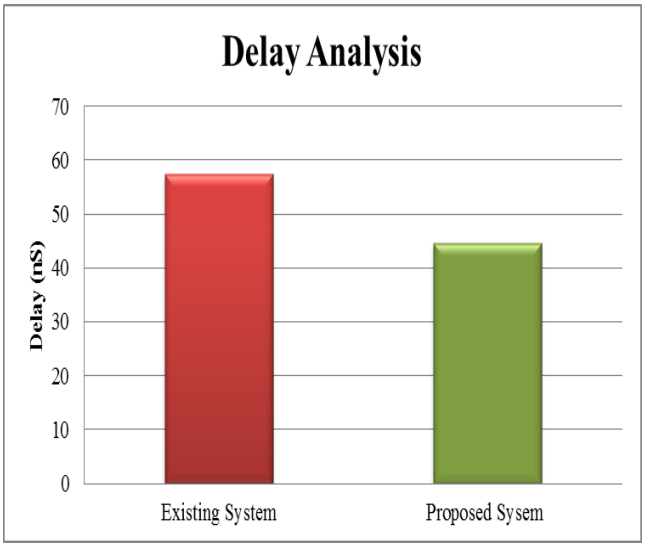

Chart-1: Delay Analysis of Two RRC FIR Filters

5. CONCLUSION

A reconfigurable RRC FIR filter architecture for multi standard DUC is designed. A two step optimization technique is used in the design of conventional reconfigurable RRC FIR filter. In the proposed system, the two step optimization technique is further improved by reducing the number of input coefficients to the FCP block. This technique reduces the hardware utilization of FCP block by 32%. The proposed architecture uses carry select adder instead of ripple carry adder in multiplier block and thus the delay is reduced by 22.23%.

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