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Design of Pulsed latch Shift register

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Abstract - *The design and implementation of Shift register with consumption of less power and less area occupation by latches. Basically shift registers are built by flip flops but here flip flops are replaced by pulsed latches to reduce area power consumption. The problem of timing in latches is removed by using the compound non overlie clock signals which are delayed instead of standard clock pulse. A 256 bit shift registers are designed in cadence virtuoso using gpdk 180nm technology and VDD=1.8v and the SSASPl latch is compared with other latches.*

Key Words*: *Pulsed latch, pulsed clock, shift register, flip flop etc..

1. INTRODUCTION

Shift register are employed in many applications, such as digital filters, communication receivers and image processing Ic's because they are basic building blocks in VLSI circuits . Recently because the size of the image data has increasing heavily due to the demand for high quality image data, word length of shift register growing to manage large number of image data in image processing ICs. As we know the word length of the shifter register increases, the power consumption and area of the shift register becomes more vital design considerations.

The design of a register is very easy. An n-bit register consist of serially attached n data FFs. The occupation of area and consumption of power are more vital than performance of FF as result there is no circuit between flip flop within shift registers. Recently, to cut down the consumption if power and occupation of area FFs have been taken down by pulsed latches in various functions, because latches are very much minor compared to flip-flop. But the pulsed latches are suffering from timing problem between pulsed latches. Here the shit registers are built with low power and using pulsed latches. The problem of timing within the latches are changed by compound non overlie clock pulses which are delayed rather than traditional single pulsed clock signal.

2. SHIFT REGISTER

Shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse1:4) and CLK_pulseT). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Delay circuits cause large area and power overheads.

Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Figure (a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. Fig. 5(a) shows an example the proposed shift register. The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse1:4 and CLK_pulseT). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Figure (b)shows the operation waveforms in the proposed shift register. The proposed shift register reduces the number of delayedpulsed clock signals significantly, but it increases the numberof latches because of the additional temporary storage latches. As shown in Fig. 6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an shift register is divided into sub shift registers, the number of clock-pulse circuits is and the number of latches is. A sub shift register consisting of latches requires pulsed clock signals.

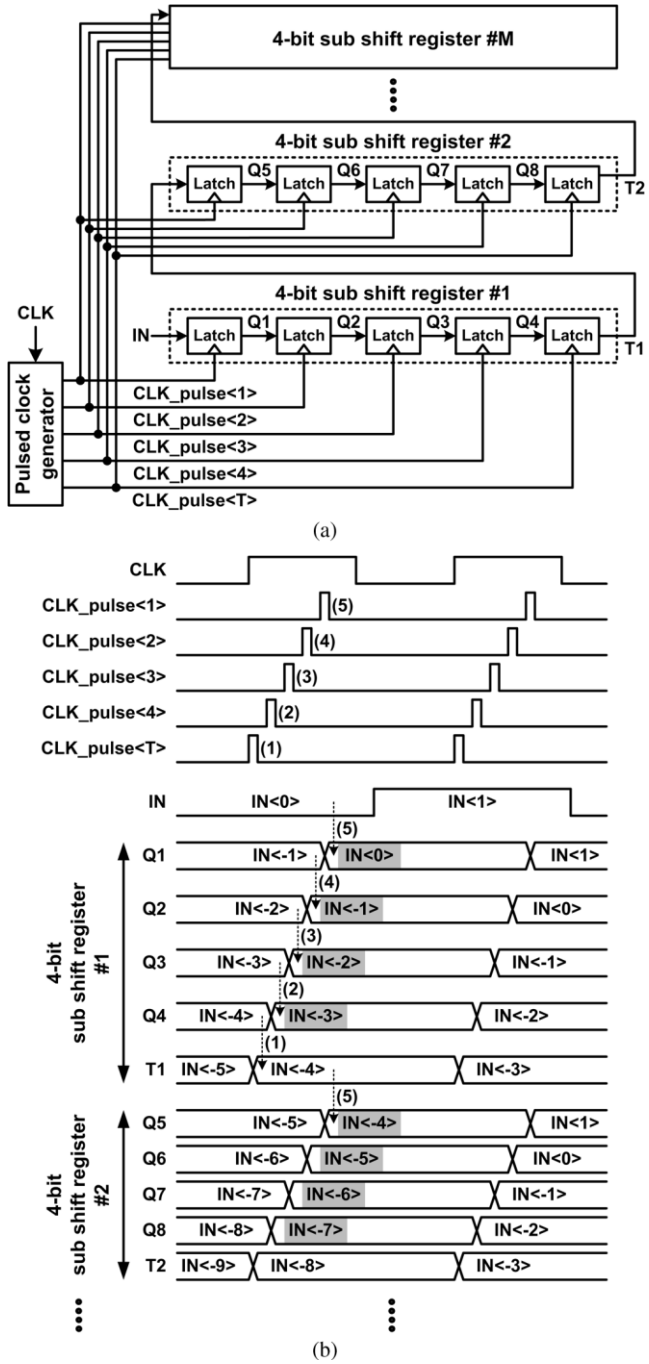

Figure1 Proposed Shift register

2.1 Pulsed Clock generation circuit

To get constant form of clock pulse the summing up of all inverters rising and falling times within the circuits of delay should be less than typical delayed clock pulsed clock circuit. However in fig2 the summing up of inverters rising and falling times are longer than within clock pulse generator with the effect of delay, the periodic dimension are often because And circuit is used to produce the very sharp pulse and 2 signals which are delayed. Therefore, for short pulse signals the pulse generation circuit is suitable.

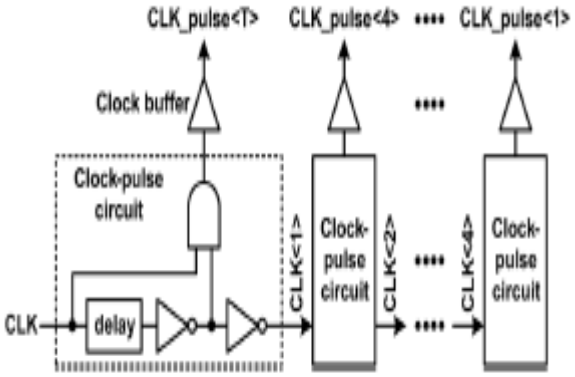

Fig2 Pulse generation circuit

3 IMPLEMENTATION

In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Figure 3, which is the smallest latch, is selected. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig. 8 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.

The SSASPL latch is designed and simulated with 180nm technology at VDD= 1.8v.

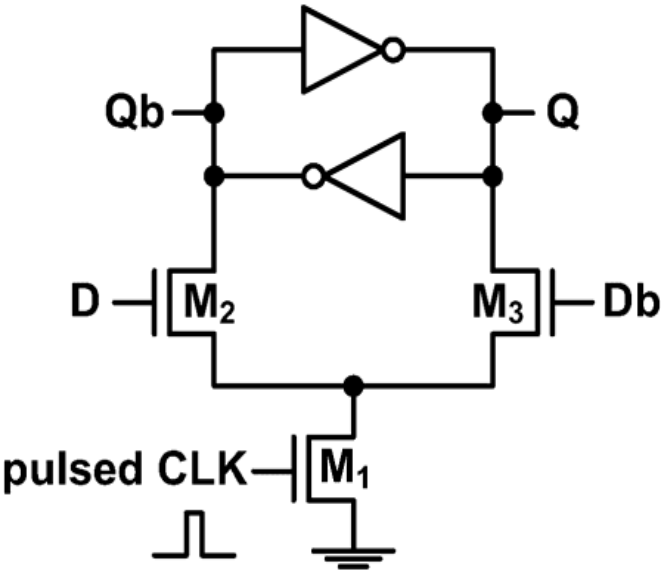

Figure3 SSASPL latch.

4. RESULT

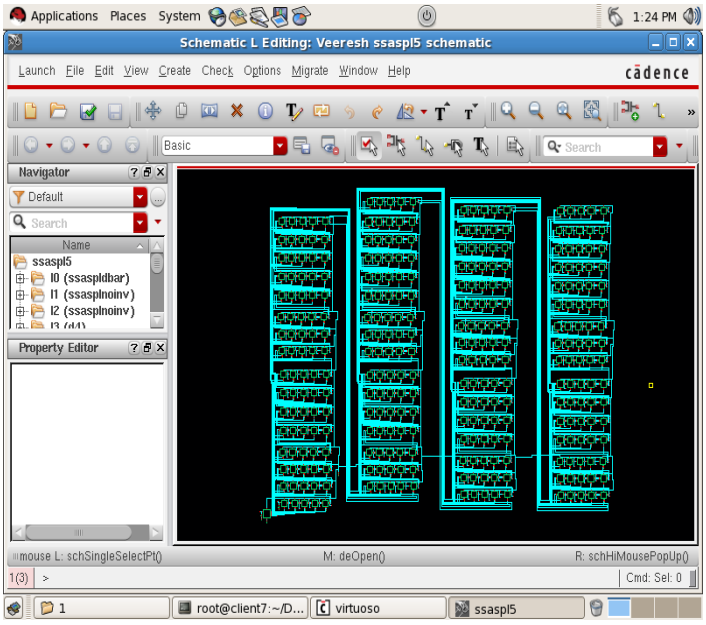

Fig Schematic of 256bit shift register

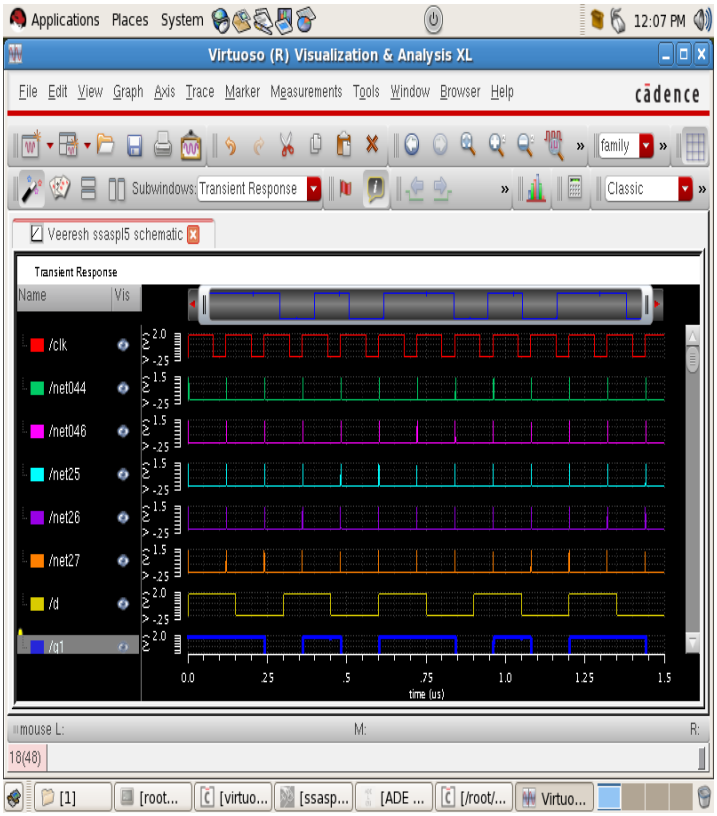

Fig Input of 256 bit shift register

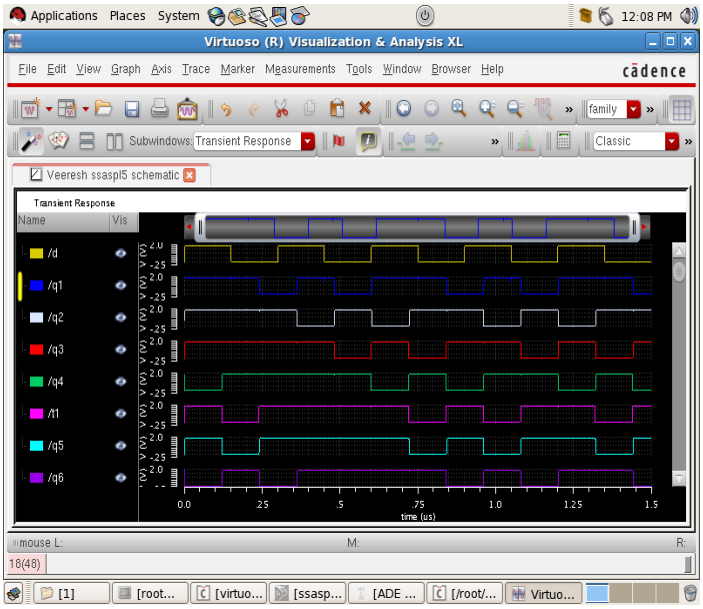

Fig Output of 256 bit shift register

5 COMPARISION

Table 1 shows Comparison of power in (mW) between latches

Sl no	Latches	Power
1.	PowerPC 603 MS latch[5]	4.6mW
2.	SSTC MS latch[5]	3.56mW
3.	DSTC MS latch[5]	3.43mW
4.	HLFF[6]	3.37mW
5.	SSALA[6]	2.78mW
6.	SSASPL	1.9mW

Table 2 shows the number of transistor count in different latches

Sl no	latches	No of transistor	No of transistor connected to clock
1.	PowerPC MS latch[5]	18	8
2.	SSTC MS latch[5]	16	2
3.	DSTC MS latch[5]	9	2
4.	HLFF[6]	20	5
5.	SSALA[6]	9	1
6.	SSASPL	7	1

CONCLUSION

This paper proposes design and implementation of shift register using pulsed latches. The shift registers are built using latches which are smaller in size than flip flop. The schematic of 256 bit shift register is designed in Cadence tool with VDD =1.8v, power is calculated with respect to different latches.

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