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# Hardware Implementation and analysis of a Seven Level MLI with SVPWM

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**Abstract -** Various modern industrial applications require higher power rating equipment. Some of the medium voltage motor drives and utility applications demand medium voltage and megawatt power level. The Multilevel power inverter has been developed to meet this demand more effectively. The constraint in MLI is that of the increasing number of switches involved. Though Sinusoidal Pulse Width Modulation (SPWM) is most popularly used for inverters, the Space Vector Pulse Width Modulation (SVPWM) is becoming popular in inverter systems with - better utilization of input voltage, lesser harmonic content and better output voltage profile, especially for a drive system. The complexity of calculations involved though, pose a difficulty in SVPWM especially with MLIs.

This paper proposes a simplified low computational Space vector algorithm applied to a reduced switch MLI topology. The simulation of the proposed model is done in MATLAB/Simulink and the hardware prototype model at low power was implemented with DSPACE.

***Key Words*: Reduced Switched Multilevel Inverter (MLI), Low Computation Space Vector Pulse Width Modulation (SVPWM) Algorithm**

## 1. INTRODUCTION

High performance and easy & accurate controllability are a demanding requirement for industrial drives in general. Controlling of high power rated industrials drives, usually induction machine drives deals with controlling of their inverter topology. From various researches it has been established that multilevel inverters are gaining prominence in now a day due to its inbuilt capability of high voltage handling and good harmonic rejection abilities with recently available power devices. While using a multilevel inverter the high number of switches contributes to high switching losses. But in recent years many efficient multilevel inverter topologies with less number switches have been proposed promising improvements in demanding industrial requirements .This paper proposes one such reduced switched multilevel topology [1-2].

Various PWM techniques have realized to control the MLI topologies to provide a good modulation range, decreased losses in switching, reduced THD, also effectiveness in digital implementation. Comparing with other pulse width modulation methods SVPWM is the highly recommended one. The typical SVPWM techniques involve tedious calculations which increase the complexity of implementation especially for higher level MLIs[3]. In this paper we realize a simplified space vector modulation algorithm avoiding the complexities with determination of sector division , derivation of switching states and its timing instants .

With higher number of levels, When employed in MLI the hardware realization will become complex and leads to increased memory consumption. Also the paper includes the hardware implementation of the reduced switch MLI with low computational SVPWM technique[4-5].

### 1.1 PROPOSED MLI TOPOLOGY

The proposed multilevel inverter to accomplish a seven level output with reduced switches is indicated in Fig.1.

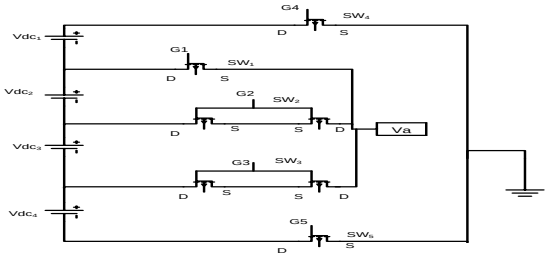


Fig.1. Circuit diagram of Proposed Multilevel Inverter Topology

The maximum possible output voltage $V_0$ is given by $V_0 = (n-1)/V_{dc}$. Where n represents the number of DC voltage sources per phase.

TABLE I. SWITCHING STATES OF PROPOSED MLI

| Voltage level | Switches Turn ON |
|---|---|
| $3V_{dc}$ | $Sw_1$& $Sw_5$ |
| $2V_{dc}$ | $Sw_2$& $Sw_5$ |
| $1V_{dc}$ | $Sw_3$& $Sw_5$ |
| $0V_{dc}$ | - |
| $-1V_{dc}$ | $Sw_1$& $Sw_4$ |
| $-2V_{dc}$ | $Sw_2$& $Sw_4$ |
| $-3V_{dc}$ | $Sw_3$& $Sw_4$ |

The proposed topology achieves the different levels as per the switching sequence shown in the switching table. For example to obtain output voltage of +Vdc, switches $Sw_3$ and

$Sw_5$ are turned ON. Similarly all the other switching levels are realized. The switching losses and complexity in multilevel inverters can be reduced by reducing the number of switches.

### 1.2 SPACE VECTOR PULSE WIDTH MODULATION

Implementation of SVPWM strategy for controlling offers less harmonic distortion in the output voltages and currents. It gives flexibility in optimizing switching pattern design. A Low computational algorithm SVPWM for a multilevel multiphase system is proposed here [6]. The following flow chart summarizes the steps of the algorithm.

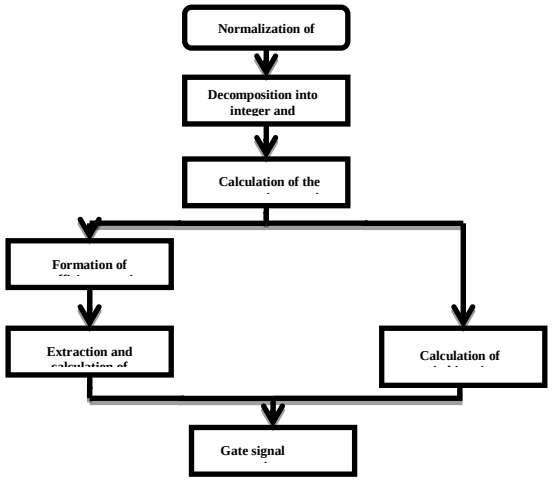


Fig. 2. Flow chart for the SVPWM implementation

1) Initially the normalized reference, Vr is obtained from the reference voltage vector $V_{dc}$ using the expression.

$$\mathbf{v}_r = \frac{\mathbf{V}_r}{V_{dc}} = [{v_r}^1, {v_r}^2, \dots, {v_r}^P]^{\mathrm{T}}$$

2) Then decompose the normalized reference vector into the sum of its integer part, $v_i$, and its fractional part, $v_f$, by means of the equations

$$\mathbf{v}_i = \mathrm{integ}(\mathbf{v}_r) \in \mathbb{Z}^P$$
$$\mathbf{v}_f = \mathbf{v}_r - \mathbf{v}_i \in \mathbb{R}^P$$

3) The next step is to calculate the permutation matrix P that sorts the vector $v_f$ in descending order in accordance with

$$\mathbf{P}\begin{bmatrix}1\\ \mathbf{v}_f\end{bmatrix} = \begin{bmatrix}1\\ \hat{\mathbf{v}}_f\end{bmatrix}$$

where $\hat{\mathbf{v}}_f = [{\hat{v}_f}^1, {\hat{v}_f}^2, \dots, {\hat{v}_f}^P]^{\mathrm{T}}$ is the sorted vector in which

$$1 > {\hat{v}_f}^1 \geq \cdots \geq {\hat{v}_f}^{k-1} \geq {\hat{v}_f}^k \geq \cdots \geq {\hat{v}_f}^P \geq 0.$$

4) Now rearrange the rows of the triangular matrix D in order to obtain the matrix D by means of

$$\mathbf{D} = \mathbf{P}^{\mathrm{T}}\hat{\mathbf{D}}$$

5) Further extract the displaced switching vectors, $v_{dj}$, from the matrix D by taking into account the expression -

$$\mathbf{D} = \begin{bmatrix} 1 & 1 & \dots & 1 \\ v_{d1}^1 & v_{d2}^1 & \dots & v_{dP+1}^1 \\ v_{d1}^2 & v_{d2}^2 & \dots & v_{dP+1}^2 \\ \vdots & \vdots & \ddots & \vdots \\ v_{d1}^P & v_{d2}^P & \dots & v_{dP+1}^P \end{bmatrix}$$

6) Now obtain the final switching vectors, $v_{sj}$, by adding the integer part of the reference, $v_i$, to the displaced switching vectors $v_{dj}$ according to equation.

$$\mathbf{v}_{sj} = \mathbf{v}_i + \mathbf{v}_{dj}.$$

7) Lastly the time corresponding to each switching vector is calculated from the components of the vector vf by means of the expression

$$t_j = \begin{cases} 1 - {\hat{v}_f}^1, & \text{if } j = 1 \\ {\hat{v}_f}^{j-1} - {\hat{v}_f}^j, & \text{if } 2 \leq j \leq P \\ {\hat{v}_f}^P, & \text{if } j = P+1. \end{cases}$$

As is evident, this is a generalized algorithm handling all the switching states, providing a sorted switching vector sequence which reduces the number of switching of the switches. This is hence capable of supporting any multi-level multiphase inverter system, enhancing the capability of the algorithm further. In this regard the algorithm is used for the proposed MLI topology here.

### 1.3 SIMULATION RESULTS

The software modeling of the system is carried out using MATLAB/SIMULINK. The Simulation parameters are shown in TABLE II –

TABLE II .Simulation Parameters

| Parameter | Value |
|---|---|
| Cell Voltage | 4.5V |
| Control signal frequency | 50Hz |
| Switching frequency | 2KHz |
| Load | R load = 100 Ω<br>L load = 100µH<br>C load = 220µF |

The proposed model was simulated for feeding passive loads - a resistive load and a resistive-inductive-capacitive load and the results are given below. Fig.3 shows the SVPWM pulses generated by the low computation SVPWM algorithm.

Fig.4 and Fig.5 shows the MLI output waveform with R load and R-L-C load respectively.

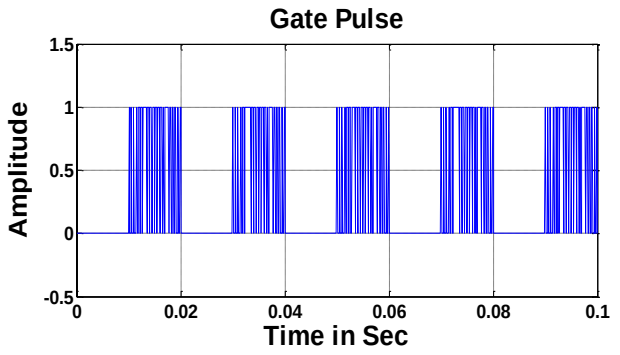


Fig.3. SVPWM pulses

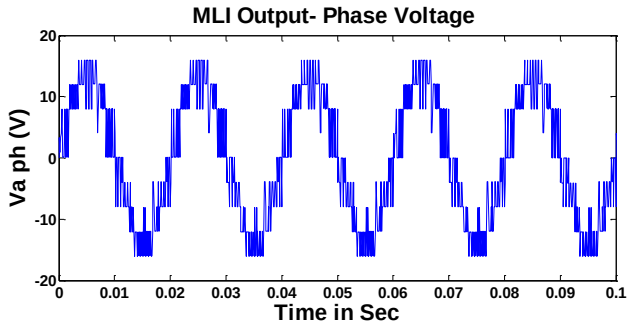


Fig.4. Output waveform with R load

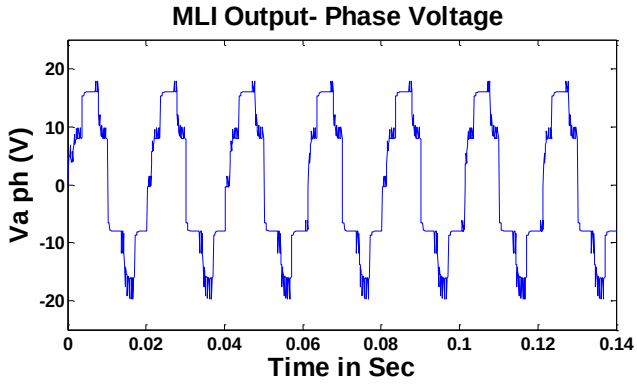


Fig.5. Output waveform with R-L-C load

The five level output is thus observed from the proposed model simulation. The pulses of the various switches can be observed to be different from each other due to the tracing of the levels as per the proposed switching states. Applying for an R-L-C load shows the approximately sinusoidal output waveform that is obtained. Filtering the output can provide near sinusoidal waveforms, promisingly better than Voltage Source Inverters with the voltage levels involved. Also this proves the effectiveness of the MLI topology as well, compared to others for the same output voltage levels, attained with reduced number of switches though.

### 1.4 EXPERIMENTAL SETUP

In addition to the simulation, a low power prototype of the proposed model was implemented. The proposed algorithm has been implemented using MATLAB interface with dSPACE DS1104. The obvious advantage of using hardware-in-loop simulations is that performance of systems for various operating conditions can be compared. Another feature of the dSPACE is the control desk which allows the graphical user interface, through the control desk the user can observe the response of the system, give command to the system through the interface [7-8]. The schematic of the experimental is shown in Fig.6

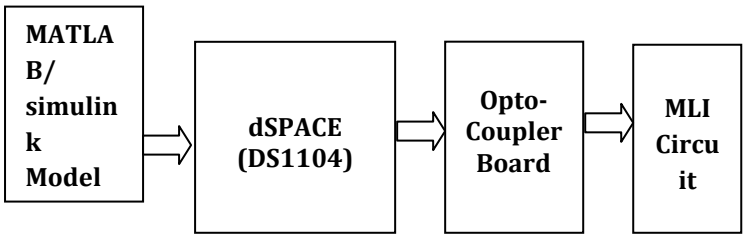


Fig.6. Hardware implementation schematic diagram

The hardware implementation of the proposed system can be divided into three parts:- Pulse generation circuit, Isolation circuit, and Power circuit.

The Pulse generation circuit consist mainly the MATLAB/Simulink model interfaced with dSPACE control card. The system implemented in MATLAB/Simulink, the model is converted to real time codes using a Real-Time Interface (RTI) of the control by the dSPACE DS1104 control card. The gate pulses generated by the model can be obtained at the Digital I/O pins of the dSPACE DS1104 I/O interface.

The pulses obtained from the interface are given to an Isolation circuit, employed to protect the pulse generation circuitry from the power circuit. A 12 pulse optocoupler isolator board is used as the isolation circuit. The isolated pulse outputs are given to the proposed MLI power Circuit.

The Power circuit consists of a 3 phase reduced MLI topology. Each phase has 5 switches with 2 of them bi-directional. Each phase of the power circuit needs 4 DC sources, which is provided by the Regulated DC Power Supply. The load used in this hardware prototype model is a resistive load and resistive-inductive-capacitive load.

Fig.7 and Fig.8 shows the experimental setup of the proposed system.

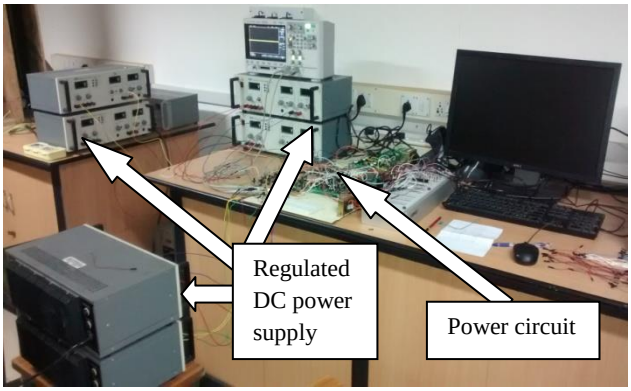


Fig.7. Complete hardware setup

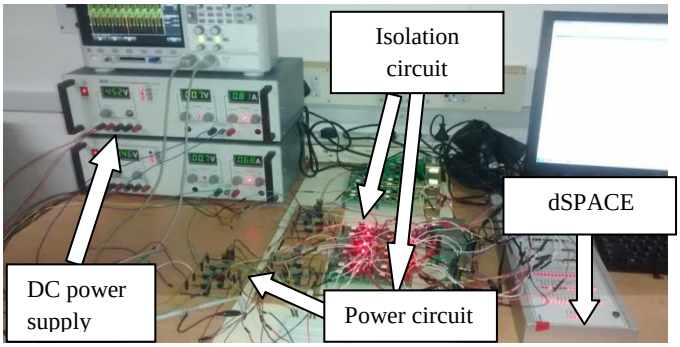


Fig.8. Hardware setup – Power circuit

Fig.9 shows the generated SVPWM pulses obtained after the isolation circuit, which are given to the switches. Fig.10 and Fig.11 presents the hardware output waveform with R load and R-L-C load respectively.

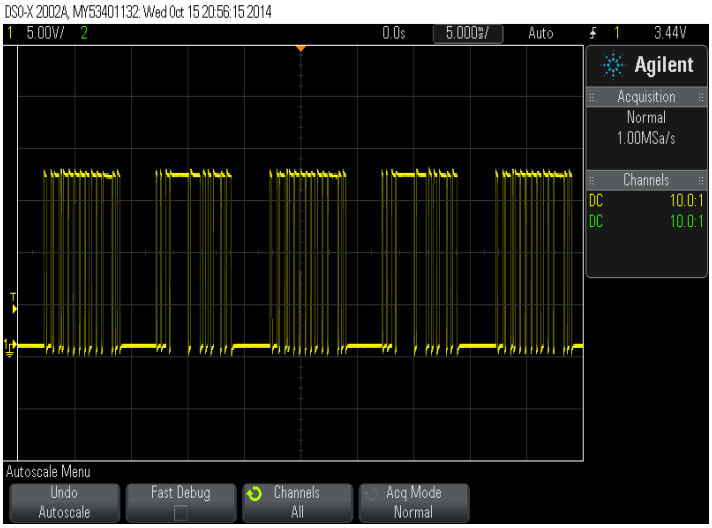


Fig.9. Hardware SVPWM pulses

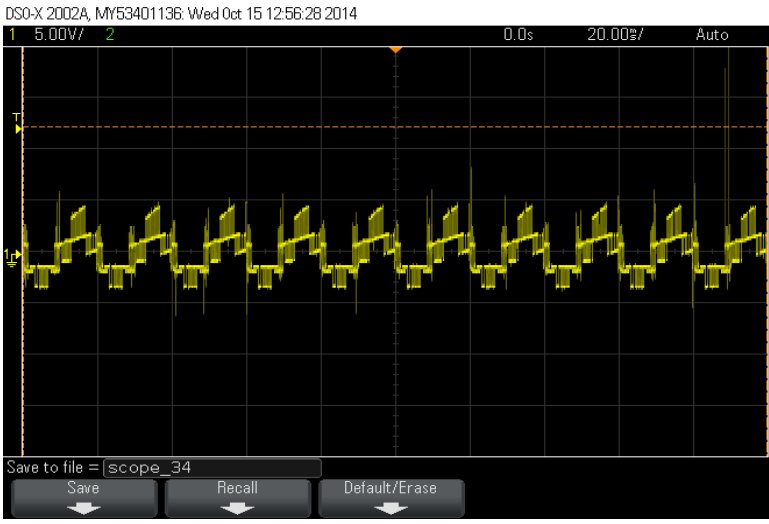


Fig.10.Hardware output waveform with Resistive load

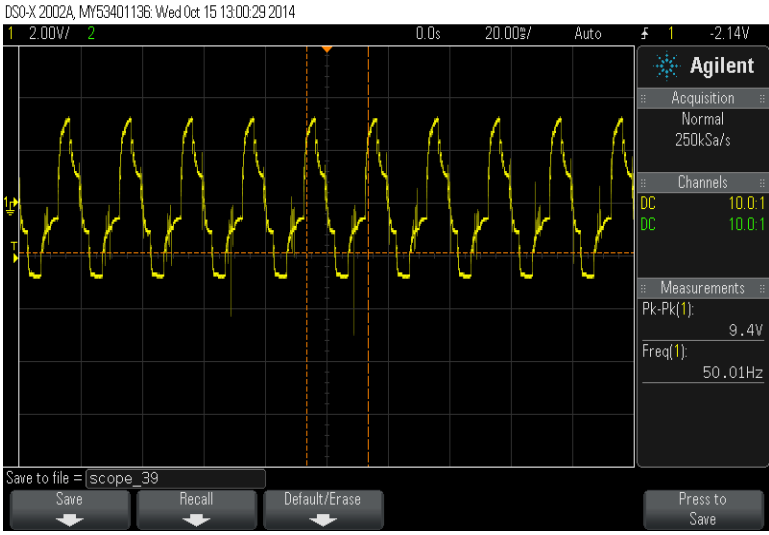


Fig.11. Hardware output waveform with Resistive-Capacitive load

The Hardware results can be observed thus to verify and validate the Simulation results. The output waveforms of both R and R-L-C loads are observed to be almost same in the simulation and hardware setup. The proposed system was thus successfully implemented as a prototype and its effectiveness was clearly observed.

## 2. CONCLUSIONS

The paper implemented satisfactorily a simplified low computational SVPWM algorithm for a reduced switch MLI topology. The observed results from both the simulation and the hardware implementation confirmed the successful

working of the proposed system of both the SVPWM algorithm as well as the reduced switch MLI topology.

This proves the effectiveness of the simplified SVPWM algorithm generally a daunting issue for digital processors and also validates the improvement of the MLI topology. The results of the implemented prototype system hence promise improved and efficient performance in the high power system as well. This is especially useful for a drive system for which the quality of source voltage and performance is of major concern.

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