A Review of Analysis and Modeling of Grid Connected Three Phase Multilevel Unity Power Rectifier with Less Component Counts

[1]Umashankar Verma, [2]Ritesh Diwan

[1]M.Tech Scholar (Power Electronics) Department of Electronics and Telecommunication Engineering, RITEE, Raipur (C.G)
[2]Associate professor, Department of Electronics and Telecommunication Engineering , RITEE, Raipur (C.G.)

Abstract: *In this project, a five level multiple-pole structure based a simple model is designed to improve power factor, to reduce total harmonic distortion and the efficiency improve by using reducing number of components counts. The proposed method is used to design this project is five-level/multiple-pole multilevel unity power rectifier (5L-M2UPFR). There are several method that has already been design which give better response but with more number of component counts. By this method, the unity power and input current shaping is achieved with reduced number of measurement components. Some addition controller is used in the implementation of grid voltage observer to get dynamic response and under unbalanced grid condition the better tracking is achieved.*

Key words: **Vienna Rectifier, 5L-M2UPFR, Power factor, average current control (ACC), Electrical Grid.**

1. INTRODUCTION

An electrical grid is an interconnected community for turning in electricity fromproviders to customers. It includes producing stations that produce electric strength, high-voltage transmission strains that carry strength from distant assets to call for facilities, and distribution strains that connect person customers [1]. Power stations may be placed near a gasoline supply, at a dam site, or to take advantage of renewable strength assets, and are frequently positioned away from closely populated areas. Multilevel converters have become greater appealing for lots industry and academia research. Most of the commercially to be had multilevel inverters require a bulky section-shifted transformer with multiple bridge rectifiers linked at the front-stop aspect [1, 2]. However, the quantity and the load of such configuration are large and heavy. In addition, more losses are skilled in the transformer during low utilization because of its middle resistance [3, 4]. Several new transformers less multilevel rectifier topologies with low switching frequency operation had been reported in the literature. The referred to low-cost topologies have performed accurate performance and additionally confirmed that the clear out length may be extensively reduced in spite of the low switching frequency operation. However, each of those topologies has its limitations and disadvantages. For example, a complex manipulate algorithm is needed to stability the flying capacitors of the three-section megastar-configured PUC topology. While in the case of RPC-DCR topology, simplest two switches are decreased in each phase-leg however the general aspect counts are not notably optimized. Hence, large wide variety of gate drivers and remote gate supplies are still required. As for the DCLP-FC topology, a very good arrangement of hybrid technique is delivered to reduce 50% of the switching gadgets compared with both conventional diode clamped and flying capacitor rectifiers. Nevertheless, a complete of eight dc capacitors is nevertheless needed for this 3-section topology to synthesize a 5-stage segment voltage stepped waveform. Due to the involvement of dc electrolytic capacitors, the lifetime of the power converter will ultimately be suffering from the thermal getting old. This paper offers a new value-effective transformer less a couple of poles multilevel unity power thing rectifiers (M2UPFR). The proposed three-phase M2UPFR makes use of simplest six switches to synthesize a 5-stage enter segment voltage stepped waveform, consequently the aspect counts are substantially reduced. A low switching frequency operation with the common cutting-edge control (ACC) method is applied for the grid modern harmonic reimbursement.

Moreover, the manage set of rules is developed with observer method. Thus, a decrease cost solution is finished with the discount of measurement sensors needed for the remarks manage loop not like the proposed switching method provided in [5]. In addition to that, top notch dynamic reaction is demonstrated with the expected performances of both grid voltage and load modern-day during unbalanced grid condition.

2. Objective

The main objective of this work is design a model to obtain better efficiency with less total harmonic distortion and improvise power factor using less component counts. To design a cost effective transformer less a couple of pole unity power factor rectifier.

3. Problem statement

From the study of various algorithm designed earlier, various problem such as bulky model due to heavy transformer, at high frequency the switching losses are dominant, the output power range also effected, less power factor, more total harmonics distortion, sometimes efficiency also reduced. In this paper, in this paper we are focusing on power factor and the total harmonic distortion of output power.

4. FIVE-LEVEL MULTIPLE-POLE UNITY POWER FACTOR RECTIFIER TOPOLOGY

4.1 Basic Operating Principle

A 5-stage (5L) M2UPFR topology with balanced load is shown in Fig. 1 is built the usage of three-level (3L) VIENNA rectifier cells in each phase-leg. The multiple-pole multilevel diode-clamped inverter concept is similar to the multiple pole structure [6]. Hence, the output terminals of both VIENNA rectifier cells are linked to the respective dc capacitors with the resource of balancing circuit as distinctive in [7, 8]. Based on switching state selection and the direction of phase current the overall performance of this method is synthesized in which each cell is characterized with the three level input voltage stepped waveform. The proposed five-level (5L) multiple-pole VIENNA rectifier (MVR) presented in this paper (Fig.1) achieves a good overall performance with reduced number of components while operating at lower switching frequency. The balanced voltage across the dc-link capacitors and precise operation of bidirectional switches synthesizes a fivelevel stepped input voltage waveform. Thus, low input current distortion and high input power factor are achieved. The requirement of input line inductance is as well reduced due to lower THD.

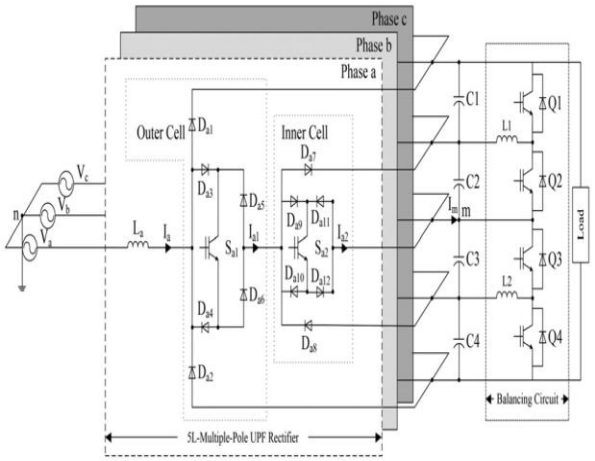

Fig 1: Unidirectional 5L-M2UPFR with the balancing circuit

4.2 Controller Design

4.2.1 Unity Power Factor Control

This power factor control both load current and grid voltage which can be seen in the circuit diagram below. The

controller structure is constructed using synchronous reference frame (SRF) current control [9]. The complicated phase locked loop design is used in d-q transformation to limit control bandwidth.

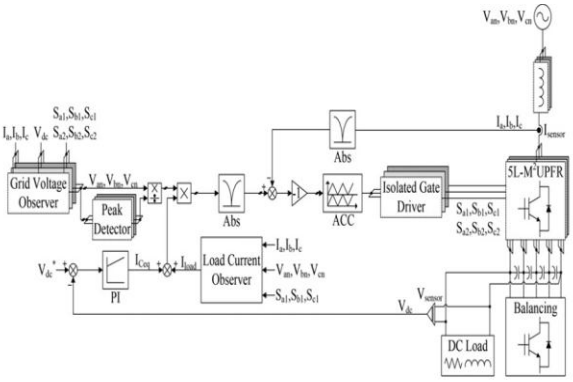

Fig. 2: Block diagram of the unity power factor controller with the grid voltage and load current observers

The dc-link voltage control carried at outer loop and current control carried at the inner loop [6]. The dc equivalent capacitors current is calculated by the outer loop control and regulates the output dc link voltage. Meanwhile, the load current is formulated from the power balanced principle.

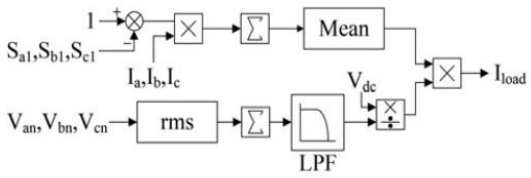

Fig 3: The Load current observer

4.2.2 Voltage Control

The dc-link voltage is regulated with a simple proportional – integral controller which is expressed as follows

$$I_{Ceq} = K_p \frac{\tau_i s + 1}{\tau_i s}\left[V_{dc}^*(t) - V_{dc}(t)\right]$$

Where, K_p is the proportional gain of the dc-link voltage regulator and t_i is the settling time of the dc-link voltage tracking and the approximation value of K_p is obtained from the energy storage model. According to stability criteria, the proportional gain of the control system expressed in below equation.

$$K_p = \frac{3V_m \tau_i}{2V_{dc} C_{eq} P_o}$$

4.2.3 Current Control

The grid current control technique of the active rectifier can be classified into four categories such as space vector modulation (SVM) [10, 11], fix hysteresis band current control (FHBCC) [9, 12], variable hysteresis band current control [13] and ACC [12, 14]. The SVM scheme requires high computational effort due to the complex sector control algorithm required for higher voltage stepped level rectifier topology [15]. Both HBCC and ACC can overcome the stated problems of SVM scheme. However, FHBCC scheme exhibits the disadvantage of variable switching frequency which complicates the design of the input inductance filter.

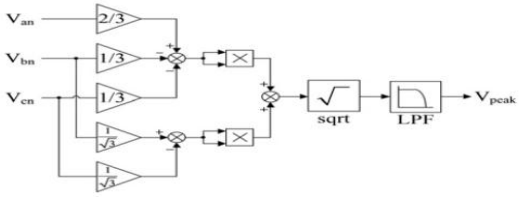

Fig 4: Energy stored model

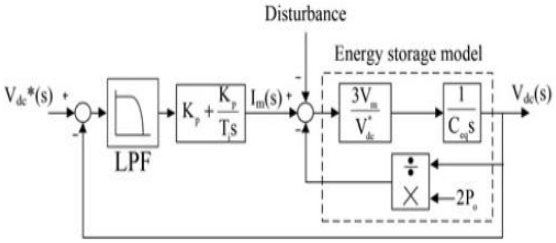

Fig 5: Peak detector of the grid voltage for the reference sinusoidal wave

The carrier-based ACC scheme is applied for the proposed 5L-M2UPFR and allows the desired voltage space vector to be modulated using simple analogue comparators. By doing so, lower cost implementation and lesser computational effort needed are achieved.

4.2.4 Grid Voltage

Several observer strategies had been proposed for numerous varieties of rectifier configuration [16-18]. Besides the benefit of disposing of the sensors needed, the observer approach reduces the size of converter and offers a lower production cost as well. Even though the statistics of three phase grid currents are enough to derive and estimate the ac and dc voltages, but huge dc hyperlink voltage ripples are experienced throughout the computational manner. Hence, inflicting high enter cutting edge total harmonic distortion (THD) inside the grid.

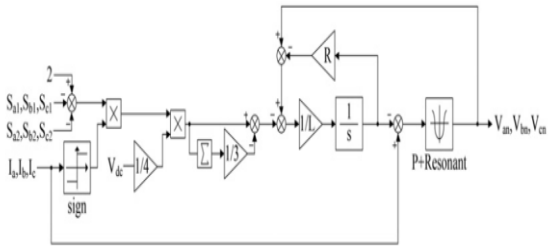

Fig 6: Grid voltage observer

5. CONCLUSION

The proposed 5L-M2UPFR method provides higher reliability of three phase power supply at extreme unbalanced condition of grid. The reduction in sensor improves system failures and by this method unity power factor with less total harmonics distortion is obtained. Most important is that we can design light weight and high power density using this method.

ACKNOWLEDGEMENT

Expression of giving thanks are just a part of those feeling which are too large for words, but shall remain as memories of wonderful people with whom I have got the pleasure of working during the completion of this work. I am grateful to RITEE, Raipur (C.G.) which helped me to complete my work by giving encouraging environment. I would like to express my deep and sincere gratitude to my supervisor, Associate Professor Ritesh Diwan . His/her wide knowledge and his logical way of thinking have been of great value for me. His/her understanding, encouraging and personal guidance have provided a good basis for the present work.

REFERENCES

[1]. Kouro, S., Malinowski, M., Gopakumar, K., et al.: 'Recent advances and industrial applications of multilevel converters', IEEE Trans. Ind. Electron., 2010, 57, pp. 2553–2580.

[2]. Miranbeigi, M., Iman-Eini, H., Asoodar, M.: 'A new switching strategy for transformer-less back-to-back cascaded H-bridge multilevel converter', IET Power Electron., 2014, 7, pp. 1868–1877.

[3]. Daher, S., Schmid, J., Antunes, F.L.M.: 'Multilevel inverter topologies for stand-alone PV systems', IEEE Trans. Ind. Electron., 2008, 55, pp. 2703–2712.

[4]. Steimer, P.K., Winkelnkemper, M.: Transformerless multi-level converter based medium voltage drives'. 2011 IEEE Energy Conversion Congress and Exposition (ECCE), 2011, pp. 3435–3441.

[5]. Gabriel, O.H.P., Maswood, A.I., Ziyou, L., et al.: 'Input current shaping of five-level multiple-pole VIENNA rectifier topologies with reduced component and better performance'. Presented at the 39th Annual Conf. of the IEEE Industrial Electronics Society, IECON 2013–, 2013.

[6]. Ooi, G.H.P., Maswood, A.I., Ziyou, L.: 'Five-level multiple-pole PWM AC-AC converters with reduced components count', IEEE Trans. Ind. Electron., 2015, 62, pp. 4739–4748.

[7]. Hatti, N., Kondo, Y., Akagi, H.: 'Five-level diode-clamped PWM converters connected back-to-back for motor drives', IEEE Trans. Ind. Appl., 2008, 44, pp. 1268–1276.

[8]. Ajami, A., Shokri, H., Mokhberdoran, A.: 'Parallel switch-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter', IET Power Electron., 2014, 7, pp. 503–514.

[9]. Maswood, A.I., Fangrui, L.: 'A unity-power-factor converter using the synchronous reference-frame-based hysteresis current control', IEEE Trans. Ind. Appl., 2007, 43, pp. 593–599.

[10]. Barbi, I., Batista, F.A.B.: 'Space vector modulation for two-level unidirectional PWM rectifiers', IEEE Trans. Power Electron., 2010, 25, pp. 178–187.

[11]. Raj, P.H., Maswood, A.I., Ooi, G.H.P., et al.: 'Voltage balancing technique in a space vector modulated 5-level multiple-pole multilevel diode clamped inverter', IET Power Electron., 2015, 8, pp. 1263–1272.

[12]. Maswood, A.I., Al-Ammar, E., Liu, F.: 'Average and hysteresis current-controlled three-phase three-level unity power factor rectifier operation and performance', IET Power Electron., 2011, 4, pp. 752–758.

[13]. Fangrui, L., Maswood, A.I.: 'A novel variable hysteresis band current control of three-phase three-level unity PF rectifier with constant switching frequency', IEEE Trans. Power Electron., 2006, 21, pp. 1727–1734.

[14]. Jong-Won, S., Bo-Hyung, C.: 'Digitally implemented average current-mode control in discontinuous conduction mode PFC rectifier', IEEE Trans. Power Electron., 2012, 27, pp. 3363–3373.

[15]. Ide, P., Froehleke, N., Grotstollen, H.: 'Investigation of low cost control schemes for a selected 3-level switched mode rectifier'. Ninteeth Int. Telecommunications Energy Conf., 1997. INTELEC 97, 1997, pp. 413–418.

[16]. Ohnuki, T., Miyashita, O., Lataire, P., et al.: 'Control of a three-phase PWM rectifier using estimated AC-side and DC-side voltages', IEEE Trans. Power Electron., 1999, 14, pp. 222–226.

[17]. Wang, B., Venkataramanan, G., Bendre, A.: 'Unity power factor control for three-phase three-level rectifiers without current sensors', IEEE Trans. Ind. Appl., 2007, 43, pp. 1341–1348.

[18]. Ghosh, R., Narayanan, G.: 'Generalized feed forward control of single-phase PWM rectifiers using disturbance observers', IEEE Trans. Ind. Electron., 2007, 54, pp. 984–993.