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Low Power GasP Circuits using Power Gating

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Abstract - *There are multiple methods to reduce power consumption of digital circuits one of them is power gating. In this project, we are using state preservation technique of power gating to reduce power consumption of GasP family of asynchronous digital circuits. Large amount of power consumption in digital circuits is due to leakage current, as sub threshold conduction, junction leakage, and tunneling leakage through gate oxide. As per result from experiment, it is found that power gating is the most effective method to reduce sub threshold leakage. In power, gating there is a PMOS, a NMOS transistor is used to provide virtual power supply to block which is known as Virtual VDD and Virtual GND. NMOS, and PMOS transistor is known as sleep transistors. The power control logic turns on the power in anticipation of the receiving signal. The power control logic turns off the power when the circuit block is idle because either it is empty or pipeline is obstructed. GasP circuit make possible power gating is used in each stage. A latch is used in this project for storing the data coming from previous stage. This latch is power efficient because it drives only when necessary. It preserve its output and permits power gating.*

Key Words: **GasP, Power Gating, Asynchronous, Lazy Latch, Static Power, Fine Grain Power Gating, Conventional Latch, Power GasP** etc…

1. INTRODUCTION

As continuously, size of electronics devices get reduce using different process technologies which significantly improves chip performance and increase the density which allows more and more computation in small area.
Due to technology, scaling power consumption is significantly increased. Now a day's battery life is cited requirement for daily electronics gadgets like cell phone and laptops. Also in server and advanced computing machine. More power consumption leads to heating which require expensive cooling techniques.
Due to all these factor design engineers need to focus on low power design techniques for digital circuits.
Power consumption in digital circuits are many of two types: dynamic power and static power consumption. Charging and discharging of transistor capacitance and wire capacitance leads to dynamic power consumption.
Technology scaling requires reducing power supply voltage to avoid the destruction of transistors due to high electric field. Supply voltage scaling also saves significant amount of dynamic power but at the cost of performance. To maintain performance threshold voltage should be scaled. Threshold voltage and leakage have an exponential relationship. Due to which leakage power, commonly known as static power, is become large fraction of total l power consumption.
Power gating is best method to achieve low power performance. When circuit is idle or in sleep mode, power to the circuit is switched OFF by controlling an additional transistor known as sleep transistor. By power, gating leakage power is reduced because power is proportional to square of supply voltage. Further leakage power can be reduce by using high threshold voltage transistors as sleep transistors and low threshold voltage transistors for logic implementation while maintaining performance.

1.1 BRIEF DESCRIPTITION

We are using stage-preserving technique of power gating for GasP family of asynchronous digital circuits to achieve power savings. The techniques used achieve power savings by reducing the sub threshold leakage in the idle state of circuit. Additional transistors are inserted between the supply and the circuit. When the circuit is idle, the additional transistors cut-off the power to the circuit. By turning OFF the power, supply to the circuit voltage at different node of circuit is reduced. Sub threshold leakage in a transistor is dependent on the voltage across it. Turning the power OFF to the circuit to reduce leakage power is known as power gating.
Due to the turning OFF the power loss of states in pipeline may occur. Special circuit is used for each stage to avoid the loss of state. The stages are turned ON in prevision of the incoming data. The power for each stage is restored when the latches are active. We turn OFF power supply of individual stage due to which no data is loss of state and power is turn on only when it is required.

2. METHODOLOGY

New Fine-grain power gating technique is designed to achieve idle state power saving in GasP asynchronous circuits. Pipeline stage is control by GasP circuits. Using fine grain technique, we can turn OFF power to the idle part of pipeline. In this technique a PMOS and a NMOS transistor is inserted as sleep transistor. Fine grain power gating controls the power of each and individual stage of pipeline. When pipeline is empty then individual stages are turned OFF. In

this technique power is turned OFF even pipeline is full. The power is turned off for combinational circuit and latches. Each stage of pipeline is divided in three parts:

1. Power-gating Block: Sleep transistors are present in this block to turn off and on the power.
2. Power GasP circuit: This circuit is use for sequencing the data through the latches and generates power control signal.
3. Latches and combinational circuits: These circuits are used for storing the data and they must be power gated.

Power-GasP circuit has the logic required to generate the sleep signal. This is referring as power control signal in this paper. Power control signal drives the sleep transistor in power gating block. Power gating block provides virtual power supplies, Vvdd and Vgnd. These power supplies are used for the latches and the combinational circuits of that stage. The Power-GasP circuit is powered from regular power supply.

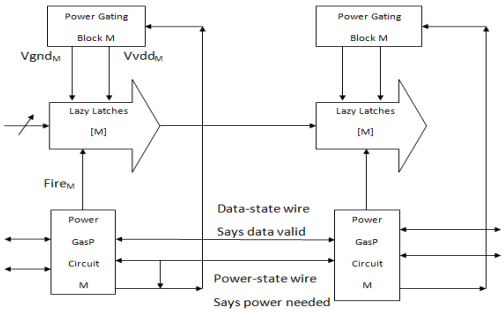


Fig -1 block diagram

2.1 Power GasP circuit

Traditional GasP circuit is modified to include power gating logic and we called it Power GasP circuit. Power Gasp circuit generates power control signal, state wire and fire signal. The power control signal slowly turns OFF the power to the latches but quickly turns ON power to avoid data loss.
Every Power GasP circuit drives latches and consists of two state wires, a Data state wire and Power state wire.

1. Data state wire: This indicates the presence or absence of data between the stages of Power Gasp circuits. Data state wire is same as the state wires of traditional GasP circuit. When the predecessor state wire is HI or FULL and the successor state wire is LO or EMPTY, the Power GasP circuit is said fire. The predecessor driver from one end and the successor driver from the other end drive the data state wire.
2. Power state wire: For power gating, we add a second state wire, the power-state wire. When the power state wire is HI, power should be applied to the latches and combinational logic associated with the latches. When the power state wire is LO, power may be interrupted and the sleep transistors may be turned off to allow the gated power supply to decay. The powerOn driver C drives the power-state wire HI from one end, whereas the powerOff driver D of the next stage drives the power-state wire LO from the other end.

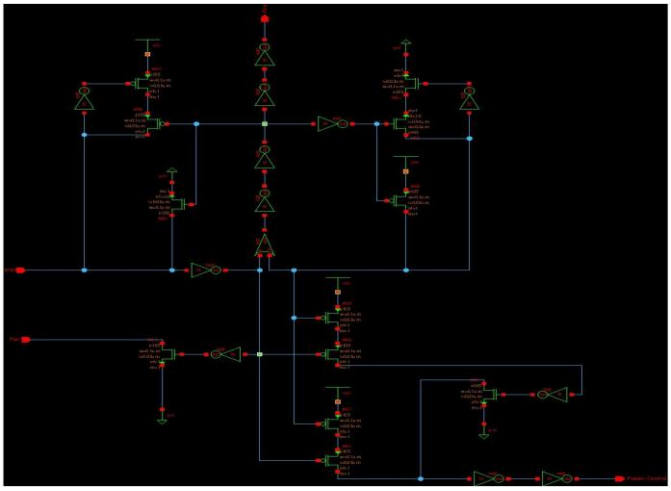


Fig -2: Power GasP

2.2 POWER gating block

The power-gating block, controlled by the power-control signal from the Power-GasP circuit, provides power for the latches and combinational circuits. The power-gating block consists of sleep transistors. In this power gating technique two sleep transistors are used, one is PMOS transistor, the header, and other is NMOS transistor, the footer. The drain of the PMOS transistor or header acts as the new power supply, called Virtual Vdd or Vvdd. The drain of the NMOS transistor acts as the new ground, called Virtual Gnd or Vgnd. The latches and the combinational circuits are power from the new supplies, Vvdd and Vgnd.
The power control signal, which is generated in the Power GasP circuit, is input for the power-gating block. When the power-control signal is high, the sleep transistors are turned ON quickly whereas when the power-control signal is low the sleep transistor is turned OFF slowly.

2.3 Lazy Latch

Lazy latch has two inputs. Data from previous pipeline stage and fire signal from the corresponding GasP module. The lazy latch mainly consists of three parts in following order parts: (1) Switch (2) Amplifier and (3) Keeper. A switch consists of 3-input NAND gate and 3- input NOR gate. The amplifier consists of a wide PMOS transistor and a wide NMOS transistor. Keeper and a chain of inverters to carry the output state back to the switch. The latch output is fed back to the switch, where it can participates in determining when the latch should drive its output.

The keeper in the latch drives the output when the amplifier transistors in the latch stop driving the latch output. When the data at the latch input and output match, the amplifier transistors are turned OFF. The keeper then takes over and preserves the state.

If amplifier stops driving the latch output, the keeper drives the output. Therefore, when the latch output equal to latch input, the amplifier transistors are turned OFF and keeper takes over to keeper the state. However, in the Lazy latch, if the power is turned OFF then keeper maintains the state of the latch.

The output signal passes through three inverters before going back to the switch of the latch. This completes a ring with five inverters. Five inverters in the ring relax the sizing constraints. The duration of five inverters, allow sufficient time for the output to attain the supply rail before keeper drives it.

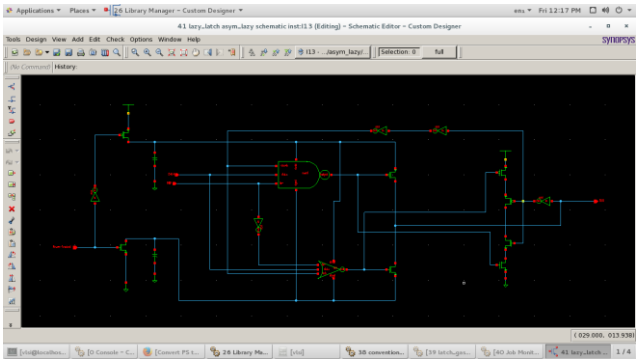


Fig -3: Lazy latch

2.4 GasP circuits

The GasP family of asynchronous circuits provides a control for simple pipelines, for branching and joining pipelines and for join on demand through arbitration. Two GasP modules connected by a single wire W called the state wire. GasP utilizes the wire capacitance for storing states instead of flip-flops and latches used to store state conventionally. A GasP module switches when its predecessor stage has new data to proffer to the successor stage. The necessary condition for switching is: predecessor stage is FULL and successor stage is EMPTY. Various convention used is: HI is FULL and LO is EMPTY.

The condition, predecessor is FULL and successor is EMPTY, is detected by an AND gate. When pred1 is HI and succ1 is LO, MODULE 1 is triggered and generates a fire signal, fire1, an ACTIVE high signal. A GasP module must achieve three things when it fires: (1) it must make data latches momentarily transparent, (2) it must declare its successor data wires FULL, and (3) it must declare its predecessor data wires EMPTY. So fire1 is followed by succ1 going HI and pred1 GOING LO. So the very condition that caused the fire signal is destroyed by the fire signal. The fire signal remains HI for five gate delays. It is responsibility of latches to transfer data in this time.

The GasP circuit in the figure is a 6-4 GasP circuit. It takes six gate delays from predecessor FULL to successor FULL. This is called forward latency. Also, it takes four gate delays from successor EMPTY to predecessor EMPTY. This is called reverse latency. Hence the name 6-4 GasP.

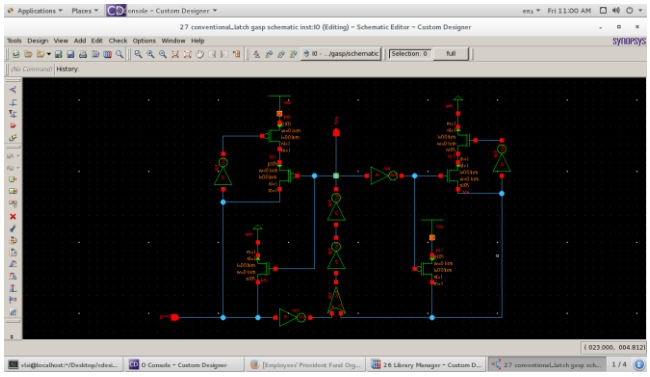


Fig -4: GasP circuit

2.5 Conventional latch

The Conventional latch consists of three parts in the following order: (1) Switch (2) Keeper (3) Amplifier. Data is the latch input, out is the latch output and fire is an input signal from the corresponding GasP module. The switch consists of inverter I and passes transistors N1 and N2. The fire signal from the GasP module controls the pass transistors. When the fire signal is high, the pass transistors transfer the input to the output. The amplifier consists of an inverter with wide transistors to drive the large fan-out. The keeper consists of a back-to-back inverter.

To achieve maximum power savings during power gating, amplifier transistors can be power gated. In the event of power gating, however, the latch output will be lost. The keeper keeps the state but fails to maintain the latch output because the amplifier is power gated. Using power gating with the Conventional latch requires retention logic to retain the state once the power is restored. Additional startup time is associated with the retention logic. In addition, a power gated latch stage may provide undefined input to the next stage. Undefined inputs may cause issues like short circuit current in the next stage. Isolation logic is required to avoid providing undefined inputs to the next stage.

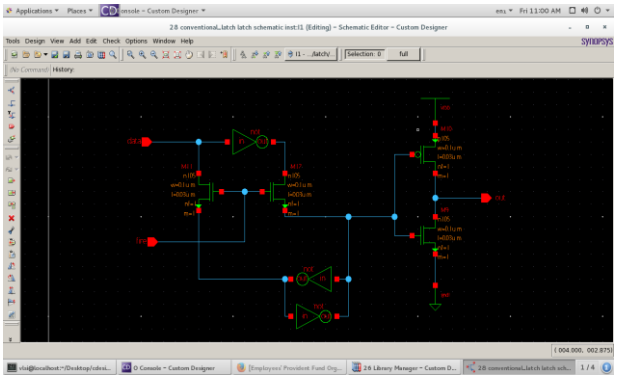
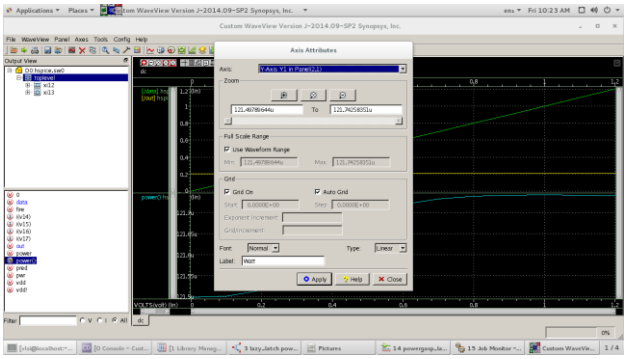


Fig -5: Conventional latch.

3. RESULTS

By comparing the results of conventional latch with GasP circuit to lazy latch with power GasP using power gating, I found that total power consumption in power GasP is 3.9n Watt and for conventional latch with GasP circuit is147.5 n Watt.



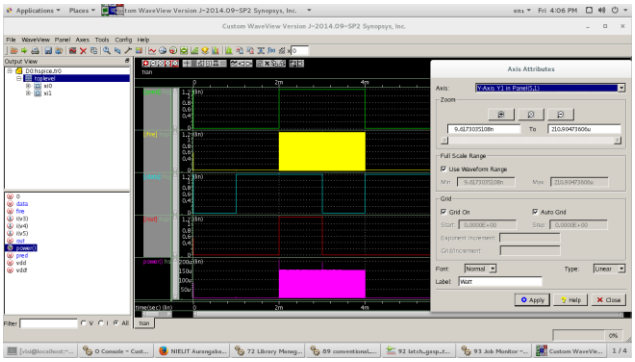
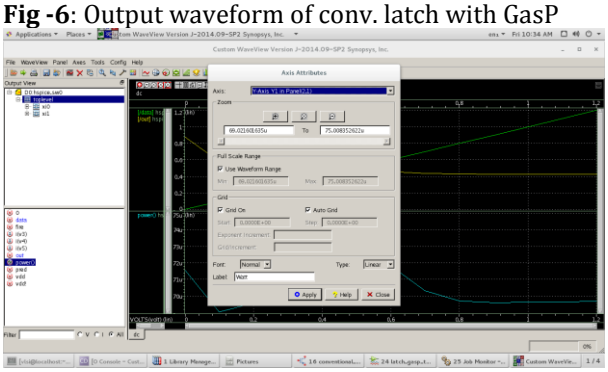


Fig -6: Output waveform of conv. latch with GasP



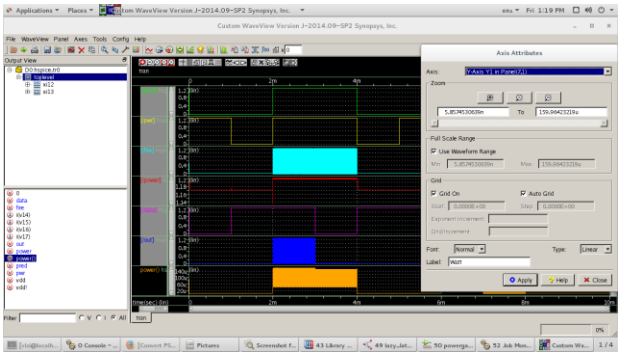


Fig -7: Output waveform of lazy latch with power GasP

Table-1: Comparison of power required

S.No.		Lazy latch with power GasP	Conventional latch with GasP
1.	DC power	69u watt	121.4u watt
2.	Total power	5.8n Watt	9.6n watt

3. CONCLUSIONS

Fine-grained power gating technique for the GasP family of asynchronous circuits is used in this paper. Fine-grained power gating can control power for each stage in the pipeline. The sleep transistors for each stage control the power to that stage and its combinational circuit. The power to the stage is turned ON in anticipation of receiving data. The power is turned OFF as long as the stage is idle either because it is empty or because the pipeline is clogged. The control circuit for implementing power gating is simple.
In this paper a new state wire called power-state wire, in addition to the traditional data state wire. The two state wires determine the requirement of power for each stage. A new power-control signal actually turns ON and OFF the sleep transistors to power the stage.
Lazy latch is introduced in this paper which keeps the state in the event of power gating. The Lazy latch drives it output only when necessary. The Lazy latch offers reduced power consumption in active and idle periods of operation.

Power gating is evaluated for the Lazy latch. This paper compares a Power-gated pipeline consisting of the power-gated Lazy latches and a Conventional pipeline consisting of non-power gated Conventional latches. The reduced load offered by the Lazy latch and turning OFF of the amplifier transistors when unnecessary achieves 39.5% power savings during active period. If no work is done for a long time then energy is saved. Energy savings achieved during idle period depends on the duration of the inactivity. The longer the inactive period the more the energy savings achieved.

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