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Design and Implementation of Two Stage CMOS Operational Amplifier

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Abstract - *A method for fabricating and implementing a Two Stage CMOS Operational Amplifier using Cadence Virtuoso 180nm Technology is presented in this paper. The proposed CMOS op-amp is designed for 1.8V power supply. Op-Amp is basically a DC-coupled high-gain electronic voltage amplifier having differential input signals and, generally a single-ended output waveform. Operational amplifiers are basically utilized to perform mathematical operations such as addition, subtraction, multiplication and division in many linear, non-linear and frequency-dependent circuits. Op-amp is widely utilized as a building block in integrated circuits because of its versatile nature. Various performance parameters such as Gain, Phase Margin, Gain Bandwidth, Common Mode Rejection Ratio, Power dissipation etc have been evaluated.*

Key Words: **Operational amplifier, Bandwidth, Gain, Power dissipation, CMMR**

1. INTRODUCTION

The operational amplifier is a standout amongst the most helpful gadgets in simple electronic hardware. Operational Amplifiers all the more regularly known as, Op-amps are worked with various levels of many-sided quality to be utilized to acknowledge capacities going from a straightforward dc inclination era to rapid enhancements or separating. Operation amps, are among the most broadly utilized building hinders in Analog and Digital Electronic Circuits and are most generally utilized as a part of buyer, electrical and logical gadgets. They have wide applications in numerous simple circuit including square wave generators, exchanged capacitor channels, sigma delta A/D converter, test and hold speakers and so forth.

The pattern towards low power, low voltage silicon chip frameworks has been becoming because of the expanding interest of littler size and longer battery life for compact applications in all promoting portions including media communications, restorative, PCs and buyer gadgets. Operation amps are direct gadgets which have about every one of the properties required for perfect DC amplification as well as are utilized broadly for output waveform molding, sifting and for performing scientific operations, for example, logarithm, expansion, subtraction, reconciliation, separation and so on.

2. DESIGN METHODOLOGY OF OP-AMP

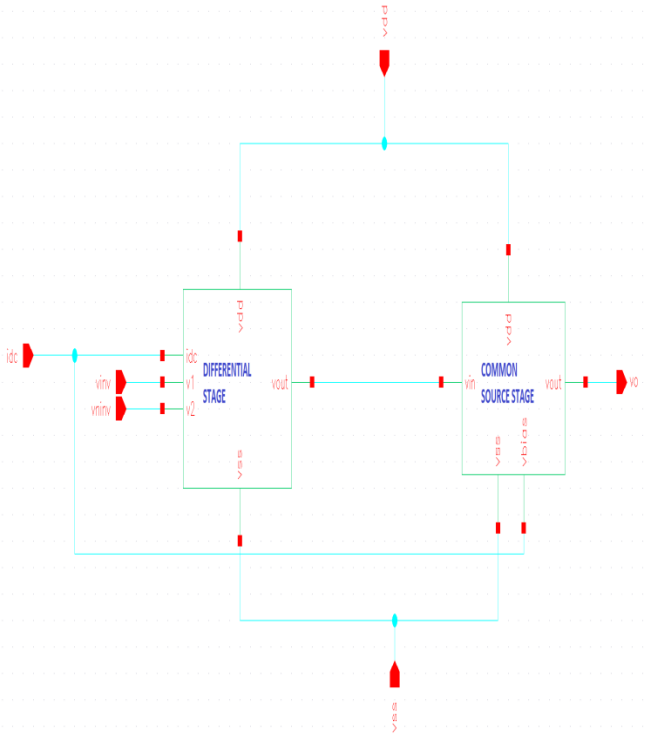

Fig -1: Schematic of two - stage Operational Amplifier

Two phase operational intensifiers comprise of a differential amplifier in the primary stage taken after by a Common Source Amplifier in the second stage. Differential Amplifier organize guarantees high pick up and Common Source Amplifier arrange additionally expands the gain and furthermore gives high yield voltage swing. The two phase operational speaker is appeared in Fig -1.

The main square is a differential amplifier. It has two data sources, an altering input and non-reversing input. It gives a differential voltage or single finished voltage, contingent upon the setup at the yield which relies on upon differential info voltage. Single finished yield corrupts the yield swing of the enhancer. As the symmetry of the circuit is lost, the Common Mode Rejection Ratio debases.

In circuits where the gain given by the differential intensifier organize is insufficient, extra enhancement required is given by the second stage, i.e. the basic source amplifier, driven by the yield of the principal arrange. The biasing circuit gives the best possible working point to

every transistor in its immersion area. A yield support stage can be appended toward the end to give the low yield impedance and bigger yield current expected to drive the heap. For a little capacitive load yield cradle is not required. At the point when the yield support organize is not utilized, the circuit goes about as an Operational Trans-conductance Amplifier or OTA.

The basic architecture of two stage operational amplifier consists of following two parts [5]:

2.1 Dual Input Differential Amplifier

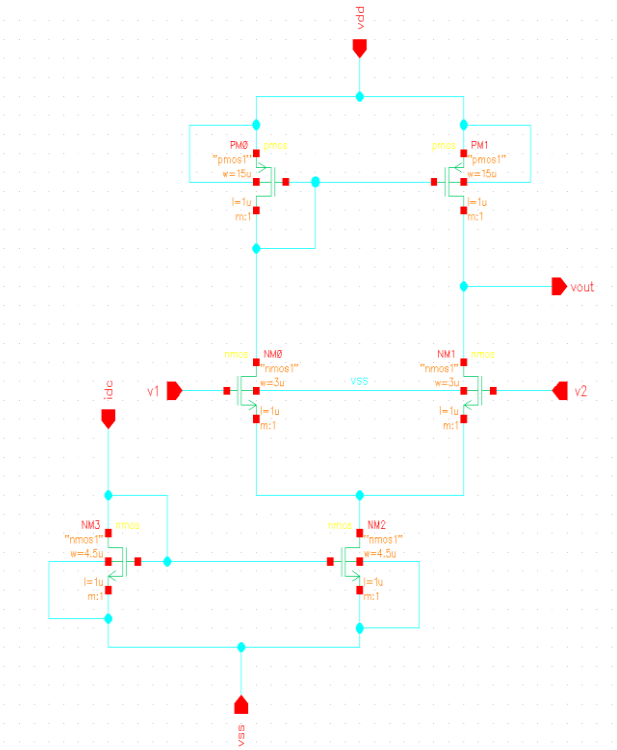

Fig -2.1: Schematic of Differential Amplifier

Fig -2.1 shows active load differential amplifier. All the transistors are in saturation mode in this amplifier as gain is higher in saturation region than triode region. For transistors to work in saturation mode, drain voltage must always be more than gate voltage minus threshold voltage. PM0 and PM1 form a current mirror. NM0 and NM1 form differential pair. NM2 and NM3 are used to provide biasing to this amplifier. Body of all the transistors are connected with their source. Current from NM2 will diving equally in two arms of PM0, NM0 and PM1, NM1. NM2 and NM3 are connected to V_{SS} and PM0 and PM1 are connected to V_{DD}.

2.2 Common Source Amplifier

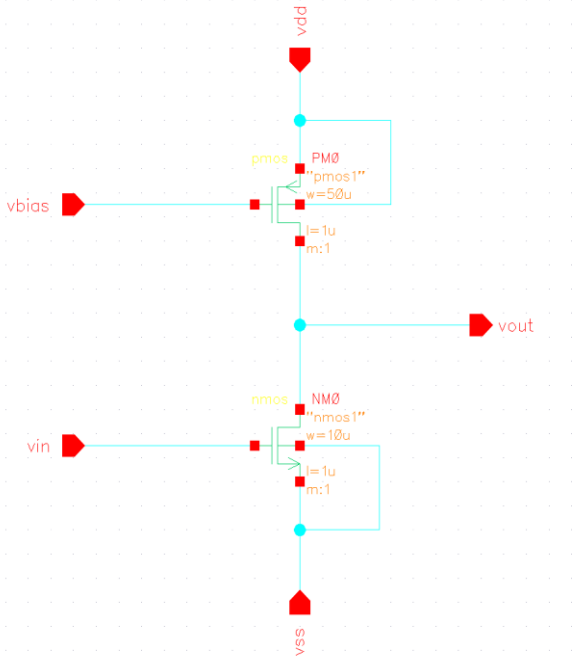

Fig -2.2: Schematic of Common Source Amplifier

Common source amplifier is the second stage used in the design of op-amp. This stage is used to improve gain and output swing of the first stage i.e. differential stage. The cadence schematic implementation of common source amplifier is shown in Fig -2.2. In this amplifier input voltage is given to NM0 and biasing voltage is given to PM0. Source and body and connected with each other. PM0 is given supply voltage V_{DD} and NM0 is provided ground voltage V_{SS}.

2.3 Characteristic Features of OP-AMP

I. **Open loop gain**: When there is no positive or negative feedback given in the circuit then obtained gain is known as open loop gain. An ideal op-amp has infinite open loop gain.

II. **Common mode gain:** When same voltage is applied on both the terminals of operational amplifier, the ratio of output to input voltage calculated is known as common mode gain of operation amp.

III. **Common mode rejection ratio:** Common mode rejection ratio (CMRR) is the ratio of common mode to differential mode gain. In a perfect world this proportion would be endless with common mode a voltage being completely dismisses.

IV. **Slew rate:** When there is step change in input then corresponding to that rate of change in output voltage is known as slew rate of the

operation amplifier. It is by and large communicated in the units of V/μ sec.

$$Slew\ rate\ SR = \frac{Io}{Cc}$$

V. **Common mode voltage range (CMVR):** The scope of common mode signals applied at input of operational amplifier for which its operation remains linear is known as CMVR (common mode voltage range).

$$ICMR(-) = [\sqrt{\frac{2ID1}{\beta 1}} + Vt_1]_{max} + V_{dsat}$$

$$ICMR(+) = [VDD - \sqrt{\frac{2Io}{\beta 3}} + |Vt_3|]_{min} + Vt_{1min}$$

VI. **Unity gain bandwidth:** The scope of frequencies inside which the open-circle voltage enhancement is more prominent that solidarity is eluded as the unity gain bandwidth of the operation amp.

$$\text{Gain bandwidth GB} = \frac{gm1}{Cc}$$

VII. **Total power dissipation:** The aggregate dc control provided to the gadget less any power conveyed from the gadget to a heap is known as aggregate power dissipation of the operation amp.

At no load,

PD = VDD * I.

3. SIMULATION RESULTS AND WAVEFORMS

3.1 Transient Analysis

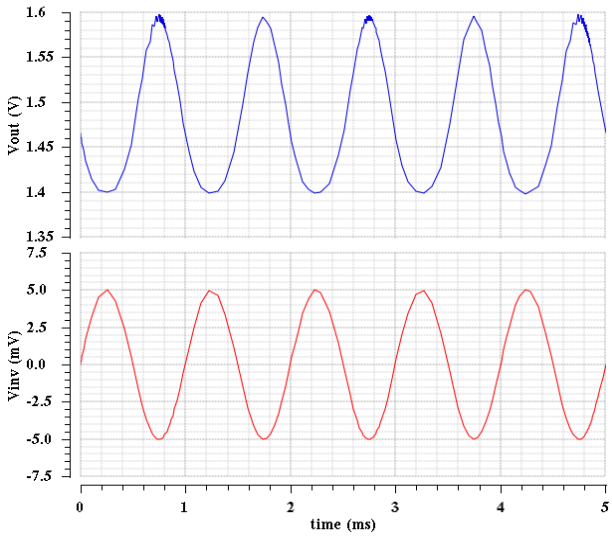

Fig -3.1: Transient response of op-amp in 180nm technology

The sinusoidal input signal having frequency 1k, offset 0V, Ac magnitude 2V, and amplitude 5m is provided.

3.2 DC Analysis

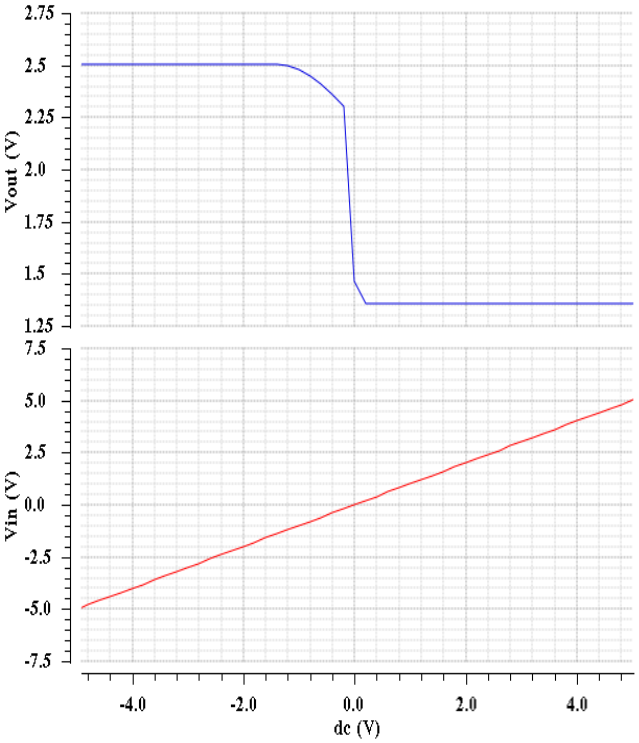

Fig -3.2: DC response of op-amp in 180nm technology

3.3 AC Analysis

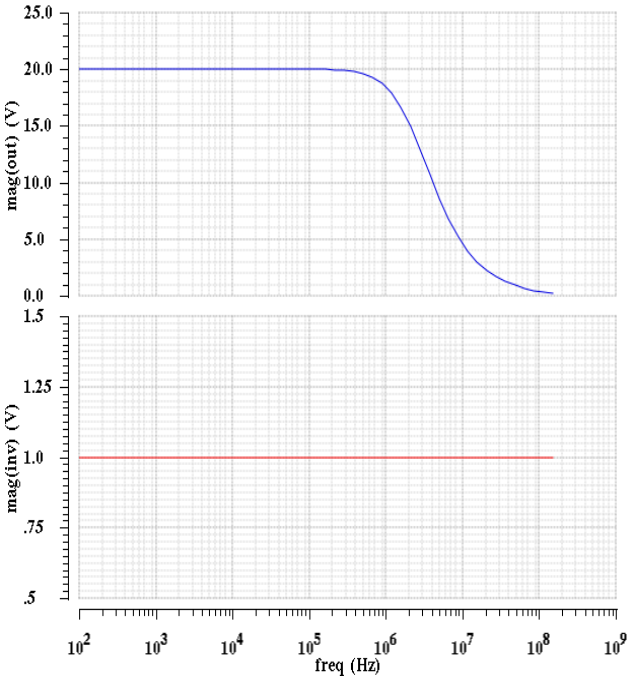

Fig -3.3: AC response of op-amp in 180nm technology

The AC analysis is used to figure out the change in the output when input is supplied with AC signals. AC analysis is used to figure out the frequency response of the circuit.

Table -1: SIMULATION RESULTS OF OP-AMP

Parameters	This work
Technology (µm)	.18
Tool used	Cadence
Power supply (V)	2.5
Bias current (µA)	5
Bandwidth (Mhz)	5
Gain (dB)	30
Slew rate (V/µs)	5
Power consumption (mW)	.11

3.4 Layout Design

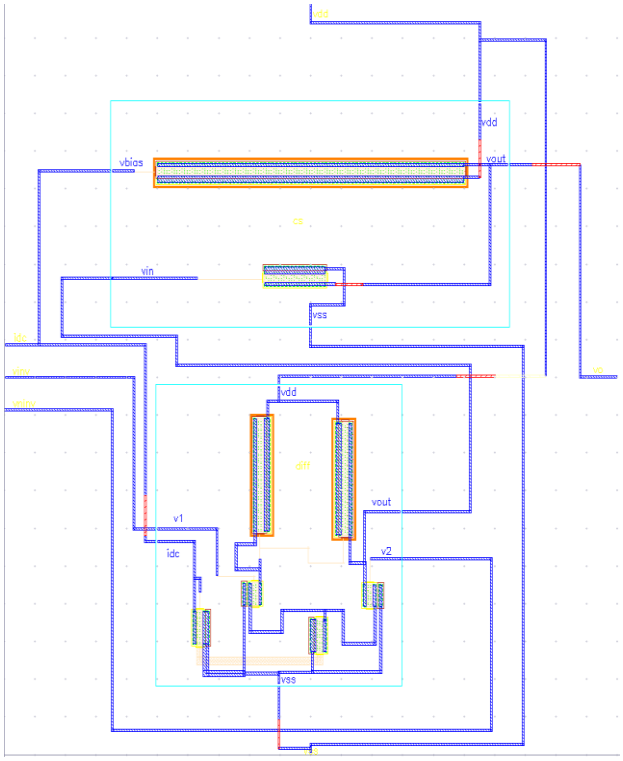

Fig -3.4: Layout design of op-amp in 180nm technology

4. CONCLUSIONS

Two Stage CMOS Operational Amplifier has been fabricated, simulated, analyzed and implemented using cadence Virtuoso in 180nm technology. The proposed design operates for power supply in the range 1.2-1.8V. Suitable effort has been done to evaluate and certain improvements have been made to the important performance parameters such as total gain, phase margin, bandwidth. The op-amp has been fabricated is providing performance parameters with gain 44.98 dB, phase margin 63.85 deg, Gain Bandwidth Product 33.4 MHz, power consumption 310µW which are the basic characteristics of operational amplifier to be relevant for commercial use.

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