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SERDES Design Challenges and their Implications on PCB

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Abstract - *This paper reviews how the high speed 28 Gbps signal travels through the different interconnects like Vias, connectors in PCB and some of the case studies to reduce the Insertion loss < -2dB and Return loss > -8dB which occurs when signal traveling through the interconnects by performing signal integrity analysis .This has been verified by using HyperLynx tool. The importance of stackup and its design as we go for high data rates greater than 1 Gbps.*

Key Words: Field Solvers, Differential vias, Insertion loss, interconnects, Return loss, Signal integrity, speed signal, Stackup.

1. INTRODUCTION

Signal Integrity (SI) is the analysis; design and validation of interconnect necessary for successful transmission of digital signals between the driver and the receiver. In the real world applications, the signal is composed by the artifacts of printed circuit board (PCB) circuit layout, IC packages, PDN networks and noise from the external source leads to distortion in the parameters of the signal like amplitude, thresholds, signal rise time and fall time, jitter and causes ringing, crosstalk, non-monotonocity, overshoot, under-shoot, noise margin. As specified in the reference book[1] at the higher data rate (> 1Gbps) the parameters in building the stackup like dielectric material, surface roughness of the copper, vias in and connectors plays a very important role in causing logic error and may system fails. In this paper we are mainly concentrating to reduce the channel losses on 28 Gbps SerDes channel signals. So, by tuning some of the above parameters, selecting the optimum trace length, performing back drilling, losses were reduced. The insertion loss (IL) and return loss (RL) of the Channel are measured by extracting the S-parameter by using 3D EM (Electromagnetic) field solvers in HyperLynx tool.

2. IMPLIMENTATION OF THE PROJECT

Here we performed SI analysis on the 28 Gbps SerDes RX and TX channels by tuning some of the parameters like PCB material, length of the transmission path, solder mask, surface roughness and differential via design in order to achieve insertion loss of < -2dB and return loss of > -8 dB.

1.1 STACKUP

PCB stackup can be defined as the substrate on which the signal and power layers are arranged in a proper way in order to meet the performance needs (electrical and mechanical) for a specific design. And this planning of stackup is very important to get the best performance of the product. And the Signal Integrity, Crosstalk, Electromagnetic Interference and Manufacturing Costs are the four key things to be considered when designing a good stackup for a printed circuit board. And for the overall system performance, PCB stackup plays an important role in the high speed interconnect transceiver technology. The poor dielectric materials in the PCB stackup design will affect signal during transmission. So, the good dielectric materials with less loss tangent should be selected while designing the PCB stackup which is as shown in below table 1.

Table -1: Material Dielectric Constant and Loss Tangent

Material	εr	Tan(δ)
Typical FR4	4	0.02
GETEK	3.9	0.01
Isola 370HR	4.17	0.016
Isola FR406	4.29	0.014
Isola FR408	3.70	0.011
Megtron 6	3.4	0.002
Nelco 4000-6	4.12	0.012
Nelco 4000-13 EP	3.7	0.009
Nelco 4000-13 EP SI	3.2	0.008
Rogers 4350B	3.48	0.0037

1.2 Choice of the material for the stackup design

As the data rate increases proportionally material loss also increases. So here we selected Rogers RO3003 & RO4450B material to design the stackup to reduce the

impedance mismatch which gives very less loss tangent and dielectric absorption. By using Rogers's material we created the 10 layer hybrid stackup in HyperLynx tool which is shown in below Figure 1.

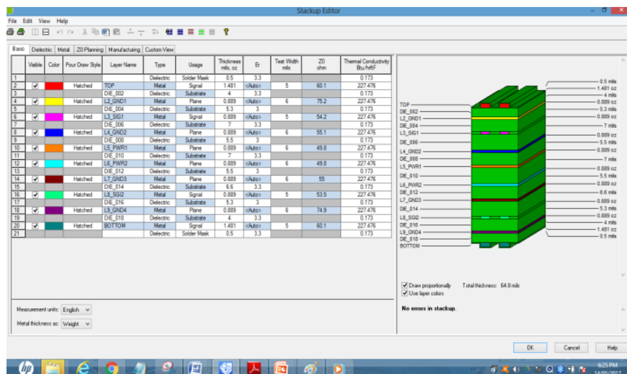

Fig -1: 10 Layer Hybrid Stackup

1.3 Selection of transmission path length

Path loss increases proportionally as the transmission path length increases. Due to this we simulate the RX/TX channel with three different optimum lengths shown in below table 2, RX topology shown in figure 2 and IL and RL graph in figure 3a, 3b.

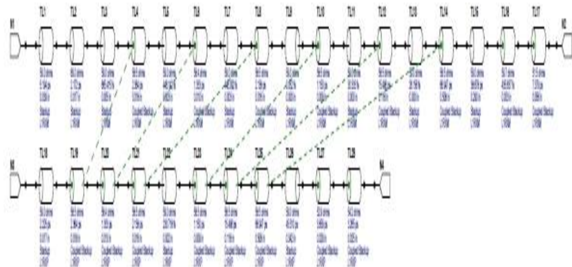

Fig -2: RX/TX topology

Table -2: Different transmission path lengths

Simulation results with different transmission path lengths		
lengths	IL (dB)	RL (dB)
~1.4 inch	1.5	13.5
~2.0 inch	1.7	13.4
~2.4 inch	1.9	13.3

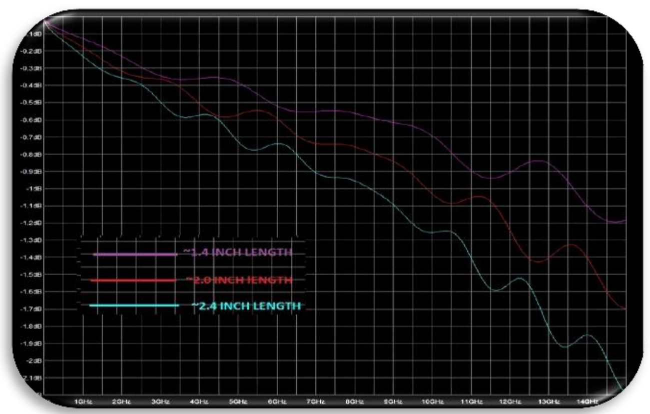

Fig -3a: Insertion loss

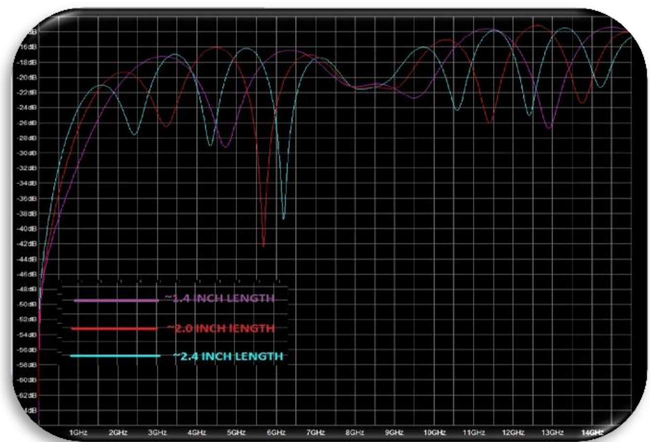

Fig -3b: Return loss

From this simulation results we decided that 1.4" is the optimum transmission path length for the RX/TX channel.

1.4 Effect of Solder mask

Effect of solder mask will be more when the thickness of the copper trace is very less. And as the copper thickness increases effect of solder mask will be no more. This will mainly used on the top and bottom of the stackup in order to provide protection against oxidation. So, by simulating the RX/TX channel without solder mask will get good IL and RL loss.

Insertion loss: .5 dB
Return loss: 12.5 dB

1.5 Effect of Surface roughness

As the operating frequency increases, along with the dielectric loss skin effect also increases hence overall total loss increases. This is mainly due to the surface roughness of the copper which leads to increase in insertion loss. By using 2.1um on dielectric side & 0.5um on top side of the

Rogers 3003 ED Copper, insertion loss is reduced upto -.95dB.

1.6 Simulation with Differential Vias

In a multi-layer PCB (Printed Circuit Board) via is the electrical connection between traces or between different layers. And at the higher data rates differential vias will be used to reduce the capacitive and inductive loss. By reducing capture pads, eliminating the NFPs (non-functional pads) and by increasing the anti-pads C-via is minimized and L-via is minimized by removing the extra stub by performing backdrilling using HyperLynx full-wave 3D field simulator. This greatly reduces the insertion and return loss. The below graphs 4 shows the Insertion loss= -2.7 dB and Return loss= -8.04 dB without back drilling.

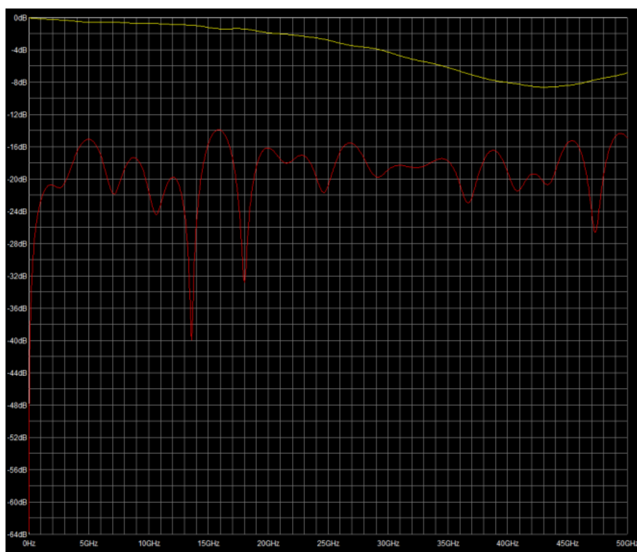

Fig -4: IL (Yellow) and RL (Red) plot

1.7 Backdrilling

Accuracy of the signal integrity simulation can be increased by removing the signal via stubs (Backdrilling) or counter-boring the backside of via in PCB in order to remove the parasitic stub. This reduces the impedance discontinuity caused by via stubs.

1.8 End Results

The below figure 5 shows the IL and RL loss, table 3 shows the comparison results of with and without backdrilling and figure 4 shows the BER (bit-error rate) plot.

Table -2: Simulation results with and without back-drilling

Simulation results with back drilling & without back drilling			
	lengths	IL (dB)	RL(dB)
With Back drilling	~1.4	-1.8	-8.04
without Back drilling	~1.4	-2.7	-5.2

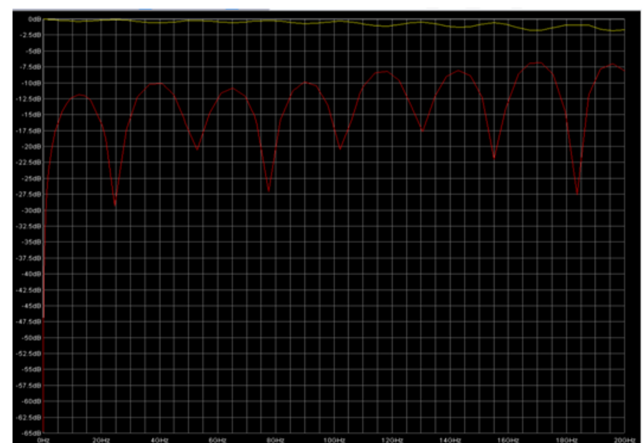

Fig -5: IL (Yellow) and RL (Red) plot

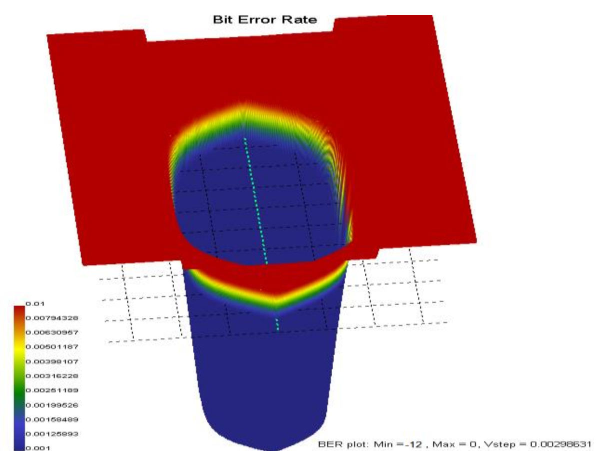

Fig -6: BER plot for 28 Gbps

3. TOOL OVERVIEW

HyperLynx Signal Integrity (SI) generates fast, easy and accurate signal integrity analysis in PCB system design. HyperLynx SI helps the engineers efficiently to manage

rule exploration, definition and validation to ensure that the engineering intent is fully achieved. This software is tightly integrated from schematic design through final layout verification and it can quickly and accurately resolve typical high-speed design effects including overshoot, undershoot, ringing, crosstalk and timing problems.

4. SERDES DESIGN CREATION

HyperLynx SI simulator helps to create and validate designs incorporating the high speed serial channel standards which are now established in every segment of the electronics industry which supports in all popular multi-Gbps SERDES design standards from consumer audio/video, computing, telecommunications and mobile phones. And also provides a fast efficient virtual prototyping environment in order to conduct the pre-layout high speed channel design tuning and models the advanced I/O architectures with pre-emphasis, equalization and complex clock recovery.

3. CONCLUSIONS

Signal Integrity analysis on 28 Gbps serdes TX/RX channel by creating 10 layer hybrid stackup with using Rogers's dielectric material, varying transmission path length, reducing anti-pad size and by performing backdrilling for the differential via we achieved the Insertion loss and Return loss by extracting S-parameters using 3D EM field solvers according to the JEDEC standard specification and bit error rate plot for 28 Gbps is plotted using HyperLynx 3D AMI simulator.

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