

# The Computation Complexity Reduction of 2-D Gaussian Filter

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**ABSTRACT:** Now a days smoothing of the image is becoming a big issue. One of the very useful method to smooth the images is 2-D Gaussian Filter, which is used in Image Processing. However, the heavy computational resources are required by 2-D Gaussian Filter, and it comes down to real-time applications. The efficiency is achieved in this implementation. We use floating point representation, but there are certain problems for the implementation because it requires large computational power in order to achieve real-time image processing. On the other hand a fixed-point approach is much more suitable for the implementation of a 2-D Gaussian filter in FPGA. By using fixed-point arithmetic for the implementation, the efficiency is increased, area is decreased, complexity decreases and computational cost is also reduced.

**Keywords—** LUT-Look up table, real-time Gaussian filter, fixed-point, computational cost

## I. INTRODUCTION

We are living in digital words. Digital world means technical and modern world. The idea of digital image processing are being applied in different fields such as medicine, astronomy, geography, industry, etc. [1]. These fields often require results in real-time, and efficiency in the implementation of digital image processing is imperative. In this paper, we present how the LUT is reduced by the implementation of a 2D Gaussian Filter on an FPGA [2]. Image Processing is processing of images using mathematical operations by using any form of processing for which the input is an image, a series of images, or a video. Image processing are basically a digital processing but optical and analog image are also possible [3]. Computer graphics and computer vision are also related to image processing. Images are manually made from physical models of objects, environments, and lighting, instead of being acquired (via imaging devices such as cameras) from natural scenes, as in most Animated movies [4]. On the other hand computer vision is often considered high-level image processing out of which a machine/computer/software intends to decipher the physical contents of an image or a sequence of images (e.g., videos or 3D full-body magnetic resonance scans) [5]. In this paper we take an example of convolution using FPGA was developed using [3\*3] sobel filter using a [15\*15] image. [6].

The remaining paper is divided into 4 sections. Section 2 covers the theory, Section 3 explains the methodology of

the Gaussian filter; shows a performance of the Gaussian filter and Kernel Quantization; while Section 4 presents the hardware implementation for the Gaussian filter for fixed-point. In Section 5, the results of the filter implementations are discussed and give the conclusion.

## II. THEORY

### I. Role of Filters

For increasing the sharpness and brightness of the image we use a filter circuit. To emphasize a desire features or to remove undesired feature we use filter. Any image can be represented by a matrix of pixels with values ranging from 0 to 255 [7]. For an example we send a [512 x 512] image to the FPGA requires converting that image into a vector of 262144 elements, where DATA is the pixel value and ADDR is the memory address of each pixel [8].

### III. Image Smoothing

Smoothing is the process which is used to control the extent of smoothing because it is a tuning parameter. The main purpose of smoothing is to remove the noise or other unwanted phenomena. In smoothing the images are modifying so that the individual points are noise free. There are two important cause in which smoothing are used that can aid in data analysis [9].

### IV. Sharpening Filters

Image sharpening means to emphasis the shape and drawing the viewer focus. If the high frequencies are attenuated or completely removed, then the visual quality of an image will be poor. In other way we can say that if the high frequency components of an image are used then the quality of the image is improved. Image sharpening means to enhance the highlighted edges and fine details in an image. For effective sharpening process we generally use the high-pass filter operation. Basically linear filter has been used in the implementation of high pass filter [10].

### V Quality and Design Metrics

Various quality and design parameters are used to evaluate the design. This subsection introduces the different quality parameters which are used in our design.

**Mean Error Distance (MED)**

MED is the average error and is another name of mean error. Therefore, MED is equal to mean error.

**Normalized Error Distance (NED)**

NED is the mean error distance divided by the maximum value of original signal. Value of NED is independent of the size of the design and depends only of the kind of architecture. Therefore, NED quantify the error metrics of the technique better than the MED.

**Peak Signal to Noise Ratio (PSNR)**

The peak-signal-to-noise-ratio is the parameter used widely in image/video processing applications to quantify the amount of the noise present in the image and it is equal to the maximum signal power to the noise power.

**Structural Similarity (SSIM)**

The existing quality metrics signifies the quantity of error in the given input signal. In an image, the noise may be perceivable or it may not. If the noise is not perceivable noise will not affect the quality of the image. In order to compute the quality of the image i.e. perceivable errors present in the image a new quality metrics based on structural similarity (SSIM) is used. This quality metrics is becoming more popular in recent years.

**ENERGY SCALABLE GAUSSIAN SMOOTHING FILTER (ES-GSF) ARCHITECTURE**

The modern devices demand reconfigurable architecture due to the ever changing requirement of the real-time applications. Based on the applications and its criticalness, the design should be able to adapt different energy-quality trade-off which is achieve by the energy scalable GSF architecture . This architecture exploits the concept of significant/non-significant coefficients and presented significant and non-significant boundaries as shown in Fig. 1.

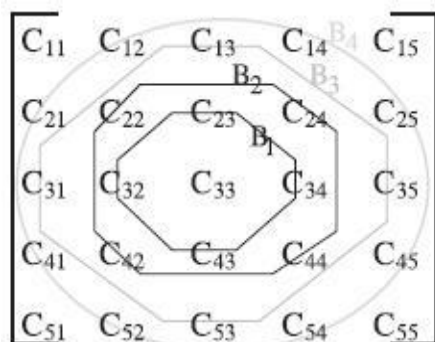


Fig. 1: Kernel coefficient with boundaries.

It observed that value of coefficient decrease from centre to the boundaries therefore, boundary B<sub>1</sub> is more significant (due to having more weight) over the B<sub>4</sub>. The ES-GSF exploits the non-significant boundaries to achieve desired quality energy trade-off. Further, the coefficient of the given boundary is of same value, the resulting architecture will compute sum of all pixel of that boundary and multiplied with the coefficient.

The algorithm accepts image and energy-scalability as input while provide smoothened image as output. In this algorithm, the input image is sub-divided into 5x5 image sub-matrix and these sub-matrices are processed. The algorithm compute approximate kernel based on the given energy budget. Since the kernel considers the significant neighbour pixel in the computation, it provides sufficient output image quality. The architecture that implement the functionality presented in the algorithm is shown in Fig. 2.

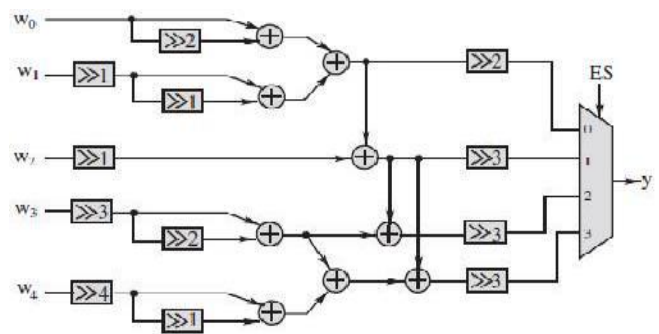


Fig. 2: Architecture of ES-GSF.

**REFERENCES**

1. M. C Hanumantharaju, M. ravishankar, and D.R Rameshbabu, "Design and FPGA Implementation of a 2-D Gaussian Surround Function with Reduced on-chip Memory Utilization" in proc. of the international conference on computer vision, pp 256-259, may 2013.
2. Frank Cabello, Julio Le6n, Yuzolana, Rangel Arthur, " Implementation of Fixes-point 2D Gaussian filter for Image Processing based on FPGA" in proc of IEEE Signal Processing algorithmic, architecture and application" PP 28-33, SEP 2015.
3. P. Burt, "Fast filter transform for image processing," Computer graphics and image processing, vol. 16, no. 1, pp. 20-51, 1981.
4. P. Burt and E. Adelson, "The laplacian pyramid as a compact image code," Communications, IEEE Transactions on, vol. 31, no. 4, pp. 532-540, 1983.
5. D. Alghurair and S. S. Al-Rawi, "Design of Sobel operator using Field Programmable Gate Arrays," in 2013 The International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE). IEEE, May 2013, pp.589-594.

6. V. Sriram and D. Kearney, "A FPGA Implementation of Variable Kernel Convolution," in Eighth International Conference on Parallel and Distributed Computing, Applications and Technologies (PDCAT 2007). University of South Australia: IEEE, Dec. 2007, pp. 105-110.
7. R.E.W Rafael C. Gonzalez, Digital Image Processing using MATLAB, 2009, vol. 24, no.11.
8. D.G. Bailey, Design for Embedded Image Processing on FPGA, 2010.
9. R.Saas and A.G. Schmidt, Embedded systems design with platform FPGAs, 2010.
10. P.Pong, FPGA proto typing by vhdl examples, 2008.
11. V.Pedroni, Digital electronics and Design with VHDL, 2008.
12. C Hanumantharaju, M. Ravishankar, and D. R. Rameshbabu Design of Novel Algorithm and Architecture for Gaussian Based Color Image Enhancement System for Real Time Applications. In Proceedings of International Conference on Advances in Computing, Communication, and Control (ICAC3), Vol. 361, pp. 595-608, 2013.
13. A.Bhatia, W.Synder, and G. Bilbro, "Stacked Integral Image," in Robotics and Automation (ICRA), 2010, pp. 1530-1535.