Design of variable digital FIR filter for software defined radio applications

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Abstract— *this paper describes a reconfigurable hardware Implementation for variable low pass, high pass, band pass and band stop FIR filters. The proposed implementation is based on a MUX based structure for various tap selection, and LUT based approach to select required configurations for each responses .In this way the arithmetic complexity will be reduced. The warped filters, obtained by replacing each unit delay of a digital filter with an all-pass filter, which are widely used for various phase shifting and time delay applications. However, warped filters require first-order and second order all-pass transformation to obtain variable low-pass or high-pass responses, band pass or band stop responses. Here we combine warped filters with the coefficient decimation technique. The proposed architecture is verified through functional verification with the filter coefficients or filter structure.*

Keywords— Coefficient decimation, FDA, variable digital filter (VDF), warped filter

1. Introduction

The design of Variable digital filter (VDF) depends upon the cut-off frequency I?l: and filter coefficients. From the past, several methods are used to design VDF; however one of the most efficient methods is warped filter design which can be obtained by replacing each unit delay of a digital filter with the all-pass structure of an appropriate order. Cut- off frequency of the warped digital filter can be changed by changing the filter coefficients. This design of Warped filters find its application in audio processing such as loudspeaker equalization, linear prediction, spectrally modifying an audio signal ,echo cancellation, detection of band-pass signals in broadband signals, and so on. Depending on the application, digital filters with variable low-pass, high-pass, band-pass, or band-stop responses can be designed. In some application finite-impulse response (F[R) filters are preferred over infinite-impulse response (IIR) filters, because IIR techniques require high precision both in design and in actual operation.

In [5], the concept of warped filters is extended to kautz filter for audio equalizer applications, which proves that the warped FIR filters are better than traditional FIR filters. In [7], adaptive notch filters are designed using the warping technique to detect band-pass signals that are immersed in a broadband signal. These adaptive filters are obtained by using reduced second-order transformation with arbitrary center frequency operations and they provide fixed-bandwidth band-pass responses. [n [8], a filter bank with variable low- pass, band-pass, and high-pass filters are designed using warped filters with different filter coefficients for low-power digital hearing aids. Due to the linear phase characteristics, VDF find its application in communication field. The design complexity of VDFs can be reduced by coefficient decimation. Similarly, many different numbers of approaches is available for VDF design. They include transformation approaches, Farrow structure-based approaches, and frequency response masking-based approach. Farrow structure varies the frequency response of the filter by varying the fractional delay [[]-[4]. Frequency response masking is an efficient scheme for the finite impulse response filter with sharp transition band [5]. However, filters designed using this technique can only adapt to a finite set of cut-off frequencies fc .Digital filters with variable cut-off frequencies i.e. are required in many channelization applications where the operating mode of the system changes dynamically. So it is desirable to design a filter having fc values controlled by the single parameter. The proposed filter and relation between the filter coefficients is presented in section II, section III describes the relation between the filter coefficients and fc. Design example and simulation results are shown in section IV.

2. PROPOSED VDF

Most of the Variable digital filter design is based on the basic principle that the cut-off frequency and the transition bandwidth can be changed by modifying the filter coefficients. The values of filter coefficients depend upon the impulse response which in turn decides the fc cut-off frequency of F[R filter. Also the length of the impulse response depends on the total number of delays in the F[R filter which decides the transition bandwidth of the filter.

The VDF designs in [2]-[6] can be obtained by updating the filter coefficients or expressing it in polynomial forms. However, the desired fc and transition bandwidth is obtained by changing the delay of the FIR filter. In many real time applications it is desirable to change the value of fc with minimum overhead of complexity. This can be achieved by fixed coefficient filter design and changing only the value of the delays which in turn alters the length of the impulse response. The proposed approach results in the digital filter with variable cut-off frequency.

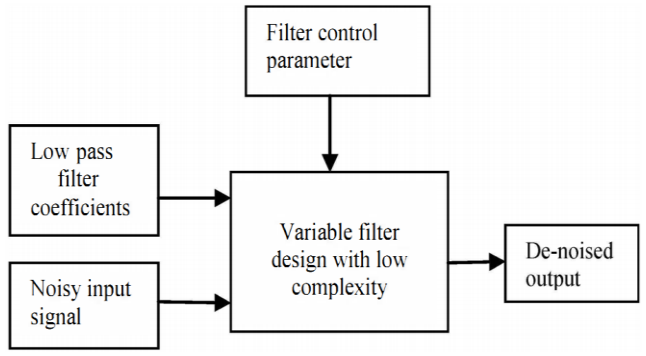
Filter control parameter
Low pass filter coefficients
Noisy input signal
Variable filter design with low complexity
De-noised output

Fig. 1. Variable digital filter

2.1 Design of the Proposed VDF

The first step in the filter design is to determine filter coefficients for original cut-off frequency fc .Let us consider an Nth-order low-pass prototype filter H(z) with cutoff frequency We0 (= 2n feo) and coefficients ho, hI, ... , hn. Keeping the filter coefficients fixed, the cut-off frequency can be varied by introducing an control parameter a. The value of a varies between 0 and 1 because the filter coefficients are fractional values. Convolution of these fractional values with the input data are more complex results in run time errors,that can be minimized by introducing delay values ranging between 0 and 2 with constant increment factor of 0. 5 as shown in Fig 2.

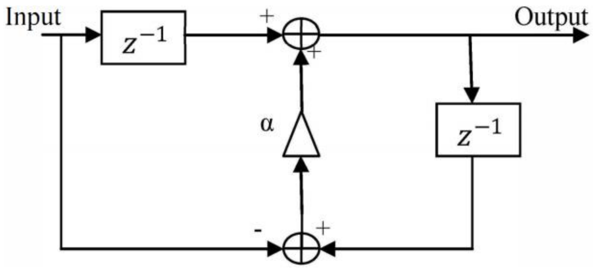

Fig. 2. Prototype filter

Low-pass filter with variable frequency responses are obtained using filter transformation as given by (1).
G(Z) = H(A(z))
Band pass filter is obtained by multiplying the control parameter a with the impulse response and the bandwidth of the filter is control by the decimation factor M. Fixed bandwidth band pass responses at an arbitrary center frequency are obtained using the reduced second order transformation given as [1].
G(Z) = H(B(z))
Where B(z) = -(1/z)A(z)

2.2 Relation between cut-off frequency and transition bandwidth.

The prototype filter consider is low pass filter with original cut-off frequency we0 (= 2 rrfeo) ,by multiplying with control parameter a we get desired set of coefficients. From the a value desired cut -off frequency can be obtained Wca given by the mathematical relation
alpha = - cos(fcenter * pi)

For FIR filter with the fixed coefficients, the product of transition bandwidth TBW and length of the filter responses N is always a constant
TBWD * ND = Constant

Desired cut-off frequency can be calculated from the original cut-off frequency using the following relation.
Fcd = fc/D

From equation (6), it is clear that desired cut-off frequency decrease with increase in D. So by pre-calculating, D value for desired fc pass band frequency and stop band frequency of the model filter is obtained

3. EXISTING ARCHITECTURE

3.1 Introduction

The main functionality of CD selector architecture is to provide a degree of freedom at the user end to select the decimation factor. Depending upon the selected decimation factor, the filter coefficients are decimated. These changes in decimation factors will in-turn aid the user to obtain variable frequency responses for the same filter architecture. Fig. 1 shows the combined hardware architecture for CD-1 and CD-2 technique. In [6], for CD-1 technique, the selection port of array of multiplexers Mux0, Mux1, Mux2..., Mux n in Fig. 1 varies according to the decimation factor to choose between the coefficient value and zero value while the selection port of multiplexers Mux20, Mux21, Mux22 ....,Mux2n remains a constant. In case of CD-2 technique the multiplexer port selection works the other way round where the selection input port of Mux0, Mux1, Mux2..., Mux n remains unchanged while that of Mux20, Mux21, Mux22 ...., Mux2n varies to select between different coefficient values. LUT based method was proposed in the literature [7, 8] for coefficient decimation selection.

3.2 LUT based CD selector technique

Look up table method is the commonly used technique for CD selection [7, 8]. This method stands out for its re-configurability factor as the coefficient selector multiplexer values are stored in look up table (LUT). The hardware architecture of the LUT is as shown in the Fig. 2. In LUT based technique, the decimation selection bits corresponding to decimation factor is stored in a read only memory (ROM). For example, for a decimation factor of M=2 the bit selection pattern will be 1, 0, 1, 0, 1, 0 ...., 1 will be stored in a distinct address location of ROM. The bit length stored in the memory location varies according to the filter length. According to the input memory address to LUT, the stored bit patterns are outputted from LUT. The bit selection values are extracted to the selection of multiplexers using bit slicers. The LUT width will be equal to filter tap length and LUT depth equals to the number of selection patters or decimation choices. The main advantage of this implementation is the degree of reconfigurability. It is possible to store different bit pattern selection in distinct memory location for different decimation factors. The main drawback of this technique is the area consumed increases with the increase in filter tap length as that the width of the LUT increases. The advantage of LUT based decimation selector is that it improves the performance of the system as the bit selection values are pre-stored in the ROM and are readily outputted at any point of time. It has been found that the field programmable gate array (FPGA) resource utilization for this technique increases linearly with the increase in filter order. Thus for a higher order filter, the hardware implementation of LUT based technique accounts for more area and larger utilization of configurable logic block in FPGA. Since it has to be ensured that the stop band and pass band edges of the decimated filter response are well within the normalized range to avoid aliasing, it is not necessary to have very high decimation value. So for a given choice of decimation selector values, the hardware implementation should be reconfigurable for varying filter order. In order to solve these issues we propose a reconfigurable decimation selector implementation that has a constant resource utilization for any filter order and supports a set of required decimation values.

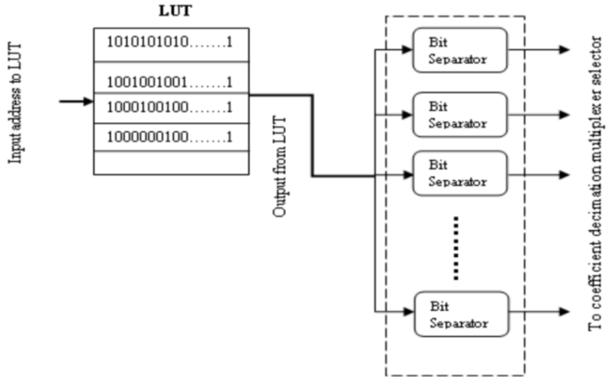

Fig. 3. Existing CD selector

3.3 PROPOSED DECIMATION SELECTOR ARCHITECTURE

The proposed coefficient decimation selector unit employs an array of multiplexers for selecting the necessary coefficients. The proposed technique exploits the pattern redundancy within multiple decimation selection pattern. It has been seen that a set of selection patterns repeats at regular interval for a given set of decimation selector values. For example, a given decimation selection parameters 1, 2, 3 and 4 the multiplexer selection bits repeats after every 12th coefficients. The redundancy in coefficient selection bit pattern will help to reduce the number of multiplexers and eventually reduce the area and power. The bit pattern repetition rate is determined by the least common multiple (LCM) of the provided decimation selection values. As the choice of decimation selection values increases, the repetition frequency also changes according to its LCM. For a multiple decimation selection values of 1, 2, 3, 4, and 5, the pattern redundancy occurs for every 60th coefficient as the LCM of the given decimation selection values is 60. The Table 1 shows the bit pattern nature for the decimation selection parameters 1, 2, 3, and 4. Zooming into the first 12 coefficients, it can be seen that there are only 6 distinct patterns - [1 1 1 1], [1 0 0 0], [1 1 0 0], [1 0 1 0], [1 1 0 1] and [1 1 1 0] that repeats. Within the first 12 coefficients h0 to h11 it can be observed that the pattern distribution is as shown in the Table 2. The observed pattern redundancy for the first 12 coefficient will repeat for the rest of the coefficients in the same manner. Similarly for a 5 input decimation selector unit with 1, 2, 3, 4 and 5 as decimation choices, there are 12 distinct bit selection patterns [1 1 1 1 1], [1 0 0 0 0], [1 1 0 0 0], [1 0 1 0 0], [1 1 0 1 0], [1 0 0 0 1], [1 1 1 0 0], [1 1 0 0 1], [1 1 1 1 0], [1 0 1 0 1] and [1 1 0 1 1] whose pattern repetition occurs at every 60th coefficient.

Fig. 3 shows the proposed decimation selector logic implementation of a 4 input [1,2,3,4] decimation selector. It can be observed that seven 4 input multiplexers are used for realizing the logic, out of which 6 multiplexers are used for implementing the 6 distinct patterns mentioned in the Table 2. Mux A in the Fig. 3 is designed to select different decimation values and depending upon the selected decimation factor different input ports of multiplexers (M1 to M6) is chosen. For example if the Mux A selection is 3 which select the 3nd input port of multiplexers M1, M2, M3, M4, M5 and M6 respectively which will eventually selects the required coefficients h0, h3, h6, h9, h12, h15, h18 etc. Similarly for a decimation selection value of M=2, alternate coefficients are decimated.

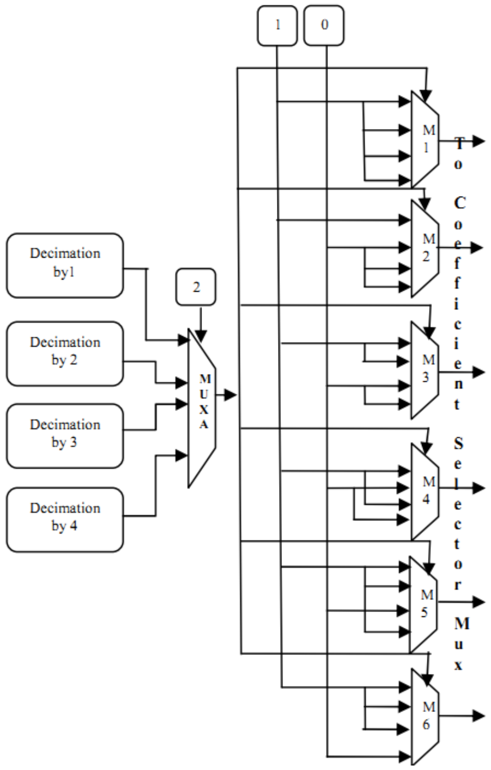

Fig. 4. Mux based CD selector

4. IMPLEMENTATION RESULTS

While comparing the existing LUT based method over the proposed coefficient decimator selector implementation, it can be found that the existing architecture occupies more area and power than the proposed technique. We have implemented all the methods in Virtex IV- xc4vsx35- 10ff668 FPGA. In Fig. 4 shows the plot of FPGA slices consumed with varying filter order for LUT based technique in comparison with the proposed decimation selector. It can be seen that for a proposed reconfigurable decimation selector with a decimation parameter [1 2 3 4 5] the number of CLB slices consumed is 30 which remains unchanged irrespective of the filter order i.e. a given decimation selection hardware can be used for a filter order of length N where the CLB utilization of a LUT based technique increases with increase in the filter order. As shown in Fig. 4 for a filter order varying from 50 to 800, the CLB slices utilized by the existing LUT based hardware implementation varies from 25 to 400.

It can be observed from the Table 3 that the proposed architecture outperforms the LUT based technique by 4.8% area savings and 1.5% power savings for a 33 tap filter. The area and power savings increases to 5.2% and 7.6% respectively for a 101 tap filer. The proposed CD selector architecture slice count remains a constant irrespective of the increased filter order.

Table.1 Comparative Results

	Parameters	Filter order = 33	Filter order = 101
Proposed technique	Total no: of CLB used for entire architecture	1181	3598
	No: of CLB used for CD selector	8	8
	Total Power in mW	0.7048	1.2946
LUT based technique	Total no: of CLB used for entire architecture	1241	3794
	No: of CLB used for CD selector	68	204
	Total Power in mW	0.7123	1.4023

5. CONCLUSION

In this paper we have proposed a low complexity reconfigurable decimation selector for CD architecture using multiplexers. The main objective of the proposed work is to reduce the hardware complexity by making use of the pattern redundancy. The proposed architecture has very low complexity and less power compared to conventional LUT based decimation selector techniques in literature. For a given coefficient decimation selector the proposed reconfigurable decimation selector architecture can be used for N tap FIR filter.

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