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Design Of Low Power High Density SRAM Bit Cell

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Abstract - *Power and area minimization is a critical concern for modern electronic industry. Low power SRAMs are essential in today's electronic gadgets as the demand of battery operated portable devices is increased. This work is the design of a SRAM bit cell for minimizing the area and power consumption. Basic SRAM cell is considerably more complex and occupies a larger area as compared to DRAM cell. Proposed work has a 4 transistor SRAM with approximately 40% less power consumption than that of conventional 6T SRAM. The area also reduced by 35%. 4T SRAM cell have a single access transistor to perform the read write operation. Cadence Virtuoso simulation in standard 180nm CMOS technology confirms all results obtained from this work.*

Key Words: CMOS, 6T SRAM,4T SRAM,180nm,Power consumption

1. INTRODUCTION

Memory structures have become indivisible part of modern VLSI systems. Semiconductor memory is presently not only just stand alone memory chip but also an integral part of complex VLSI systems. The predominant criterion for optimization is often to squeeze in as much as memory as possible in a given area. This trend toward portable computing has led to power issues in memory[1] .The trend of scaling of device sizes, very low threshold voltage, and ultra-thin gate oxide have increasingly been challenged by variability, and therefore, by reliability-related issues. These unwanted variations, in turn, can result in excessive subthreshold leakage, reverse diode leakage, and power dissipation which undesirably affect the stability and energy consumption[2]_[3].

Many modelling techniques have been proposed to minimize the negative impact of process, operation, environmental effects, and/or aging-related variations on energy efficiency, reliability, and yield in SRAM and cache, including chip-area models power/leakage models, access-time models, and failure probability models. Newer techniques can also be used to combat process variations such as adaptive body biasing (ABB) or chip-by-chip resource resizing in various micro-architectural structures . However, these either have inherent costs, must be applied with great caution, or require modification of the chip architecture. Such costly complications demonstrate the importance of inexpensive and early modelling to determine an optimal design that will allow the SRAM to improve its energy efficiency while being more tolerant of variations.

A typical SRAM cell uses two PMOS and two NMOS transistors forming a latch and access transistors. Access transistors enable access to the cell during read and write operations and provide cell isolation. During the unaccessed state an SRAM cell is designed to provide non-destructive read access, write capability and data storage (or data retention) for as long as cell is powered. In general, the cell design must strike a balance between cell area, robustness, speed, leakage and yield. Power cannot be reduced indefinitely without compromising with other parameters like cell area and speed of operation.

In this paper we introduce a design of SRAM bit cell using 4 transistors. In this approach the power and area is efficiently reduced. The main contributions of this paper include: (1)Design of a conventional 6T SRAM in 180nm CMOS technology by Cadence Virtuoso tools.(2)Design for new 4T SRAM bit cell circuit which has lower power consumption and more area efficiency.(3)Design 4T SRAM bit cell with an inverter to improve the performance. (4)The power and area of the conventional 6T SRAM is compared with the proposed 4T SRAM bit cell design.

2. CONVENTIONAL 6T SRAM BIT CELL

SRAM is a bistable element used to data as voltage potential. It consist of a cross coupled inverter. There are different type of SRAM configurations available. Most common one is conventional 6T SRAM .

The basic 6T SRAM cell consist of cross coupled CMOS inverters. The supply current drawn by this 6T SRAM cell is limited to the leakage current of transistors in the stable state. The inverter usually have a large nMOS width as compared to the pMOS width. This often causes switch threshold of inverter to be close to nMOS threshold

voltages. Basic 6T configuration is given below.

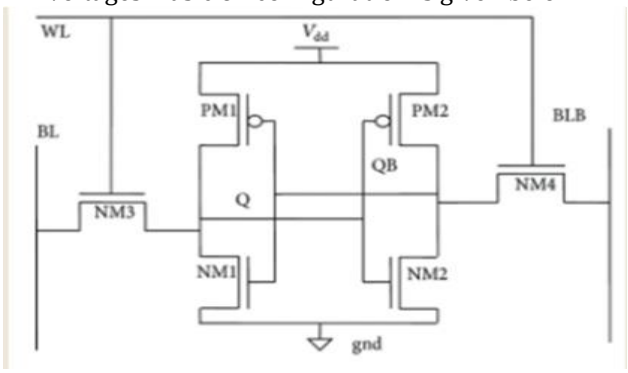

Fig -1 6T SRAM

With the help transistors NM3 and NM4, the data can be either accessed or written into the cell. These two cross-coupled inverters are used for storing one bit of information at a time (either 0 or 1).Data are often written by driving WL high and amplifier driving the lines BL & BLB with knowledge with complementary values. This circuit is designed and implemented using CADENCE VIRTUOSO tool. This circuit is designed using 180nm technology. The schematic is shown in fig.2

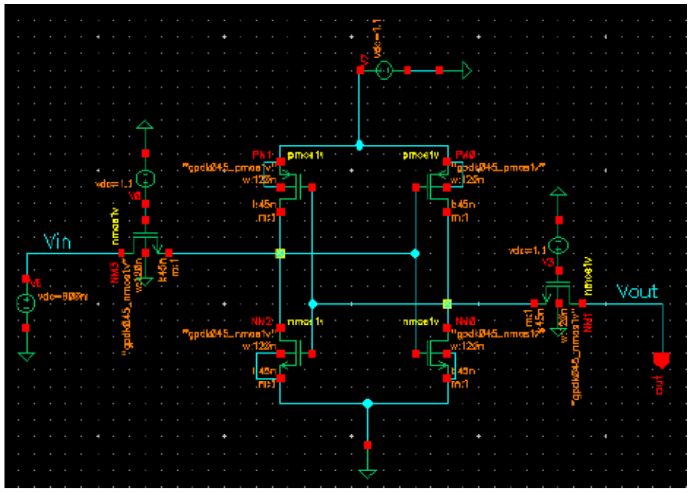

Fig -2 Schematic of 6T SRAM in 180nm

3. PROPOSED 4T SRAM BIT CELL

The proposed SRAM design consist of 4 transistors which will reduce power consumption and also improve area efficiency of memory cell. Here the number of transistors reduced from 6 to 4 by modifying the circuit .The power consumption is further reduced by transistor scaling, i.e., varying the W/L ratio of transistors. Fig.3 shows the proposed circuit diagram of 4T SRAM.

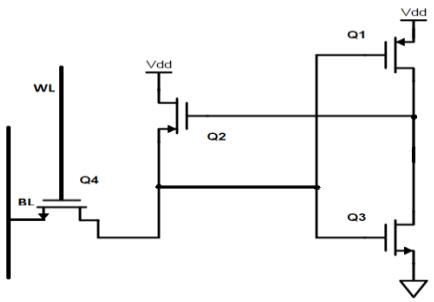

Fig -3 4T SRAM

The design of 4T SRAM is connected with getting an appropriate ratio of pass transistors with respect to pull down transistors, i.e., the aspect ratio of the cell. It is clear that the aspect ratio of the cell should ensure that no time the internal voltages rise to a value large enough to upset the cell state. We should note that energy dissipation due to discharge of bit line capacitance is considerably larger than the energy required to switch the cell.

During READ/WRITE operation, a high-node level in the SRAM cell is lower than a supply voltage (Vdd) by a threshold voltage of the transfer transistor, even though both bit lines are pre charged at Vdd. This is because transfer gates operate as source-follower circuits when the cell is selected. After closing the transfer gate, current through the load element raises the high-node level to (Vdd) but it takes an order of milliseconds since the current is, in most cases, 1–10pA. During this transient time as well as READ/WRITE operation itself, this 4T-SRAM cell is very unstable against noise from peripheral circuits because of less critical charge.

When a “0” is to be written in the cell, the load and driver transistors have to be ON and there is a feedback mechanism between the ST and STB node. So the STB node is pulled to ground by drive transistor and STB node has been pulled to VDD by load transistor. When a “1” has to be written to bit cell the load and driver transistor is made to be OFF.

The read operation is initiated by enabling the word line (WL) and connecting the precharged bit lines, BL and BLB, to the internal nodes of the cell. Upon read access, the bit line voltage VBL remains at the precharge level. The complementary bit line voltage VBLB is discharged through transistors connected in series. Effectively, transistors NG1 and PG1 form a voltage divider whose output is now no longer at zero volts and is connected to the input of inverter P1 and N1. Sizing of NG1 and PG1 should ensure that inverter P1 and N1 do not switch causing a destructive read.

The static memory SRAM with 4 transistor topology has been designed using the CADENCE Virtuoso tool. The figure shows the schematic of the 4T SRAM. The layout of the circuit is shown in the Fig.4 From the layout we can see the area is reduced than that of the 6T SRAM.

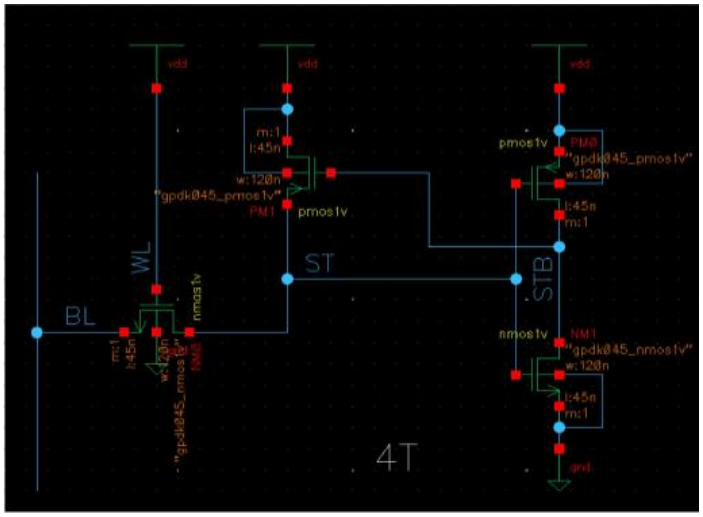

Fig -4 Schematic of Proposed 4T SRAM

4. TRANSIENT RESPONSE OF 6T & 4T SRAM BIT CELLS

By doing the transient analysis of SRAM cell we generate the transient response of 6T & 4T SRAM. Fig 5 & Fig 6 shows the transient responses of 6T & 4T respectively.From the transient response the average power in the SRAM cell can be calculated using "psf" function and the virtuoso calculator.

The average power obtained for the 6T SRAM cell is 9.468*10^-9W. Power obtained in the reference paper is 5.361*10^-9W .The average power is calculated using virtuoso calculator. The average power is 5.556*10^-15W . The average power of 4T SRAM is approximately 40% lower than that of the 6T SRAM.

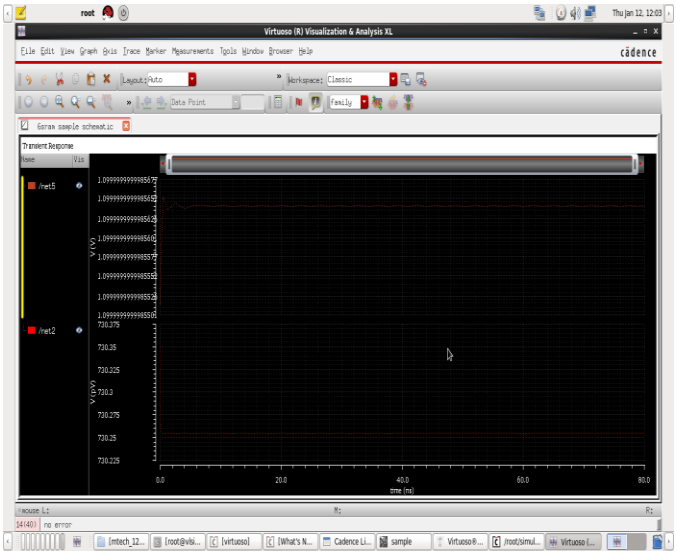

Fig-5 Transient response of 6T SRAM

Fig-6 Transient response of 4T SRAM

5. LAYOUT OF 6T & 4T SRAM BIT CELLS

Another design criterion was reducing the area, to analyze area of SRAM bit cell we need to generate the layout of the circuits. The layout of 6T SRAM is generated and analysed using virtuoso. The DRC check and LVS analysis is carried out. Layout is shown in fig.7

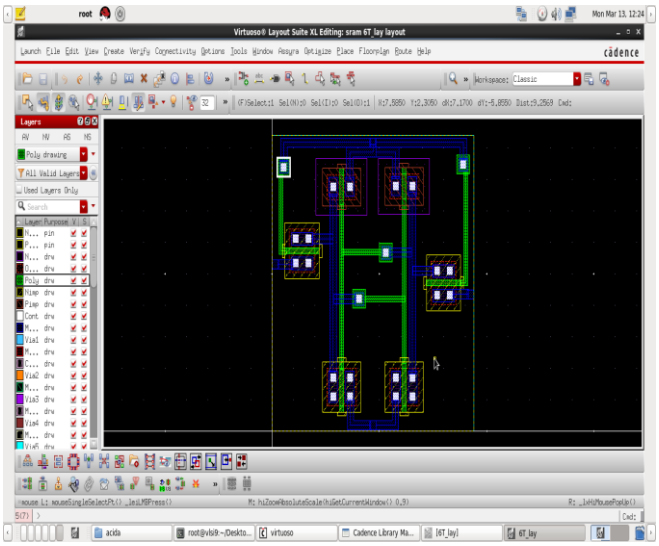

Fig -7 layout of 6T SRAM

The layout of the circuit is shown in the fig.8. From the layout we can see the area is reduced than that of the 6T SRAM.

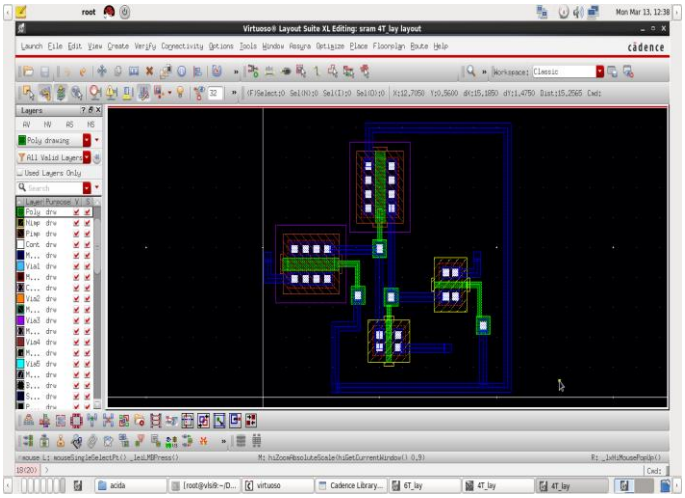

Table -1: Result analysis of different SRAM configurations

SL.NO.	SRAM Topology	Power	Area
1	6T SRAM	9.468*10^-9W	54.21μm^2
2	4T SRAM	5.556*10^-15W	19.22μm^2

6. CONCLUSIONS

In this project an existing conventional 6T SRAM is implemented using 180nm CMOS technology with supply voltage 1.1V and threshold voltage 0.18V. A new 4T SRAM circuit is designed which reduces the power consumption as well as area of the memory cell. Both conventional and proposed circuits are implemented and their area and power is calculated. It is found that the power is reduced approximately 40% in 4T SRAM than that of 6T SRAM.

The area of bit cell is calculated by generating the layout of both 6T SRAM and 4T SRAM. The layouts of existing 6T SRAM in 180nm technology and the proposed 4T SRAM is implemented in Cadence. The new cell size is 35.45% smaller than a conventional six-transistor cell using same design rules.

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