Switched DC Sources Based Novel Multilevel Inverter

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Abstract – *This paper we are represent the five-level inverter, it reduces the no. of switches and gives the large no. of output levels. It comprises two input dc sources connected in opposite polarities with one another through power switches. Each input dc level presents in the stepped load voltage either separately or in additive combinations with other input levels.*

This approach results in reduced number of power switches as compared to existing topologies. The operating principle of the proposed topology is demonstrated with the help of a single –phase five-level inverter. An exhaustive comparison of the proposed topology is made against the existing cascaded H-bridge topology.

Key Words: *Existing topologies, five-level inverter, reduced component count, pulse width modulation (PWM), total harmonic distortion (THD).*

1. INTRODUCTION

In the last few decades, five-level voltage-source inverters have come forth as a viable solution for high-power dc-to-ac conversion applications [1]. A five-level inverter is a linkage structure of multiple input dc levels (obtained from dc sources and/or capacitors) and power semiconductor devices to synthesize a staircase waveform. Voltage stresses practiced by the power switches are lower as compared to the overall operating voltage level [2]. In addition, the multilevel waveform has improved harmonic profile as compared to a two-level waveform obtained from ordinary inverters. Other benefits of MLIs are reduced *dv/dt* stress on the load and possibility of fault-tolerant operation [3]. Researchers are also exploring approaches to employ MLIs for low-power applications [4]. The nature of the multilevel waveform is enhanced by increasing the number of levels. However, in existing topology used large number of power switches and complex gate drive circuit. This increases complexity of system and cost and reduces the reliability and efficiency of system. For a efficient system requires reduce the number of switches and gate drive circuit [5].

However, there is a expressive increase in the number of power switches, the number of switches conducting concomitantly, and the overall cost of the system with the increase in the number of output levels. Researchers, therefore, proceed to focus on reducing the component count in multilevel topologies through several approaches. In this paper, a new topology is proposed in which alternate dc sources are linked in adverse polarities via power switches. This approach significantly lessens the number of power switches needed as compared to the existing topologies. Furthermore, for regular input dc sources, the proposed topology presents similarity with the CHB topology in two forms: 1) it's necessities multiple isolated input dc voltages; and 2) input dc voltage levels can be concrete into complete additional values. Thus, the topology can be used as a utility interface for renewable energy systems where a more number of isolated dc sources are available [2], [7], [9]. It can be used in medium-voltage drive applications where a phase-shifting transformer with multiple secondary windings is generally applied (primarily for the reduction of line current distortion), thus providing isolated dc sources [6]. The applications of the proposed topology for battery-powered (such as electric vehicles and submarine propulsion). This paper is arranged as follows. Section 2 introduces the generalized structure of the proposed topology with mathematical formulations. The operating principle of the topology is also defined in this section with the help of a five-level single phase inverter. Terms for the calculation of losses are present in Section 3. A comparison of the proposed topology with existing topologies is presented in Section 4. In Section 5 conclusions are summarized.

2. PROPOSED MULTILEVEL TOPOLOGY

In that section, we are introduced the structure of proposed topology, and its operating principle is illustrated with the help of a single-phase five-level inverter. Terms' for output voltage, source currents, voltage stresses, etc., are also introduced.

2.1 Generalized Structure

Fig.1 shows that a generalized single phase structure of five-level inverter. its having a n number of DC sources . linkage structure of sources as like a positive terminal of one DC source connected to negative terminal of another DC source , in this way we are linkage the n number of DC source .in fig. 1 shows input sources as like E_j (where j=1 to n) . Source current indicated of each source as like i_j(t) . We are uses power switches in that as like MOSFET, IGBT.AND ANTIPARALLEL DIODES are used across with power switches. In fig.1 we shows IGBT switches with an anti-parallel diodes and complementary pairs are designated as like as (T_j ,T_j') (where, j=1 to n+1). In fig. 1 indicated nodal voltage and current are V_L (t) and i_L (t) respectively.
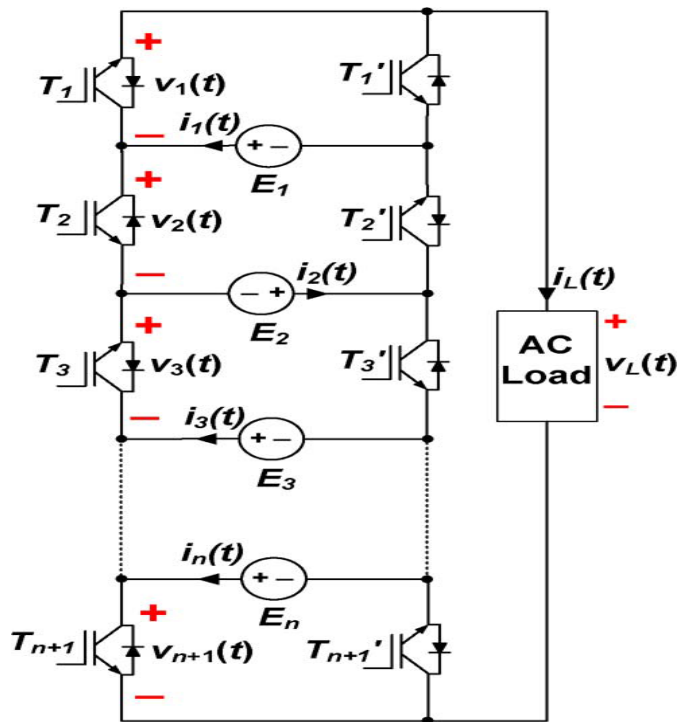
Fig -1: Generalized single-phase construction of the proposed topology.

2.2 Working Principle

The working principle of the proposed topology is defined with the help of a single-phase inverter with two input dc sources $E1$ and $E2$, as shown in Fig. 2. It has three couples of active switches (Tj, Tj') (j = 1, 2, 3). Since the elements of these couples are counterparty and it's having eight valid operating modes. These modes are shown in Fig. 3 and are briefed in Table 1 along with nodal voltages and source currents. Using these operating modes shown in Fig. 3, the load is supplied with five levels, viz., $\pm V$dc, $\pm 2V$dc, and zero for $E_1 = E_2 = V$dc. With such a regular source configuration, modes 3 and 4 become excessive for output level $+V$dc, while modes 6 and 7 become redundant for output level $-V$dc. It is main to note here that, for whole positive voltage levels and one "zero" level (modes 1, 3, 4, and 5), switch T_2' always conducts, while for whole negative voltage levels and another "zero" level (modes 2, 6, 7, and 8), switch $T2$ always conducts. Accordingly, it is possible to operate these two switches at the fundamental frequency to acquire five output levels. To do so, modes 1, 3 (or 4), and 5 need to be applied for the synthesis of positive levels (including a "zero" level), and modes 2, 6 (or 7), and 8 need to be applied for the synthesis of negative voltage levels (contains a "zero" level). It is also important to declare here that dc source voltages have been assumed to be equal in this work. In usage, they might differ (e.g., due to different states of charge of batteries or due to shading of some cells if the sources are

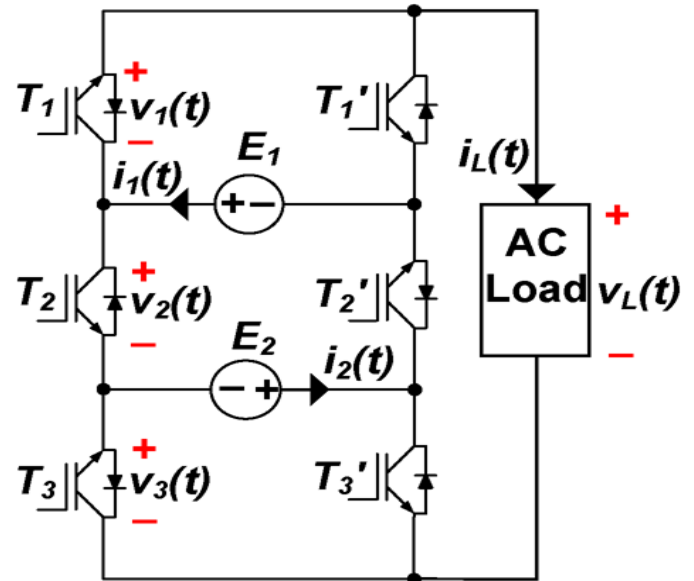becoming from a photovoltaic (PV) system). To account for

Fig -2: Single-phase inverter based on the proposed topology with couple input sources.

this deviation, both hardware-based solutions (e.g., using separate dc–dc converters [8]) and control-algorithm-based solutions (e.g., battery adjusting methodology [19]) can be appliance.

2.3 Mathematical Formulations

According to Fig. 1, switches Tj and Tj' (j = 1 to n + 1) operate correspondingly. Let S_j be a switching function complementarily to switch Tj presented as

$$S_j = \begin{cases} 1, & \text{if } T_j \text{ is on} \\ 0, & \text{if } T_j \text{ is off.} \end{cases} \tag{1}$$

Then, the load terminal voltage $v_l(t)$ can be specified in terms of nodal voltages $v_j(t)$ as

$$v_L(t) = \sum_{j=1}^{n+1} v_j(t) \tag{2}$$

Where

$$v_j(t) = (-1)^j (1 - S_j)(E_j + E_{j-1}) \tag{3}$$

Using j = 1 to j = n + 1 & $E_0 = E_{n+1} = 0$ as there are no such sources.
Using (2) and (3)

$$v_L(t) = \sum_{j=1}^{n+1} \left[(-1)^j (1 - S_j)(E_j + E_{j-1}) \right]. \tag{4}$$
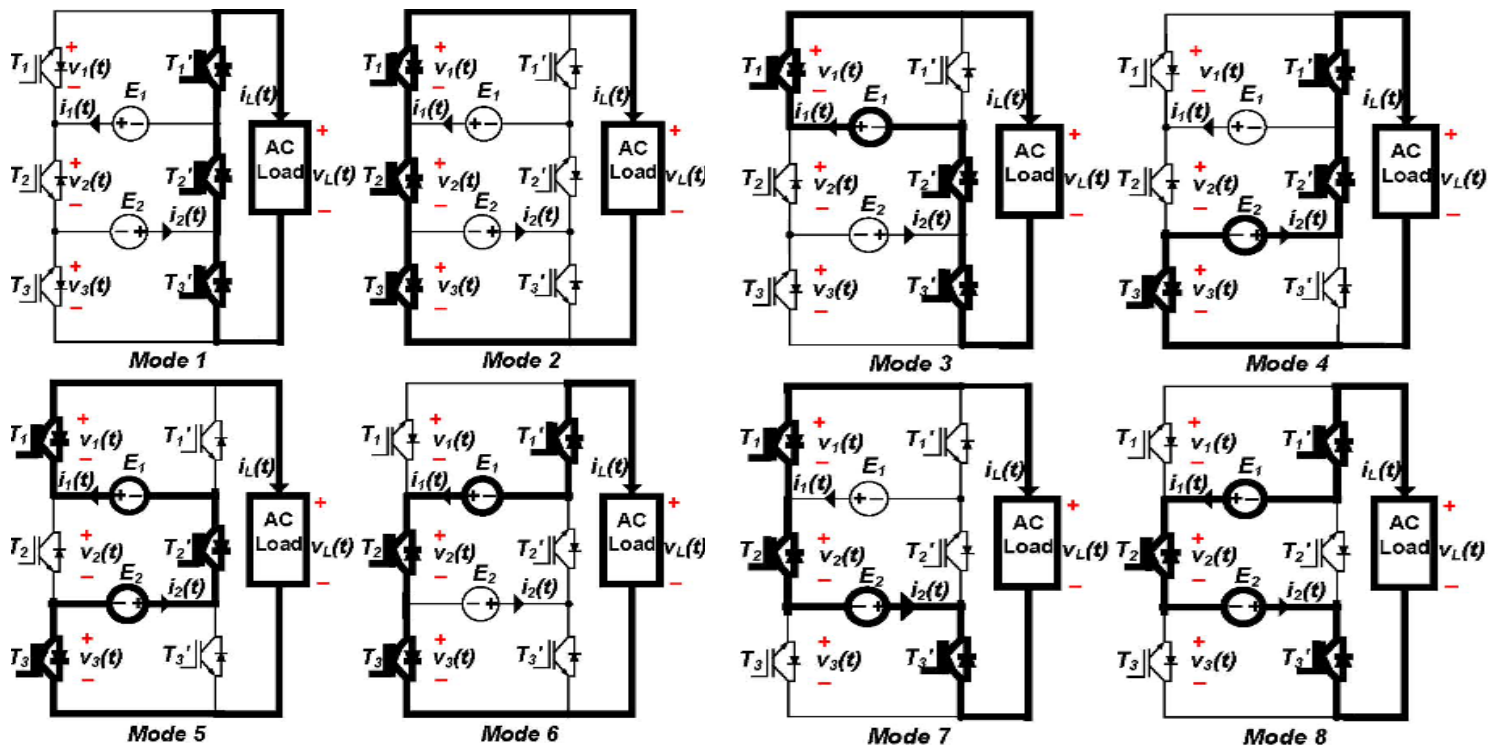
Fig -2: Valid operating modes for the inverter.

Table -1: Operating modes

| Mode | Switch States (1 = ON; 0 = OFF) | | | Nodal Voltages | | | Source Currents | | Output Voltage |
	T_1	T_2	T_3	$v_1(t)$	$v_2(t)$	$v_3(t)$	$i_1(t)$	$i_2(t)$	$v_L(t)$
1	0	0	0	$-E_1$	E_1+E_2	$-E_2$	0	0	0
2	1	1	1	0	0	0	0	0	0
3	1	0	0	0	E_1+E_2	$-E_2$	$i_L(t)$	0	E_1
4	0	0	1	$-E_1$	E_1+E_2	0	0	$i_L(t)$	E_2
5	1	0	1	0	E_1+E_2	0	$i_L(t)$	$i_L(t)$	E_1+E_2
6	0	1	1	$-E_1$	0	0	$-i_L(t)$	0	$-E_1$
7	1	1	0	0	0	$-E_2$	0	$-i_L(t)$	$-E_2$
8	0	1	0	$-E_1$	0	$-E_2$	$-i_L(t)$	$-i_L(t)$	$-(E_1+E_2)$

The output voltage in terms of the values of input dc sources and switching functions is administrated by (4).

Likewise, the source current i_j (t) through a given source E_j $(j = 1$ to $j = n)$ can be specified in terms of switching functions and load current $i_L(t)$ as

$$i_j(t) = (-1)^{j+1}(S_j - S_{j+1})i_L(t). \qquad (5)$$

Voltage stress $V_{stress,j}$ for both switches of the jth switch pair (T_j, T_j') can be specified as

$$V_{\text{stress},j} = E_{j-1} + E_j \qquad (6)$$

Where j = 1 to $(n + 1)$, with n case the number of input dc sources.

For symmetrical input dc sources, i.e., $E1 = E2 = \ldots = Ej = \ldots = En = V$dc, voltage stresses born by switch pairs (T_1, T_1') and $(Tn+1, Tn'+1)$ are equal to Vdc each, much as for all the staying switches, the voltage stress is equivalent to $2V$dc each.

In accession, the number of levels synthesized by the topology is present by

$$N = 2n + 1. \qquad (7)$$

The peak voltage achieved for such a configuration is given by

$$v_{\max} = nV_{\text{dc}}. \qquad (8)$$

3. CALCULATION OF LOSSES

The losses consorted with a power electronic converter can be equated with the amount of power losses incurred by the separate semiconductor devices. Losses incurred by a semiconductor device can be typically presented under three class:

1) When the device is blocking (i.e., OFF state);
2) When the device is conducting (i.e., ON state); and
3) When the device is switching (i.e., the state is changing

from ON to OFF or vice versa).

3.1 Conduction Losses

All switches demanded in the proposed topology are bidirectional conducting and unidirectional blocking, this is shown in Fig. 1, the immediate conduction losses of typical transistor and diode are

$$\rho_{c,T}(t) = [V_T + R_T i^\alpha(t)]\, i(t) \tag{9}$$

$$\rho_{c,D}(t) = [V_D + R_D i(t)]\, i(t) \tag{10}$$

Where $\rho_{c,T}(t)$ and $\rho_{c,D}(t)$ denote the immediate conduction losses of the transistor device and diode, respectively. V_T and V_D are the ON-state voltage fall, mean while R_T and R_D are the equivalent ON-state resistances of the transistor device and diode, respectively, and α is a constant administrated by the transistor characteristics.

The average conduction losses can be specified, using (9) and (10), as

$$\rho_{c,\mathrm{avg}} = \frac{1}{\pi} \int_0^\pi [\{N_T(t)V_T + N_D(t)V_D\}\, i_L(t)$$
$$+ \{N_T(t)R_T i_L^{\alpha+1}(t)\} + \{N_D(t)i_L^2(t)\}]\, d(\omega t). \tag{11}$$

3.2 Switching Losses

To calculate the switching losses of an particularly switch, a linear resembling of voltage and current during a switching period (transition from ON to OFF state or vice versa) is used.

Energy losses can be calculated as during transistor turn ON

$$E_{\mathrm{on},j} = \int_0^{t_{\mathrm{on}}} v(t)i(t)\, dt$$
$$= \int_0^{t_{\mathrm{on}}} \left[\left\{V_{o,j} \frac{t}{t_{\mathrm{on}}}\right\} \left\{-\frac{I}{t_{\mathrm{on}}}(t - t_{\mathrm{on}})\right\} \right] dt$$
$$= \frac{1}{6} V_{o,j} I t_{\mathrm{on}} \tag{12}$$

Where
$E_{\mathrm{on},j}$ turn-on loss of the jth transistor;
T_{on} turn-on time;
I current through the transistor after turning on;
$V_{o,j}$ voltage that the jth transistor needs to block.
Similarly, energy losses of the jth transistor during turning off can be calculated as

$$E_{\mathrm{off},j} = \int_0^{t_{\mathrm{off}}} v(t)i(t)\, dt$$
$$= \int_0^{t_{\mathrm{off}}} \left[\left\{V_{o,j} \frac{t}{t_{\mathrm{off}}}\right\} \left\{-\frac{I'}{t_{\mathrm{off}}}(t - t_{\mathrm{off}})\right\} \right] dt$$
$$= \frac{1}{6} V_{o,j} I t_{\mathrm{off}} \tag{13}$$

Where t_{off} means the turn-off time for the jth transistor and I' is the current through the transistor before turning off. The total switching power losses can be adapted as

$$\rho_s = \sum_{j=1}^{2n+2} \left[\frac{1}{6} V_{o,j} I (t_{\mathrm{on}} + t_{\mathrm{off}}) f_j \right] . \tag{14}$$

The total inverter losses can now be acquired using (11) and
(14) as

$$\rho_{\mathrm{losses}} = \rho_{c,\mathrm{avg}} + \rho_s. \tag{15}$$

4. COMPARISON WITH OTHER TOPOLOGIES

In this section, compared the proposed topology with other topologies. In Section 4-4.1, the topology is compared with existing topologies in terms of component requirements. In Section 4-4.2, an exclude and exhaustive comparison is carried out with the CHB topology because, as present earlier, the proposed topology resembles the CHB in conformation and functional features.

4.1 Overall Comparison with Existing Topologies

The proposed topology requires significantly lesser number of power switches as compared to existing topologies. Likewise, the total voltage stress born by main switches and diodes in the proposed topology is equal to those of existing topologies.

4.2 Comparative Analysis of the Proposed Topology with the CHB Topology

Power Switch demands: With "n" number of dc sources, the CHB topology demands "$4n$" switches, while the proposed topology demands "$2n + 2$" switches.

Switching Losses: With adapted switching control, the proposed topology can be appliance with lesser switching losses as compared to the CHB topology.

Table -2: Comparison between Existing Topology with Proposed Topology

Inverter type /Component	NPC	Flying capacitor	Cascaded H-Bridge	Proposed Topology
Number of main switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3(N+1)$
Number of main diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3(N+1)$
Number of clamping diodes	$3(N-1)(N-2)$	0	0	0
Number of DC bus capacitors/ Isolated supplies	$(N-1)$	$(N-1)$	$3(N-1)/2$	$3(N-1)/2$
Number of flying capacitors	0	$(3/2)(N-1)(N-2)$	0	0
Total component count	$(N-1)(3N+7)$	$(1/2)(N-1)(3N+20)$	$27/2(N-1)$	$(15N+9)/2$
Total voltage stress born by main switches	$6(N-1)V_{DC}$	$6(N-1)V_{DC}$	$6(N-1)V_{DC}$	$6(N-1)V_{DC}$
Total voltage stress born by main diodes	$6(N-1)V_{DC}$	$6(N-1)V_{DC}$	$6(N-1)V_{DC}$	$6(N-1)V_{DC}$
Total voltage stress born by DC bus capacitors / Isolated supplies	$3(N-1)V_{DC}$	$3(N-1)V_{DC}$	$3(N-1)V_{DC}/2$	$3(N-1)V_{DC}/2$

5. CONCLUSION

A Five-Level inverter are gaining attention, exertion are being directed toward attenuating the device count for increased number of output levels. A novel topology for Five-Level inverter has been proposed in this paper to attenuate the device count. The operating principle of the proposed topology has been illustrated and mathematical formulations suiting to output voltage, source currents, voltage stresses on switches, and power losses have been eliminate. Comparisons of the proposed topology with existing topologies acknowledge that the proposed topology significantly reduces the number of power switches and associated gate driver circuits.

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