International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 04 Issue: 06 | June -2017 www.irjet.net p-ISSN: 2395-0072

Review on Transmission and Reception of Data Through USB in VHDL

Mangesh M. Sahare[1], Prof.Vinay Keswani[2]

[1]M.Tech. IInd year, Dept.ofElectronic & Communication, Vidharbha Institute of Technology, Umrer,Maharashtra,India
[2]Assistant Professor,Dept.ofElectronic & Communication, Vidharbha Institute of Technology, Umrer,Maharashtra,India

---

Abstract - *The scope of project is based on USB controller which depends upon the Video and Audio Host controller. High speed data which flow between Video and Audio devices improves the speed quality in Telephone Integration, Consumer Electronics and in productivity applications. USB is designed to standardized connection of computer application. It is useful insecure storage of data, personal data transportation. Universal Serial Bus is an industry standard that defines cable connectors and communication protocols for connection, communication and power supply between computer and electronic devices. USB Receiver/Transmitter architecture is used to innovate this approach. The various concepts were implemented in hardware description language to provide model for simulations. Simultaneously the code is synthesizable, and may be physically implemented in programmable logic devices.*

***Keywords*: USB, ComputerTelephony Integration, transmitter, Receiver.**

1. INTRODUCTION

All communications on USB originates at the host under software control. The host hardware consists the USB host controller, which initiates the transactions over the USB system, and the root hub, which provides attachment points for USB device. The host controller is responsible for generating the transactions that have been scheduled by the host software. The host controller driver builds a linked list of data structures in memory that defines the transactions that are scheduled to be performed during a given frame. These data structures, called transfer descriptors, contain all of the information the host controller needs to generate the transactions. The USB standard was developed to overcome the shortcomings of older interfaces to peripheral devices for PCs. The standard makes interfacing to the PC extremely easy for the end user and life more complicated for the peripheral designer. The USB 2.0 Transceiver Macro cell understands the USB protocol and is capable of carrying out transactions on behalf of the device. Verilog is a hardware description language widely used in the VLSI industry.

2. EXISTING WORK

For testing our project we will be using a memory for storing descriptors to be transferred, which are actually provided by the USB device driver. These descriptors are fed to the packet generation unit and then to SIE, which appends SYNC, EOP, CRC bits to it, performs bit stuffing and then finally encodes it in NRZI format before transmitting it to USB.In testing we will be demonstrating the Control transfer and the isochronous transfer. Control transfer because it is necessary for the configuration of a new device and isochronous because full speed devices support it and it will be more appropriate to test the device for critical high-speed operation than for a low speed operation.

3. PROPOSED WORK

Input module: This module convert the serial input from the host .Remember, all data must be packaged into packet that suitable for USB protocol. Its implementation uses 8-bit shift register.

Setup/in packet: This module determines whether the incoming packet is setup packet or in packet .This information can be known by detecting the type and check bits of the packet. Clearly, we may use two comparator to handle each packet.

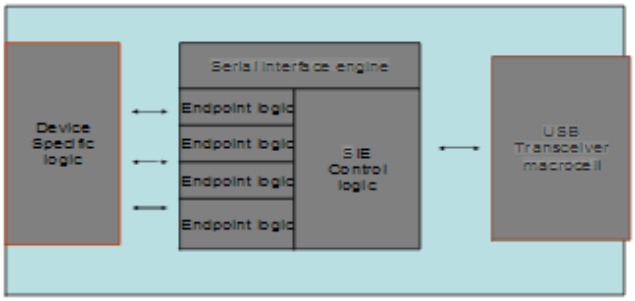
CRC circuit: The USB specification lists two generator polynomials, one for token and the other for data packet. The generator polynomial for tokens is x 5+x2+x0 while the generator polynomial for data packets is x16+x15+x2+x0. Since the remainder is always of smaller degree than the generator polynomial, the token CRC is a bit pattern and the CRC is a 16 bit pattern. Its implementations use XOR gates and D-flip-flops.
Register and address comparator: When the incoming packet is a setup, then we have to send 0000000 as an input to the 7bit comparator. If a match signal is detected, then address register will save the address. To realize this circuit, we need latch and comparator.
ACK generator circuit: When a setup packet is received, one expects to receive an 8byte data packet, and then we have to respond with an ACK. The 8byte data packet contains the newly assigned address.

Data in packet generator: When the in packet from host was received properly, the controller has to respond it by sending the data requested by host. As mention above, this data must be packaged into packet and then send to host serially. We using an 8 bit register and multiplexer to realize this circuit.

4. PROPOSED METHOLOGY

ASIC Technology is used for designing high volume USB 2.0 device with the help of embedded USB 2.0 support. Operating frequency is low enough to allow data recovery for full speed USB devices. It can be handle ledin vendors VHDL, code with the ASIC vendor. ASIC vendor providing only simple level translator for meeting the USB signaling requirements. Comfortably gate arrays are operates now days. Gate arrays operates between 30 and 60 MHz Existing design methodology must change with USB 2.0 signaling running at hundreds of MHz Without modification it is difficult to compile VHDL code for operating frequencies go up. USB 2.0 peripheral development is formal for the intent of the UTMI. ASIC and peripheral development is used for document defines and interface.

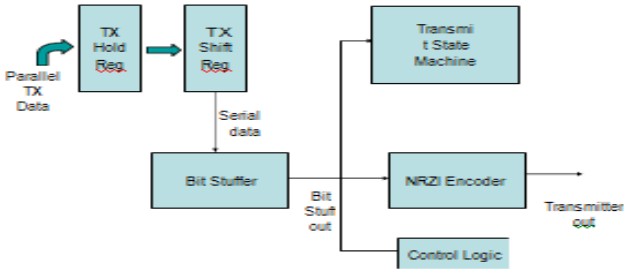
Figure 4.1: USB 2.0 Transceiver



Transmitter

Several tasks are performed by the transmitter. Parallel to Serial data conversion is due to the transmitter. Forming data's one of the function of transmitter, It handshakes the packets before sending them to the host. Another function of transmitter is to calculate the 16 bit CRC included in data packets sent to the host High level functionality that is required to exist in macro cell.

Figure 4.2: Transmitter



Receiver

Function of receiver is the opposite to the function of the transmitter. Function of transmitter is more complicated than transmitter; 5 bit CRC and 16 bit CRC are both the capability of receiver. Token packets contain 5 bit CRC and Data Packets contain 16 bit CRC, Hence both 5 bit CRC and 16 bit CRC are necessary. The value it calculated with the received from the packet are compared by the transmitter. Retransmission is requested if there is inconsistency.

USB 2.0 Transceiver Macrocell

USB 2.0 (Universal Serial Bus) The host controller will support one of the multiple modes of data transfer that is isochronous data transfer .The isochronous transfers send and receive data in real time with guaranteed bus band width but without any reliability. In general these transfer types are used in audio and video devices.

The USB host Controller will properly support the configuration process whereby the device is assigned an address. It then monitors the bus for packets addressed to itself and handles the transfer of data to host machine. Data must be packaged into packets and transmitted to the host. Meanwhile incoming packets must be verified for validity through the use of 5 and 16-bit CRCs and 1's complement check bits. The controller will be able to handle two types of transactions, meaning it must respond to two packets. The 1st packet is a SETUP packet. When a SETUP packet is received one expected to receive an 8 byte data packet and the chip have to respond with an acknowledge signal(ACK). The 8 byte data packet contains the newly assigned address. We called it configuration process. The second packet is an IN packet. When an IN packet is received from the host, the controller checks to see if the address matches the chip's assigned address. If a match is detected, we send a data packet. We called it application process. The design process of this chip uses finite state machine (FSM) method based on top-down modular design approach. Its VHDL code is described either at behavioral or structural level. Then we simulated and verified each module we

have designed. The final step is to Synthesized its logic circuit and implemented its hardware.

5. CONCLUSIONS

Reviewed USB Trans receiver microcell is useful in Linux and android operating system hardware architecture of high speed data communication for USB 2.0 device reviewed. It is tested that demonstrating the Control transfer and the isochronous transfer. Control transfer because it is necessary for the configuration of a new device and isochronous because full speed devices support it and it will be more appropriate to test the device for critical high-speed operation than for a low speed operation.

6. REFERENCES

[1]Babulu K. and Rajan K. (2008, July). FPGA Implementation of USB Transceiver macro cell Interface with USB2 0 Specifications. In Emerging Trends in Engineering and Technology, 2008. ICETET'08. First International Conference on (pp. 966-970). IEEE.

[2]Jolfaei F., Mohammadizadeh N., Sadri M., and FaniSani, F. (2009, December). High speed USB 2.0 interface for FPGA based embedded systems. In Embedded and Multimedia Computing, 2009. EM- Com 2009. 4th International Conference on (pp. 1-6). IEEE.

[3]Guo G., Li Z., and Yang F. (2011, July). Design of high speed pulse data acquisition system based on FPGA and USB. In Multimedia Technology (ICMT), 2011 International Conference on (pp. 5374-5376). IEEE.

[4] Lun C., bin Marzuki A. and Wei S. (2012, June). Analog front-end design implementation of USB 2.0 OTG Attach Detection Protocol. In Intelligent and Advanced Systems (ICIAS), 2012 4th International Conference on (Vol. 2, pp. 774-779). IEEE.

[5]Szecowka P. and Pyrzynski K. (2012, September), USB receiver/transmitter for FPGA implementation. In signals and Electronic system (ICSES), 2012 International Conference on (pp.1-6). IEEE.