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Design of Voltage Reference Using Process Invariant Current Reference

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Abstract - *The objective of the work is to make a voltage reference which is process invariant circuit using cadence virtuoso tool. An efficient voltage reference circuit is a key building block to many analog and analog mixed signal circuits. For that a PTAT and CTAT (Complementary to Absolute temperature) current reference is needed which together will provide a constant current supply. But here utilizes MOSFET zero temperature coefficient point for building the reference. A PTAT current reference circuit is simulated in 180nm technology using an on chip resistor which tracks the process variation. The obtained voltage reference is having a temperature coefficient of 36* $ppm/^{o}C$.

Key Words: PTAT, CTAT, Voltage reference, ZTC (Zero Temperature coefficient), Transconductance

1.INTRODUCTION

Most of the circuits use a reference, be it voltage, current or time. A reference in a circuit establishes a stable point used by other sub-circuits to generated predictable and repeatable results. This reference point should not change significantly under various operating conditions. Temperature is an important parameter which affects the performance of references. Special attention should therefore be paid to the temperature behavior of the reference. The typical metric used for variations of the reference voltage across temperature is the temperature coefficient (TC) and it is normally expressed in parts-per-million per degree Celsius.

A voltage reference having high temperature independency is a good requirement for analog circuits.. Through this work a voltage reference circuit is proposed by utilizing zero temperature coefficient point of MOSFET. Voltage reference is usually made by using a PTAT and CTAT references. Here the circuit utilizes a PTAT current only. Beyond that the sensors utilizes the property of the PTAT circuit.

PTAT current can be obtained by using on chip and off chip resistors. On chip resistors require large area to fabricate. Also on chip MOS resistors will be dependent on technology parameters like mobility threshold voltage etc. To avoid process and temperature variations a process independent grounded resistor is used in [2]. The constant on-chip resistor is used to generate constant transconductance bias circuits [3] [4] [5].

2. PMOS IN TRIODE REGION

A PMOS transistor in triode region will act as a good resistor. The resistance of the transistor is given by.

$$R = \frac{1}{\mu_p . C_{ox} \left(W/L\right)\left(V_{sg} - |V_{thp}|\right)}$$

where *μp* is the hole mobility, *Vthp* is the threshold voltage, and *Cox* is the oxide capacitance of the PMOS transistor.
On rewriting the equation

$$V_{sg} = |V_{thp}| + \frac{1}{R.\mu_p . C_{ox}\left(\frac{W}{L}\right)}$$

The effect of temperature variation of mobility on the required gate voltage is larger than that of threshold voltage. Therefore a gate voltage with a complementary to absolute temperature (CTAT) behavior is required.

2.1 CTAT Voltage Generator

To compensate the effect of tempereature effect of PMOS transistor in triode region a CTAT voltage generator is used. [7] [8].

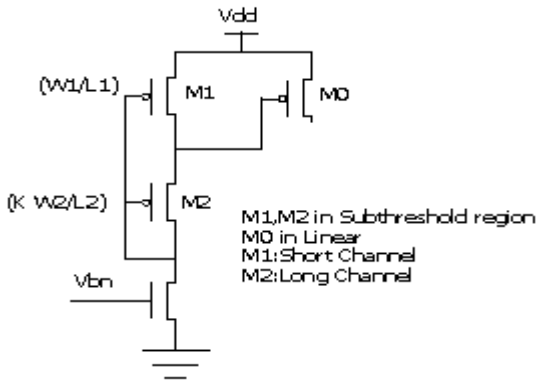

Fig -1: Process Tracking CTAT Voltage Generator

Transistors *M*1 and *M*2 are biased in the subthreshold region. Transistor *M*1 is of short channel length, and transistor *M*2 is of long channel length. The short channel transistor is susceptible to more process variations than the long channel transistor [1] [6].

The output voltage *Vd*1 is used to bias the gate of transistor *M*0. Therefore, *Vd*1 should be well below *VDD*. This requirement imposes an unreasonable large value for parameter *K* . A solution for this problem is provided by using the stack of CTAT voltage generators. The stack provides flexibility in choosing the desired aspect ratios according to the required bias voltage.

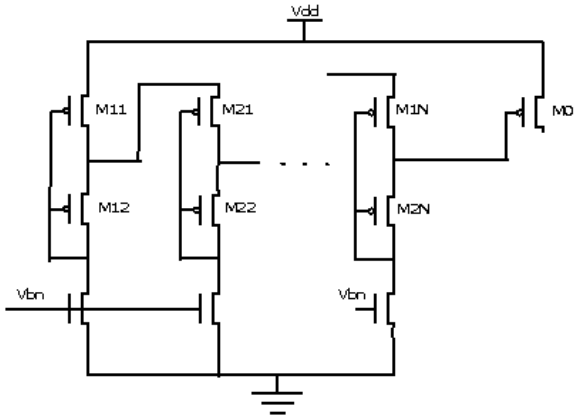

Fig- 2: Stack of CTAT Voltage Generators

3. PTAT CURRENT GENERATOR

Fig 3 shows the PTAT current reference generator using PVT invariant resistor.

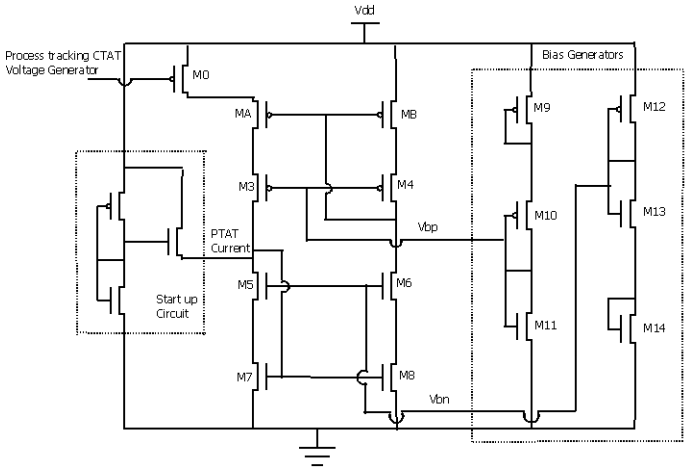

Fig -3: PTAT Current Generation using PMOS Resistor.

4. ZERO TEMPERATURE COEFFICIENT

The drain current of an NMOS transistor in the saturation region is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs}-V_{th}\right)^2$$

In the above equation threshold voltage and mobility are the main temperature dependent parameters. As the temperature increases, both the threshold voltage and the mobility decrease. But the decrease of VTH and the decrease of mobility have opposing effects on the drain current; a lower threshold voltage tends to increase the drain current, but a lower mobility tends to decrease it. At some value of VGS, this mutual compensation of mobility and threshold voltage results in a zero temperature coefficient, (ZTC), at a particular bias point of a MOS transistor [9] [10].

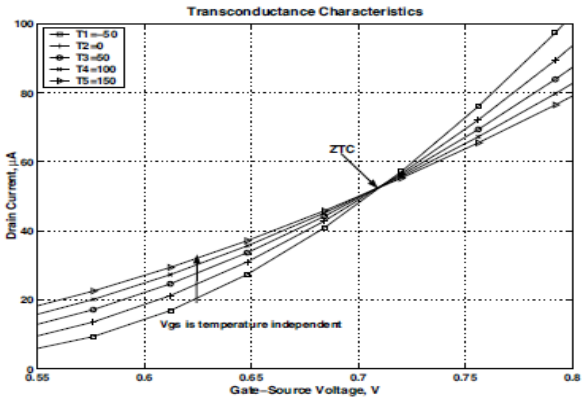

Fig-4: Transconductance characteristics of a NMOS transistor

The fig 4 also shows that when the transistor is biased with a constant current I_D, above the ZTC point vicinity, the gate-source voltage has a positive temperature dependency and when it is biased with a temperature-stable constant current below the ZTC point vicinity, the gate-source voltage has a negative temperature dependency.

5. PROPOSED VOLTAGE REFERENCE

Using a proportional to absolute temperature (PTAT) bias current, which is much easier to realize than a temperature independent current source, it is possible to obtain a temperature independent gate-source voltage when the transistor is biased below its ZTC point

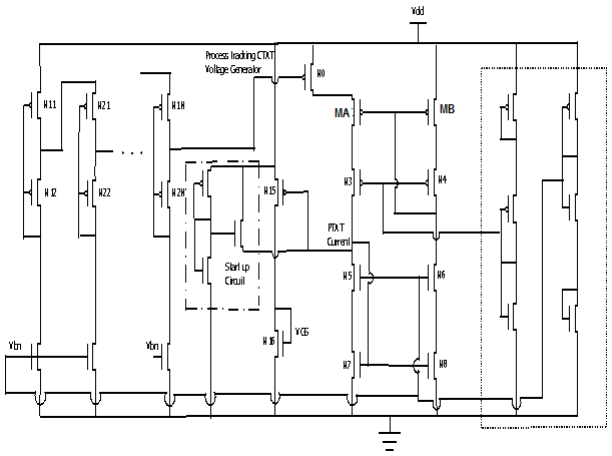

Fig-5: Voltage reference using PTAT current reference

Table 1 gives the size of the transistors

Table 1-: Transistor sizes for the circuit in fig 5

Transistor	Width(μm)	Length(μm)
M11,M12,...M1N	2.4	0.18
M21,M22,...M2N	28	0.21
M0	0.4	20
MA	4	0.5
MB	20	0.5

6. RESULTS

The circuit is simulated using cadence virtuoso tool in 180nm technology.

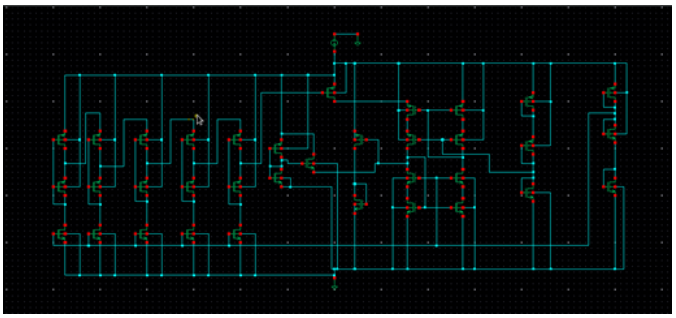

Fig-: 6. Shematic of Voltage Reference

Fig 6 shows schematic of the circuit which is derived from PTAT current reference.

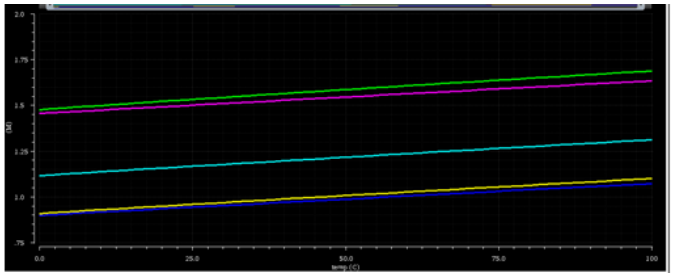

Fig-: 7 Simulation Result for Constant Resistance

PMOS transistor is used for the process tracking. Resistance is plotted for various process corners such as slow-slow(SS), slow-fast(SF), fast-slow(FS), fast-fast(FF) and typical-typical(TT). The resistance is in the range of mega ohms.

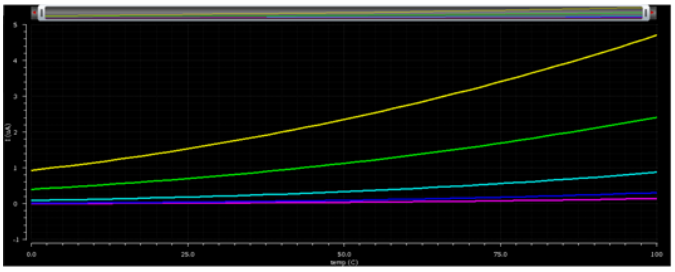

Fig-: 8 Process invariant PTAT current

PTAT current is plotted for various process corners. Using this current a PMOS transistor is driven which is connected to the diode connected NMOS transistor. Gate source voltage of the diode connected NMOS is obtained as voltage reference.

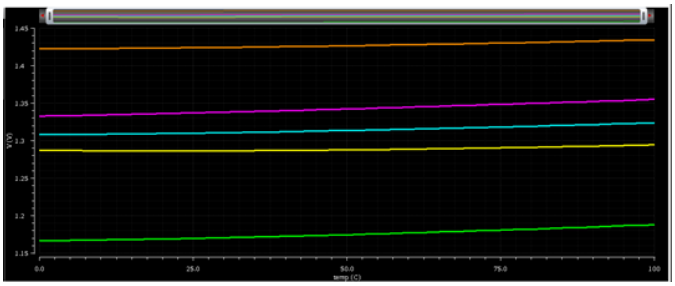

Fig-: 9 Reference voltage for various process corners.

The typical metric used for variations of the reference voltage across temperature is the temperature coefficient (TC) and it is normally expressed in parts-per-million per degree Celsius

$$TC_{ref} = \frac{1}{\text{Reference}} \frac{\partial \text{Reference}}{\partial \text{Temperature}}$$

The proposed voltage reference is having a temperature coefficient of 36 ppm$/^{\circ}C$ over a temperature range of 0 to$100^{0}C$.

6. CONCLUSION

This work is mainly focused on designing a voltage reference using process invariant PTAT current reference circuit. Schematic of classical models of proportional to absolute temperature current and complementary to absolute temperature currents are drawn. From literature survey gives the idea of constructing a simple voltage reference circuit using a PTAT current reference. And also gives the advanced property of process independency. Reference voltage has a temperature coefficient of 36 ppm$/^{\circ}C$. The circuit is simulated using cadence virtuoso tool in 180nm technology.

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