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# Design and Simulation of Power efficient All Digital Phase Locked Loops (ADPLL)

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***Abstract -*** *We presents a new generalised power efficient ADPLL design & Simulation using Verilog . Xilinx ISE 10.1 Simulator is used for simulating Verilog Code and is synthesized using Cadence RTL compiler using gpdk 45 nm technology. To validate its functionality, verification and simulation is done by using the Cadence IES (Incisive Enterprise Simulator) tool. This paper gives the details of basic building blocks of the absolute ADPLL design. And the planned power optimized clock gating technique that is implemented in the Digital loop filter without altering the performance of overall system. The power consumption of this ADPLL is 0.704 µW at a center frequency (fc) of 625 KHz. The total chip area is 207 µm$^2$.*

***Key*** **Words: ADPLL; Digital Loop Filter (DLF); clock gating technique; Power efficient; verilog**

## 1. INTRODUCTION

A Phase Locked Loop is a closed-loop control system that is used for the purpose of synchronization of the phase and frequency with that of an incoming signal. Analog PLLs are in wide use in Television, Radio, Pager, Telephony, Servo Motor control and several other areas. In modern communication systems, Advances in Telecommunication, Wireless & Wire line, and Intelligent Network concepts is posing greater demand towards design of PLLs. Faster and efficient operation of PLLs is very much desired.Phase Locked Loops have become ubiquitous because of its versatility. A phase locked loop (PLL) is a feedback system that synchronizes an oscillator to the frequency and phase of an incoming input signal. It is widely used in frequency modulation and demodulation, clock recovery and frequency control of communication equipment [1]. Traditionally, the PLLs are designed by using the analog approaches. But these PLLs suffer from higher switching and lock in time [2]. Also, the complexity of the circuit increased. In addition to this, the analog PLLs are sensitive to process parameter and for each new technology, it should be redesigned [3]. In contrast to analog based PLLs, ADPLL can be overcome all these problems. ADPLLs have become lucrative due to its scalability, faster lock in time and easy redesign with process changes [4].

In the era of System on Chip (SoC), the primary emphasis has been given to minimizing the power consumption while maximizing speed and functionality. The ADPLL proposed in [5] is based on Time to Digital Converter (TDC). In this design, the resolution has been improved, but it has more power consumption due to the use of additional circuits. Retimed reference clocks based Time to Digital clock scheme has been introduced in [6] to reduce the TDC power; still the overall implementation consumes significant power which is 9.6mW. In [7], low power ADPLL is proposed by using phase prediction technique which involves additional blocks results in more power consumption. ADPLL implementation proposed in [8] uses a digitally controlled oscillator with the delta-sigma modulator for achieving high-frequency resolution. Due to the use of delta-sigma modulator, the power consumption is more.

In the proposed ADPLL, the dynamic power, as well as the total power has been reduced by replacing the digital loop filter with the power optimized digital loop filter. The optimized digital loop filter consumes the lesser power than the conventional one. The Power consumption is reduced with the help of clock gating technique [9].

## 2. ADPLL ARCHITECTURE

The ADPLL block diagram is shown in Fig 1. It consists of three parts: Digital Phase Detector, Digital

Loop Filter and Digitally Controlled Oscillator (DCO). All these three parts are connected to form a closed-loop frequency feedback system.

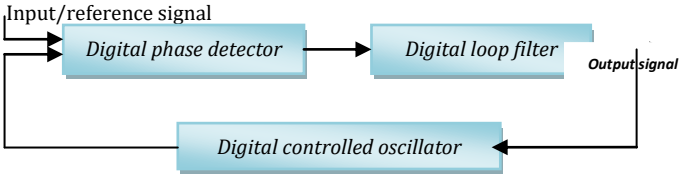



Fig.1. Block diagram of ADPLL

For improvements and advancement of digital very-large- scale integration circuits (VLSI's), all-digital phase-locked loops (ADPLL's) have good abilities to fulfill the requirements of communication applications. In ADPLL, all components used are digital in nature. The use of digitized components in ADPLL provides immunity from factors like parasitic capacitance, noise, temperature dependency which were bottleneck of the analog based PLLs.

The circuit of ADPLL is shown in Fig. 2 [10] [11].in the schematic of Fig. 2, the Ex-OR gate is used as digital phase detector, K counter as digital loop filter and the DCO is formed by the combination of ID counter and ÷N counter

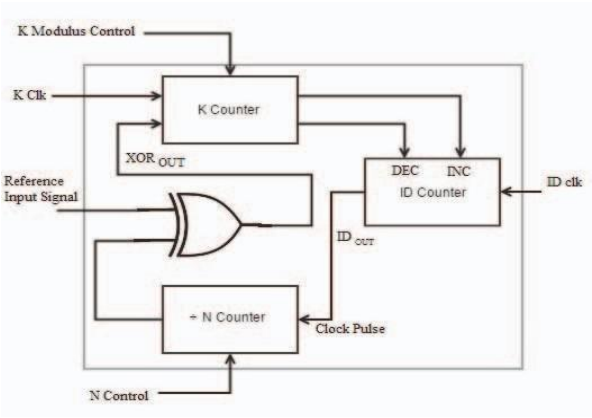



Fig.2. All Digital PLL circuit diagram

In following section, the corresponding circuits of the ADPLL subsystems depicted in Fig. 2 are described.

*A. Digital Phase Detector*

In this ADPLL design, the phase detector is implemented by EXOR gate. The EXOR mechanism offers a simple yet reliable method of phase detection.It compares the phase of the incoming input signal with the phase of the signal produced at the output of the ADPLL and produces an error signal that is proportional to the phase difference.

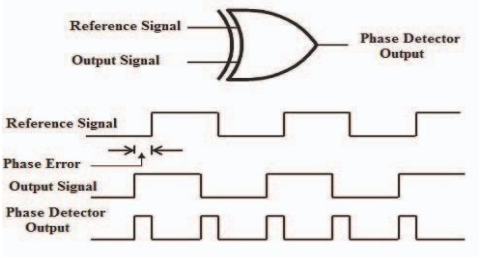
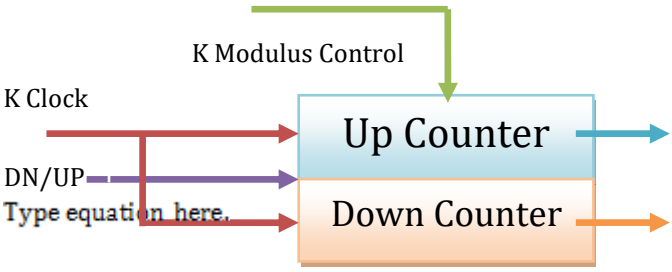


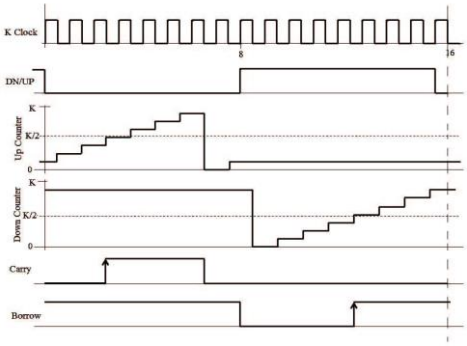

Fig.3. EXOR Gate phase detector and its corresponding waveform

*B. Digital Loop Filter*

The K counter consists of two independent counters, which are usually referred to as "UP-counter" and "DOWN counter". In reality, however, both counters are always counting upward. K is the modulus of both counters; that is, the contents of both counters are in a range from 0 . . . K-1. K can be controlled by the K modulus control input and is always an integer power of 2.




(a)




(b)

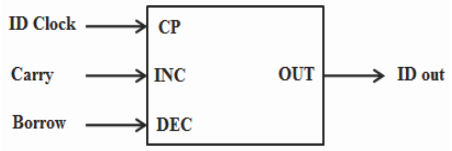
Fig.4. K Counter Loop Filter (a) Block Diagram (b) Corresponding Waveform

When DN/UP signal is high, the down counter is active and the contents of up counter will be frozen. In opposite case, When DN/UP is low, the up counter counters and down counter

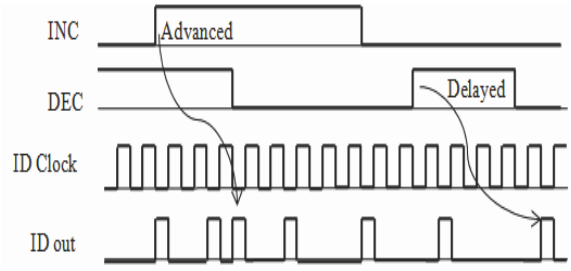
remains in frozen. Both counters resets to zero when their content exceeds K-1. Carry and borrow is the MSB bits of up and down counter respectively [10].

*C. Digital Controlled Oscillator*

A variety of DCOs can be designed. Depending upon output of the loop filter they change their frequency. Increment Decrement counter is used for our ADPLL design.ID counter is used for DCO in this design. It has three inputs: a clock input, increment and decrement. When there is no carry or borrow pulse; The ID counter gives output pulse on every second ID clock. When a carry pulse appears at the INC input then the next ID pulse is advanced in time by one ID clock period and when borrow pulse appears at the DEC input then the next ID pulse is delayed in time by one ID clock period.




(a)




(b)

Fig.5. ID counter (a) Block Diagram (b) Corresponding Waveform

The disadvantage of above design [10] [11] is that when up and down counters are in frozen state, the clock is fed to the both counter that makes the design to consume unnecessary dynamic power. This also results the increment in the overall power consumption of the ADPLL circuit.

## 3. PROPOSED ADPLL ARCHITECTURE

In the proposed ADPLL circuit, the modified K counter is designed using the dynamic power reduction technique known as clock gating. The conventional K counter in ADPLL circuit is replaced by the Modified K counter. In the further section clock gating technique, proposed k counter and proposed ADPLL is explained.

*A. Clock Gating Technique*

Clock gating is the most popular and effective technique to reduce the dynamic power consumption into the digital circuits [9]. The purpose of gating is to stop the switching activities of the clock when the circuit is inactive or in frozen state. In this work, the latch based clock gating [9] has been used. Fig. 6 gives an overview of the clock gating technique that has been used.

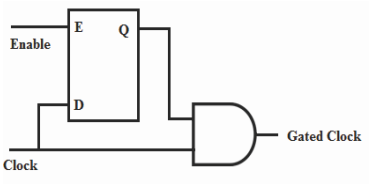



Fig.8. Proposed ADPLL circuit

The main goal of using the clock gating technique is to suppress the propagation of transition. The sources of the power consumption in the circuits are due to charging and discharging of the capacitors, so if the switching activities, transitions at the nodes reduce then the power dissipation also reduces. These switching activities are decreased by gating those modules which are idle and hence avoiding the unnecessary power consumption.

*B. Proposed K counter*

The digital loop filter i.e. K counter with gated clock is given in Fig.7.When the DN/ signal is low, the upper gating circuit CG 1 in proposed K counter outputs the clock which is fed to the Up Counter while the lower gating circuit CG 2 prevents the clock being fed to down counter. In the same way, when the DN/ is high, the clock is only fed to down counter and the upper gating circuit shut off the clock for the counter.

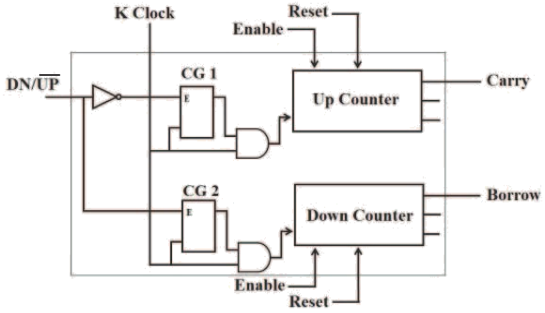



Fig.7. K Counter with Gated clock

### C. *Proposed ADPLL using modified K counter*

The proposed ADPLL is shown in Fig.8. When the K counter with gated clock is used in the ADPLL, the overall reduction in power can be achieved.

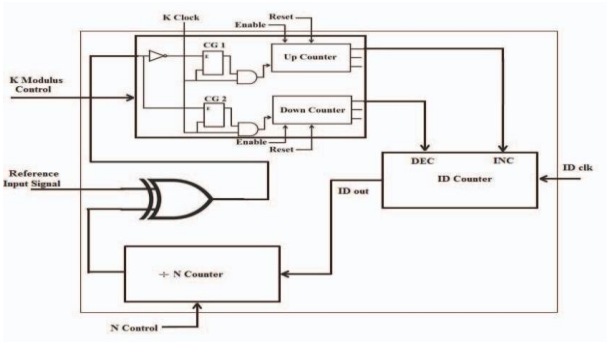



Fig.8. Proposed ADPLL circuit

## 4. EXPERIMENTAL SETUP AND SIMULATION RESULTS

The functional blocks of the proposed ADPLL are implemented by using Verilog-HDL and synthesized using the Cadence RTL Compiler tool using gpdk 45nm CMOS technology library. The parameter detail of designed ADPLL is given in TABLE I. To use the sane signal generator for the K clock and ID clock, in this work M = 2N is taken and for minimum ripple M=4K is taken [10].

TABLE I. PARAMETER DETAIL OF DESIGNED ADPLL

| Parameter | ADPLL Design |
|---|---|
| K | 4 |
| M | 16 |
| N | 8 |
| Center Frequency ($f_0$) | 625 KHz |

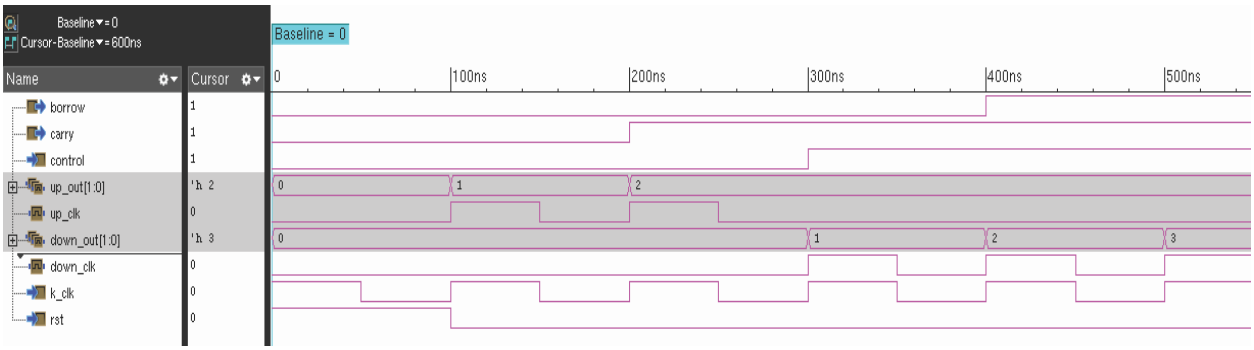
The dynamic power and the total power of the conventional K counter and optimized K counter is compared. It is observed from the obtained result that optimized K counter has reduced dynamic power and total power to 72.8% as given in TABLE II.

TABLE II. PERFORMANCE OF K COUNTER

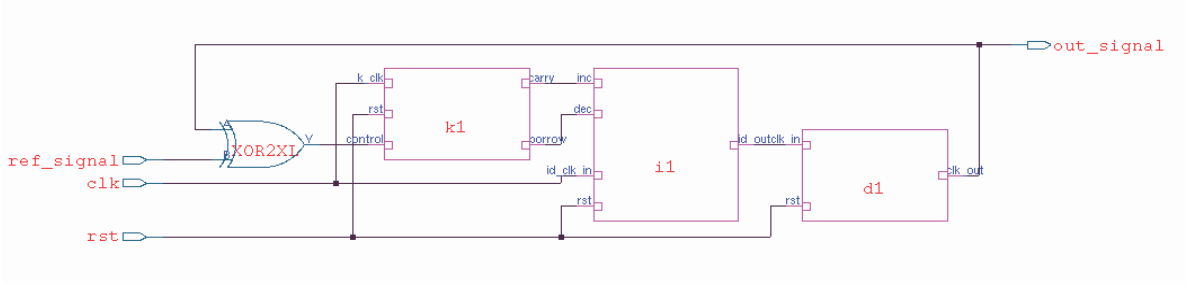
| K Counter | Dynamic Power | Total Power |
|---|---|---|
| Conventional | 240.74nW | 241.593nW |
| Modified | 64.510nW | 65.535nW |

The simulated output of optimised K Counter and the proposed ADPLLis shown in Fig. 9(a) and 9(c) respectively. The schematic diagram of the synthasised proposed ADPLL is shown in Fig. 9(b).

The results obtained after the synthesis has benn compared with previous works and shown in TABLE III.




(a)

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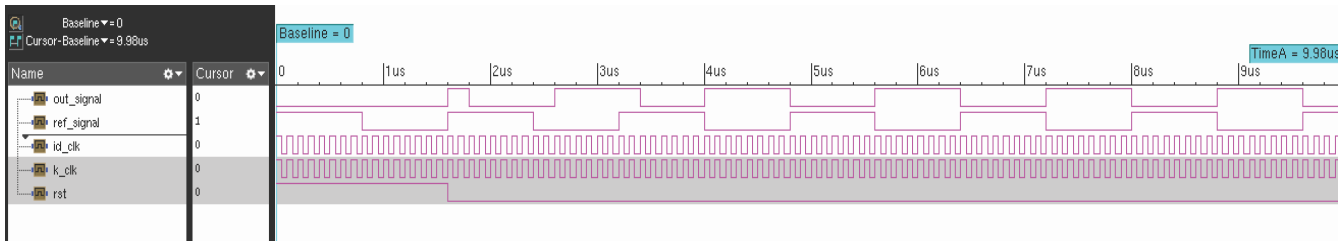


(c)

Fig.9. (a) Simulated Output of Optimized K Counter (b) Schematic representation of proposed ADPLL

(c) Simulated output of proposed ADPLL

TABLE III. PERFORMANCE SUMMARY AND COMPARISION

| | This Work | Ref [11] | Ref [8] | Ref [6] | Ref [5] |
|---|---|---|---|---|---|
| **Process** | 45nm | 45nm | 130nm | 90nm | 0.18µm |
| **Supply** | 1V | 1V | 0.7V | 1.0/1.2V | 1.8V |
| **Power** | 0.704µW | 0.883µW | 840µW | 8/9.6mW | 1.8mW |
| **Area** | 207µm$^2$ | 195 µm$^2$ | - | 0.34mm$^2$ | 0.1mm$^2$ |
| **Lock in Time** | 3.2 µs | 3.2 µs | 80µs | 0.74µs | - |

## 5. CONCLUSIONS

In this paper power efficient ADPLL is designed with power optimized digital loop filter. The power consumption of digital loop filter is minimized with the help of clock gating technique. The proposed ADPLL consumes 0.704µW power which is lesser than prior works. Therefore it can be termed as low power, simple and efficient VLSI implementation.

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