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Low Power Hilbert Transformer Design with Reconfigurability using Row Bypassing Multiplier

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Abstract - *Low power and reconfigurability have always been the main concern for the efficient filter implementation. This paper introduces two new low power and high speed reconfigurable Hilbert transformer designs. These designs are based on the carry save adder (CSA) and ripple carry adder (RCA) based row bypassing multipliers. The primary power reduction is procured by turning off adders when the multiplier operands are zero. In addition, the proposed Hilbert transformers are implemented with parallel architecture of multipliers to shorten the delay time. The proposed designs can be dynamically reconfigured with arbitrary coefficients that are only limited by their length and word size.*

The effectiveness of the proposed design method is presented with an example. The performance of both the designs is evaluated in terms of area (number of slices), speed, i.e., maximum frequency and power consumption. The results depict that the CSA row bypassing multiplier based Hilbert transformer achieves 17% increase in speed and 13% area reduction in comparison with RCA row bypassing multiplier based Hilbert transformer. While the power dissipation of the later transformer is 65% less than the former one.

Key Words*: *Hilbert transformer, IIR Digital filters, Row bypassing multiplier, Carry save adder, Ripple carry adder.

1. INTRODUCTION

Rapid technological change has compelled manufacturing to stand a brand new monetary objective: reconfigurability, i.e., the capability of reconfigurable computing of a device, in order that its conduct may be modified by reconfiguration. Power intake is every other vital difficulty within the layout of nowadays and future digital systems. For a long battery lifetime in transportable gadgets such as clinical equipment, low strength intake is needed. Recently, with the onset of software described radio (SDR) era, digital signal processing and biomedical engineering, research is now focused on low energy reconfigurable realizations of digital filters. Recently, many reconfigurable finite impulse reaction (FIR) virtual filters have been proposed in literature [3]. It is understood that the FIR filter consumes extra computational strength compared to a limitless impulse response (IIR) filter with comparable sharpness or selectivity, in particular while low frequency cutoffs are wanted.

Also, the IIR filter realization has a bonus over FIR filter realization in term of variety of coefficients and applied mathematics performance [5], [6]. In our paper, we've got utilized one among the famous IIR filter digital structure, i.e., direct form II for the conclusion of Hilbert transformer.

In signal process, Hilbert transformer is taken into account as a very important tool and notice applications in several areas like digital communication wherever it's used for single side-band modulation and edge detection of digital pictures [6],[8]. Antecedently FIR and IIR digital primarily based Hilbert transformers are developed victimization many ways specifically the Remez exchange formula [9], Eigen filter methodology [10], and weighted least sq. technique [11]. Numerous methodologies for implementing the Hilbert transformer were additionally investigated that includes of switched-capacitor implementation [12], neural network [13], and multiplier-less triangular array realization [14]. However, it's discovered that these approaches are appropriate for the fastened constant applications. The FPGA implementation of quick Fourier remodel (FFT) primarily based Hilbert transformation is given in [15] [16]. Although, these filters don't seem to be reconfigurable in nature. Whereas in current state of affairs, reconfigurability is demanded. This drawback is dealt during this paper. So as to design a low power reconfigurable digital filter, one ought to concentrate on multipliers to form them economical as these are the foremost space and power intense components. Hence, by reducing the power consumption in multipliers an oversized power will be saved. During a logic circuit, the power dissipation is distinguished as static and dynamic power dissipation. The static power consumption is proportional to the amount of transistors used. Whereas the dynamic power dissipation depends upon charging and discharging of load capacitance [17].

The average dynamic power dissipation of a CMOS gate is

$$P_{avg} = 1/2CfV_{dd}2N \quad (1)$$

where,

C is that the load capacitance,

V_{dd} is that the power offer voltage,
f is that the clock frequency, and
N is that the range of switch activity during a clock cycle.
Thus, by reducing the switch activity of a given logic circuit, the power consumption are often reduced while not fixing it's perform.

In this work, 2 new reconfigurable Hilbert transformers supported low power, row bypassing multipliers are proposed. Hilbert transformers are enforced exploitation 2 multipliers proposed in [10] and [11], severally. The multiplier factor design [9] is exploitation carry save adders and a final ripple carry adder for its implementation. Whereas in [9] the number relies on solely ripple carry adders. The filter coefficients are directly saved into look-up-table (LUT). These coefficients are accessed by multipliers. The performance is compared in terms of speed, i.e., most frequency, space (number of slices) and power consumption. The proposed Hilbert transformer can be enforced and utilized in those applications wherever filter coefficients have to be compelled to modification like in communication systems.

2. HILBERT TRANSFORMER

Hilbert transformers are wide utilized in signal process applications. Correct frequency-domain algorithms for designing Hilbert transforms exist, but these algorithms necessitate costly FFT computations and block-based process. Economical implementations are often accomplished exploitation IIR filters.

It is identified that there exists a particular relation between the distinct Hilbert transformer and sophisticated half-band filter. Complicated half-band filter satisfies frequency domain constraints of the Hilbert transformer [5]. The frequency response of the best Hilbert transformer is characterized as

$$H_{HT}(e^{j\omega}) = \begin{cases} j, & -\pi < \omega < 0 \\ -j, & 0 < \omega < \pi \end{cases} \quad (2)$$

The advanced half-band filter is simply procured by adding a shift of π/2 radians within the real half-band filter's frequency response [5]. the important half-band filter G(z) is written as

$$G(z) = \frac{1}{2}[A_1(z^{-2}) + z^{-1}A_2(z^{-2})] \quad (3)$$

where, $A_1(z)$ and $A_2(z)$ represents are stable allpass filters. once applying frequency transformation, advanced half band filter are often procured from half-band filter [20] exploitation

$$H(z) = jG(-jz) \quad (4)$$

The resultant advanced half-band transfer perform is expressed as

$$H(z) = \frac{1}{2}[A_1(-z^{-2}) + jz^{-1}A_2(-z^{-2})] \quad (5)$$

Where $A_1(-z-2)$ and $A_2(-z-2)$ represents real and stable all pass filter. it's to notice that if G(z) may be a half-band low pass filter with its passband on the correct half the unit circle, then by applying the frequency transformation, H(z) becomes the complicated half-band filter with its passband on the higher half of the unit circle [21]. The complicated half-band realization victimization all-pass filter is shown in Fig. 1.

The all pass filter block within the advanced half-band filter realization is replaced with the direct kind II structure of all pass filter to get the canonic structure to Hilbert transformer. In canonic realization, multiplier factor coefficients of the structure are primarily the filter coefficients [5]. the specified range of coefficients for the conclusion of the ordinal order IIR filter are 2N +1using canonic structures.

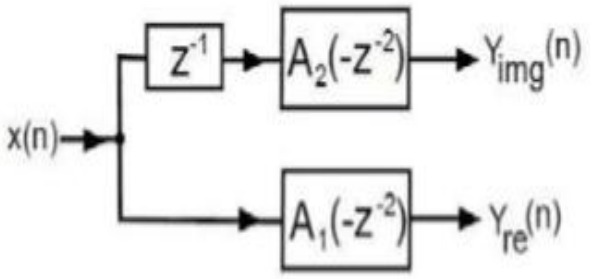

Figure 1. Realization of Complex half-band filter using All pass filter.

Fig. 1. Complex half-band filter realization using All pass filter.

3. PARALLEL MULTIPLIER

Consider the multiplication of 2 unsigned n-bit numbers, wherever A = $a_{n-1}a_{n-2}$ ...a_0 is that the multiplicand and B = $b_{n-1}b_{n-2}$ ...b_0 is that the multiplier. The product P = $p_{2n-1}p_{2n-2}$ ...p_0 is written as follows:

$$P = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}(a_i \cdot b_j)2^{i+j}$$

An example of an unsigned 4×4 multiplication is shown

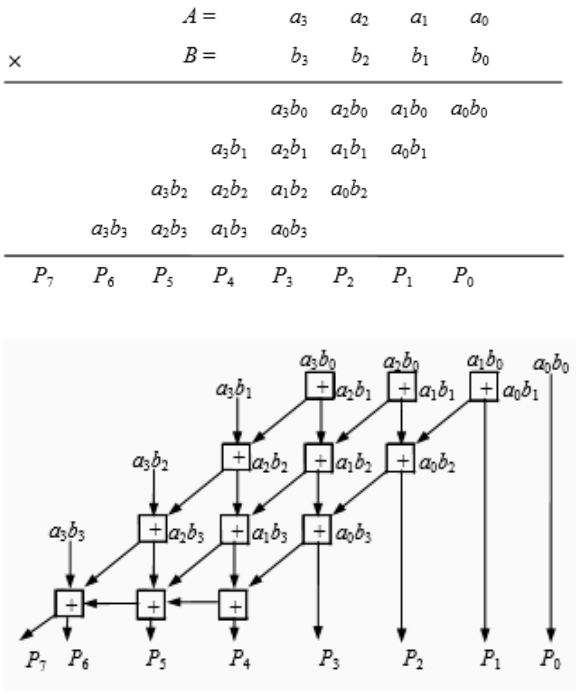

Figure. 2. A 4×4 Braun multiplier

An array implementation, called the Braun multiplier [2], is shown in Figure 2. On the other hand, the Baugh Woolley number [3] uses constant array structure to handle 2's complement multiplication, with a number of the partial product replaced by their complements. The multiplier factor array consists of (n–1) rows of carry-save adders (CSA), during which every rows contains (n–1) full adders (FA). The last row could be a ripple adder for carry propagation.

4. LOW POWER ROW BYPASSING MULTIPLIER

In this paper, we shall propose a design with low power for this multiplier.

The utilization of power of a multiplier can be lessened through multiplexers by killing the segments when operands of multiplier are zero. The average contribution of zero of the multiplier operand is found as 73.8% in customary DSP applications [19]. For this, to lessen control utilization control and speed increment, push bypassing methods are utilized as a part of multipliers. These multipliers with bypassing technique can be composed utilizing CSA and RCA portrayed as takes after.

4.1 CSA BASD ROW BYPASSING MULTIPLIER

The motivation behind line bypassing multiplier [18] is to handicap adders in the j^{th} row if the bit y_j is zero in the multiplier, i.e., every one of the bits in the $x_i y_j$, $0 \le i \le n-1$, are zero, where n is the word length of operands.

Consequently, lessened in the power scattering. Modify the ordinary full adder keeping in mind the end goal to deactivate the adder of a specific row as appeared in Fig. 2.

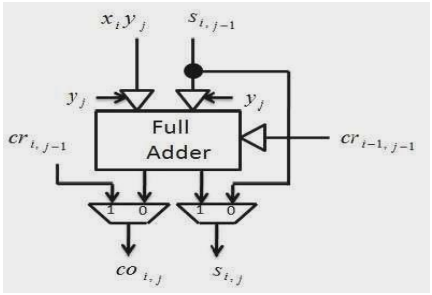

Fig. 2. Full adder cell with modification.

Where tri-state buffers are applied with the inputs x_i, y_j and cr and $s_{i,j}$ and $co_{i,j}$ are the outputs. 2 multiplexers are used at the outputs to perform bypassing technique. The decision to disable the adder is taken by the applied tri-state buffers when the value is zero at the multiplier bit y_j. The correct outputs are selected by using multiplexers.

We need to use signed multiplier, because the input vectors and coefficients in Hilbert transformer may be positive or negative. Therefore, by using the modified adder cell in Fig. 2., a 8×8 signed Braun multiplier is designed.

4.2 RCA BASED ROW BYPASSING MULTIPLIER

The row bypassing multiplier based on RCA is presented in [19]. The basic adder cell has one output two inputs.

Hence, if the bit y_j is zero in the multiplier, the adder operation is disabled by only two tri-state buffers. Also, to select correct output only one multiplexer is required as compared to CSA based multiplier. Due to the longer critical path RCAs are rather slow compared to CSAs. Therefore, speed is enhanced by using two 8 × 4 multiplier blocks by which parallel architecture of an 8 × 8 signed multiplier is designed.

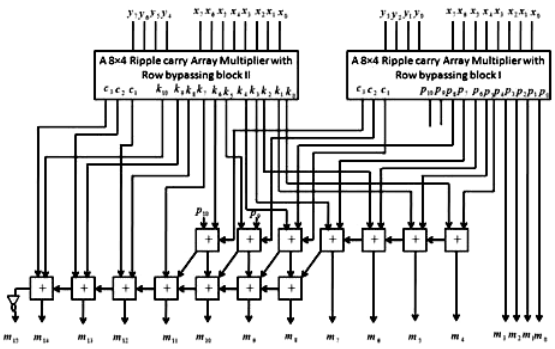

Fig. 3. CSA based 8×8 signed row bypassing multiplier

4.3 Example

The real half band filter specifications are as follows: edge frequency of stop band, ωs =0 .6π and stopband ripple, δs =0 .016. For these specifications, the transfer function of the real-half band filter is given by

$$H(z) = \frac{1}{2}\left[\left(\frac{0.236471021 + z^{-2}}{1 + 0.236471021z^{-2}}\right) + z^{-1}\left(\frac{0.7145421497 + z^{-2}}{1 + 0.7145421497z^{-2}}\right)\right]$$

The resultant complex half-band filter transfer function is obtained by applying frequency transformation as

$$H(z) = \frac{1}{2}\left[\left(\frac{0.236471021 - z^{-2}}{1 - 0.236471021z^{-2}}\right) + jz^{-1}\left(\frac{0.7145421497 - z^{-2}}{1 - 0.7145421497z^{-2}}\right)\right]$$

where

$$A_1(-z^{-2}) = \frac{0.236471021 - z^{-2}}{1 - 0.236471021z^{-2}}$$

and

$$A_2(-z^{-2}) = \frac{0.7145421497 - z^{-2}}{1 - 0.7145421497z^{-2}}$$

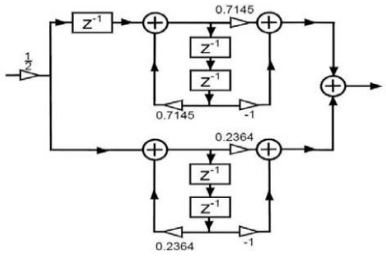

Figure 4. Realization of Direct form II Hilbert Transformer

5. RESULTS

5.1 Simulation results

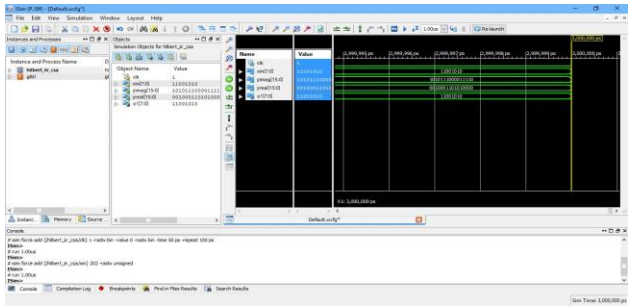

Figure 5. IIR filter Output (CSA based)

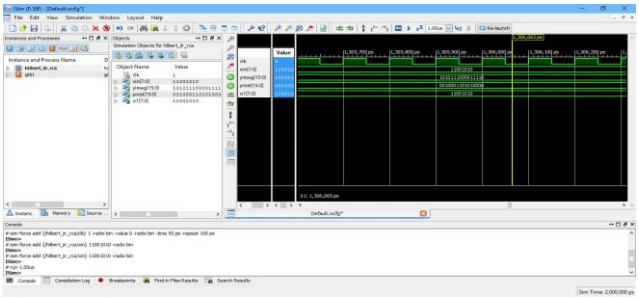

Figure 6. IIR filter Output (RCA based)

5.2 Design summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	42	54576	0%
Number of Slice LUTs	245	27288	0%
Number of fully used LUT-FF pairs	27	260	10%
Number of bonded IOBs	41	218	18%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Figure 7. Design summary of RCS based filter

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	47	54576	0%
Number of Slice LUTs	250	27288	0%
Number of fully used LUT-FF pairs	27	270	10%
Number of bonded IOBs	41	218	18%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

Figure 8. Design summary of CSA based filter

5.3 Timing summary

CSA based filter:

```
Minimum period: 3.151ns (Maximum Frequency: 317.360MHz)
Minimum input arrival time before clock: 2.897ns
Maximum output required time after clock: 13.790ns
Maximum combinational path delay: 13.633ns
```

RCA based filter:

```
Minimum period: 3.151ns (Maximum Frequency: 317.360MHz)
Minimum input arrival time before clock: 2.897ns
Maximum output required time after clock: 13.790ns
Maximum combinational path delay: 13.633ns
```

5.4 Power report

- Dynamic total power of CSA Based IIR filter is 0.342mW.
- Dynamic total power of CSA Based IIR filter is 0.343mW.

6. CONCLUSIONS

The efficient implementation of Hilbert transformer is proposed with high speed and low power. By turning of the adders The primary power is reduced when zero is at the multiplier operands. Therefore, Hilbert transformer is designed using row bypassing multipliers based on CSA and RCA.

In addition Due to the longer critical path RCAs are rather slow compared to CSAs. Therefore, to shorten the delay time, speed is enhanced in RCA row bypassing multiplier based transformer by a parallel architecture of multiplier. By only limiting the arbitrary coefficients length and word size, the proposed designs can be dynamically reconfigured.

The power dissipation, speed and area are performance parameter of the two implementation.

The result indicate that Hilbert transformer based on CSA row bypassing multiplier is better with respect to area and speed while Hilbert transformer based on RCA is better in terms of power dissipation. Among these the designer can choose the optimum Hilbert transformer structure for a specific application.

7. ACKNOWLEDGEMENT

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